PROJECT REFLECTIONS

Henrik Schulze and Oscar Castro

Version 1.0

Based on Linköping Interaktive Project steering,
http://lips.isy.liu.se/en/lipsmallar.html /
http://lips.isy.liu.se/en/lipsmallar_engelska/17Reflections_en_c.doc

Status

Reviewed		
Approved		

On Designing a System for an FPGA – JPEG Compression Partly Accelerated

Project Group 2, 2017/Spring, Uppsala University, Department of Information Technology

Participants of the group

Name	Responsible	Phone	E-mail
Henrik Schulze	Responsible for writing the version of C code presented	0730-646272	Henrik.Schulze.0353@student.uu.se
Oscar Castro	Responsible for the accelerator design and test bench	0722714269	Oscar.Castro.6578@student.uu.se

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Course leader: Stefanos Kaxiras <stefanos.kaxiras@it.uu.se> Course director
Tutors: Mahdad Davari <mahdad.davari@it.uu.se> Teacher
Mehdi Alipour <mehdi.alipour@it.uu.se> Assistant

Contents

Document history

Version	Date	Changes	Sign	Reviewed
1.0	2017-05-26	Final presentation slides	hs,	

1 TIME REPORT

Henrik

--2017-05-18, 12 hours.

2017-05-19, 4 hours.

2017-05-20, 8 hours.

2017-05-22, 10 hours.

2017-05-23, 6 hours.

2017-05-24, 8 hours.

2017-05-25, 8 hours.

2017-05-26, 3 hours (including the presentation).

2017-06-02, 3 hours (writing these reflections).

Oscar

2017-05-15, 1 hours

2017-05-16, 1 hours

2017-05-17, 2 hours

2017-05-18, 5 hours

2017-05-19, 7 hours

2017-05-20, 5 hours

2017-05-21, 8 hours

2017-05-22, 10 hours

2017-05-23, 12 hours

2017-05-24, 12 hours

2017-05-25, 12 hours (including presentation)

2017-05-26, 1 hours (last revision of the presentation)

Summing up, Henrik estimates to have spent about 62 hours on the project, and Oscar 76 hours.

1.1 Distribution of the work between the project participants

Oscar completed lab 3 earlier than Henrik, and was therefore also able to start working on the project earlier than Henrik. Thus, Oscar solved the design and wrote the test bench in Verilog, while Henrik focused on writing the C code needed for testing the design on the FPGA hardware.

1.2 Time spent on the project

Phase	Used time
During	Henrik: 62 hours + Oscar: 76 hours

2 ANALYSIS OF WORK EFFORTS AND PROBLEMS

2.1 Collaboration in the group

Oscar worked on the design and on the test bench, and finally also on writing the C code for running the accelerated design on the FGPA hardware, Henrik and Oscar worked together in the test on the target board.

2.2 Collaboration with the supervisor

Mahdad's help on completing lab 3 was indispensable. This laid the ground for our efforts in the project.

3 FULFILLMENT OF THE GOAL

3.1 Summary of achievements

The different labs taught us programing in Verilog and its different methods, especially lab 3 showed us to load the code on the FPGA and how it interact with the C code. It works as base to start the project. One of the goals was to demonstrate how the design could be run on the FPGA hardware, and to measure the speedup. We could not get the design to run in a satisfactory way on the FPGA. However, we *did* succeed in measuring the number of cycles used by the general purpose CPU, which was around 500 cycles. By comparing with running the accelerated design in the test bench – around 200 cycles – we estimated that the maximum speedup to be expected would be in the order of 2.5.

3.2 How the study situation influenced the project

Henrik had to complete assignments in the course Computer Programming II. Those assignments turned out very time consuming which negatively impacted the time left for the project, also lab 3 impacted the group work since it also took more time for some people.

4 SUMMARY

4.1 The two most important experiences

Verilog programming and testing the design is crucial.

Learning how to flush the caches when trying the Verilog design on hardware would probably have been helpful