Features

- Powerful processing elements PE's.
- Each PE can conceivably issue a request for data in each bus cycle.
- Multiple memory modules allow concurrent responses to data access requests.
- Caching can be used to reduce data access delays (latency).
- Each PE has its own scheduler and OS running locally.

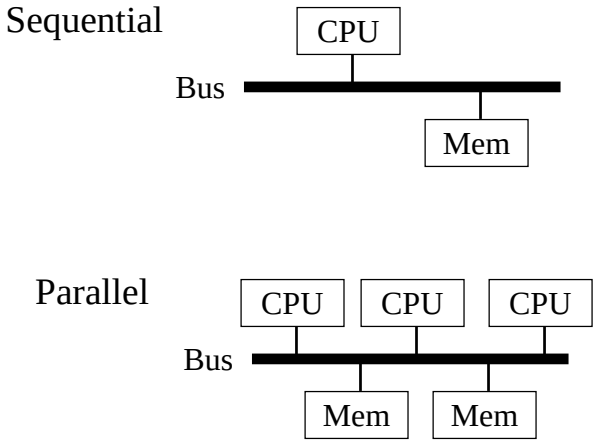
Lecture 8

Bus-based and MIN based systems, caches, combining, hotspots

Performance Issues

- Potential bottlenecks caused by shared resources. The bus is a major problem.
- How to resolve data access requests when more than one PE wants to read or write data to the same address or memory module.
- Cache consistency involves maintaining consistency between all the caches and the main memory. This requires new protocols.

Bus-based systems



Non-determinism

{x=2}
cobegin
    x= x+1;
●
    x= x+1;
coend
{x=3 ^ x=4}

Managing concurrent accesses

- What happens when two PE's try to read or write data to the same physical address in the same clock cycle.
- One solution is to impose a global order on the concurrent data accesses.
- A global order is "valid" if it can be obtained by interleaving the data accesses specified by the program, without contradicting the control flow requirements of the program.

Non-determinism

{x=2}
cobegin
    x= x+1;
●
    x= x+1;
coend
{x=3 ^ x=4}

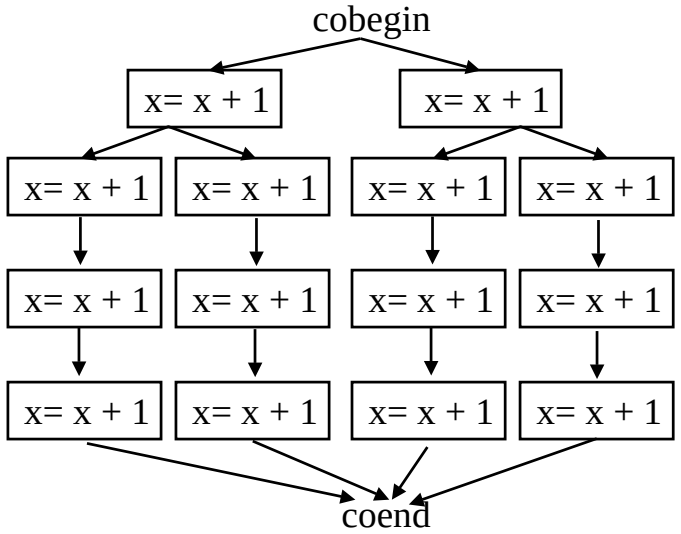
Optimising concurrent accesses

- In a bus based machine we can introduce hardware to help optimise data accesses.
- If there are multiple writes to an address in a bus cycle, only one need be forwarded to the memory.
- If several processes requre a value stored at the same address they can snoop on the bus and get the value. Only one request is needed.

Bottlenecks

- A single OS kernel, locking in the OS for access to printers, schedulers, and memory managers can degrade performance.
- The bus also restricts concurrent access. To provide a slotted bus we must effectively clock the bus at a faster rate than the PE's.
- Physical limits imply that we cannot build infinitely large machines using a bus.

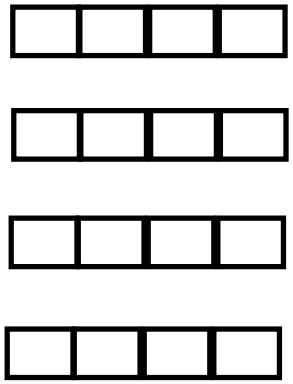
Data access interleaving



Snooping caches

- The bus allows all PE's to see all the data traffic.
- This allows them to update or invalidate their information.
- The memory merely stores data values.

Data access interleaving



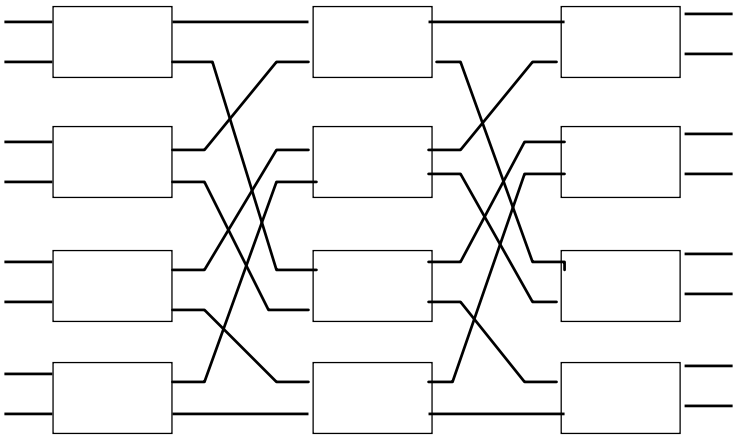
Issues with MIN's

- How to do cache consistency.
- How to do combining and routing.
- Fault tolerance.
- Hot spots.
- Tree saturation.

Cache directories

- The memory stores values and keeps track of cached copies using a directory.
- The memory classifies accesses by type, and responds accordingly.
- Read operations get a copy, the location is stored in the directory.
- Write operations use the directory to locate and update (or remove) any cached copies that exist.

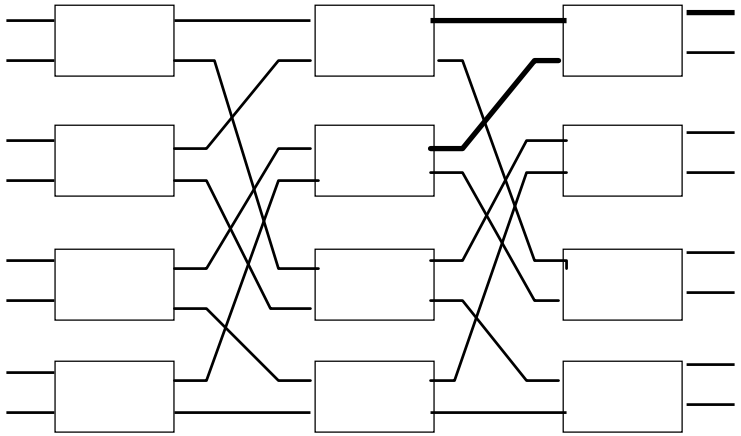
Sample MIN



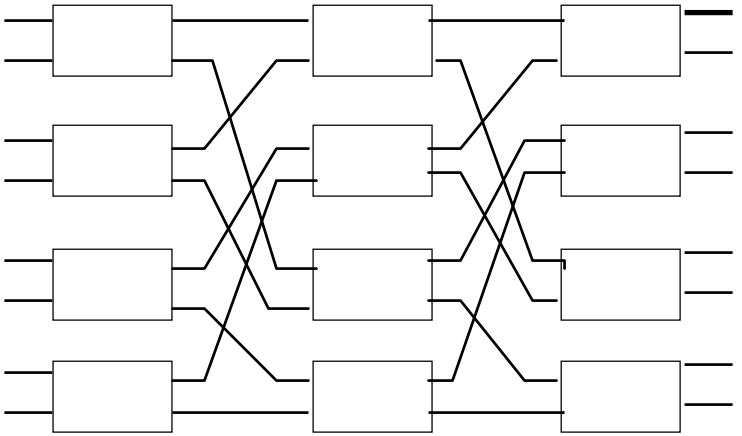
Multistage Interconnection Networks

- Provide multiple concurrent paths to memory.
- There is a unique path from each PE to each memory module.
- Simple routing.
- Uniform delay to memory.
- Traffic reduction techniques (combining).

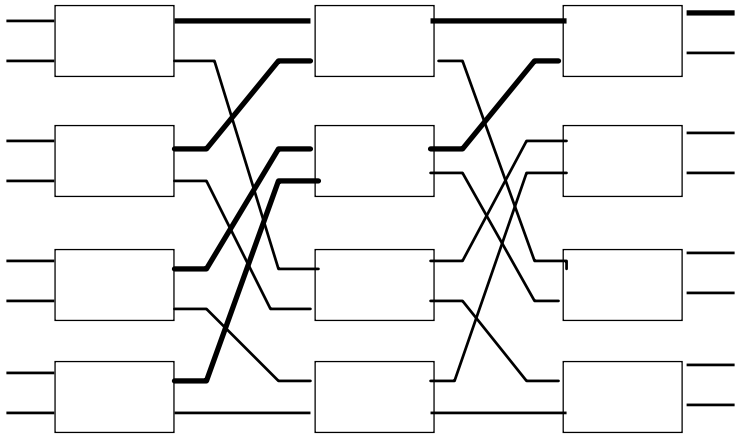
Tree Saturation



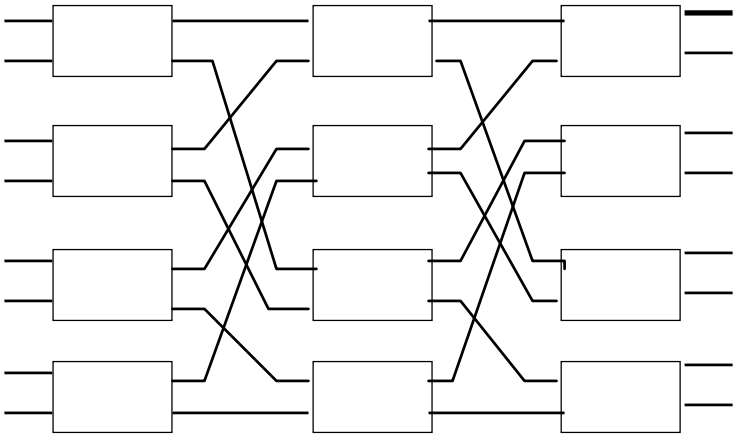
Hot Spot



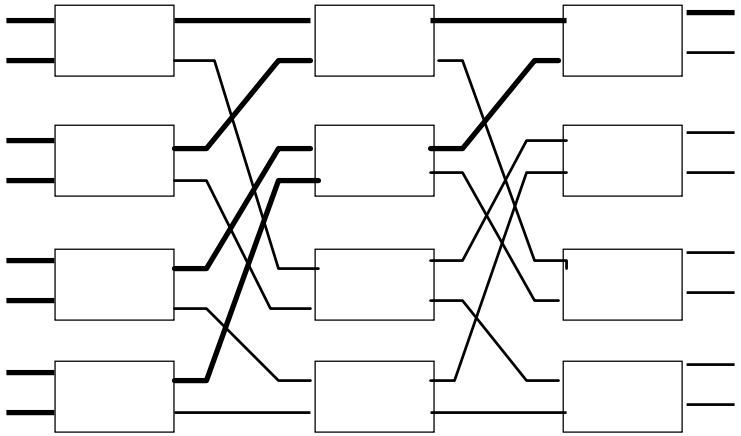
Tree Saturation



Tree Saturation



Tree Saturation



Combining

Input A	Input B	processing	reply	return A	return B
read	read	forward 1 read	yes	reply	reply
read	write	forward B	no	input B	nil
write	read	forward A	no	nil	input A
write	write	forward A or B	no	nil	nil