



- It is to provide a general and rigorous design method for system development
- "modeling" is a design process: describe the abstract behaviour of a system
- "verification" is to complement scheduling analysis to check system properties including safety and liveness-properties

Software development: the future

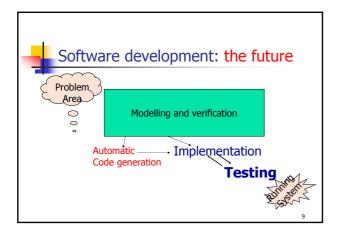
Problem
Area

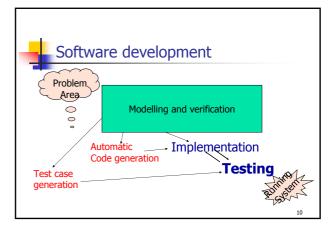
Modelling and verification

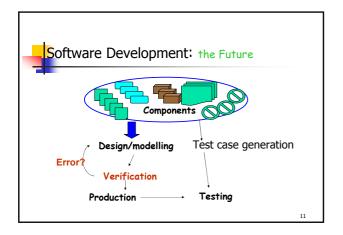
Automatic
Code generation

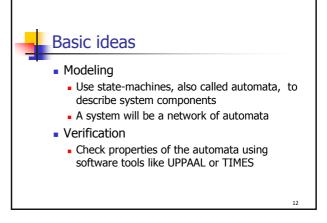
Testing

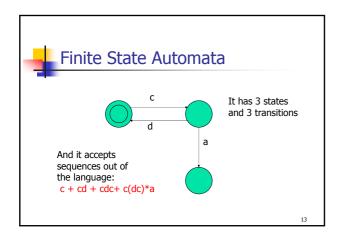
Testing

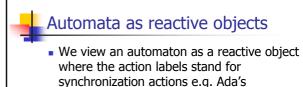








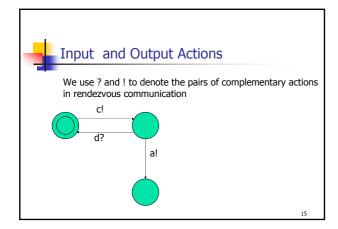


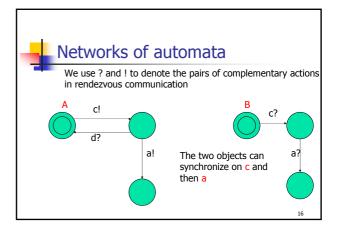


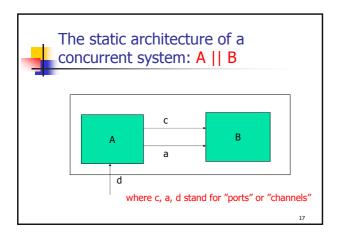
rendezvous

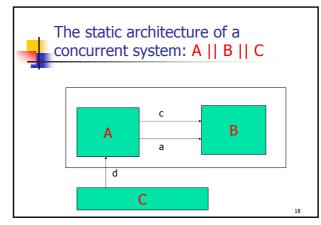
For example, the previous example could be a network protocol where c and d stand for "connect!" and "disconnect?" and a for "abort!"

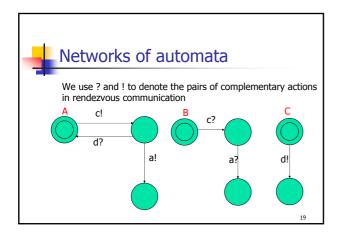
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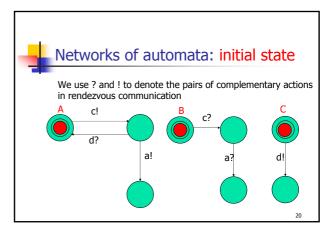


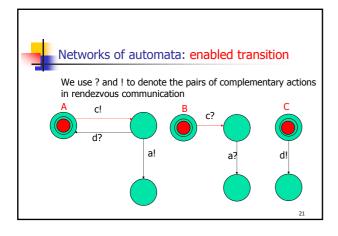


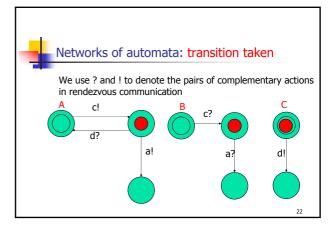


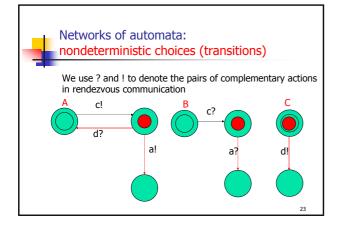


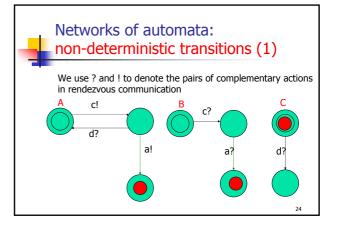


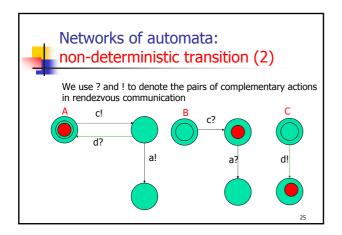


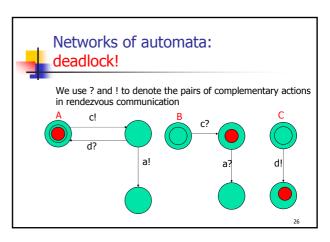


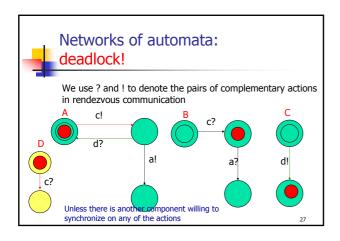


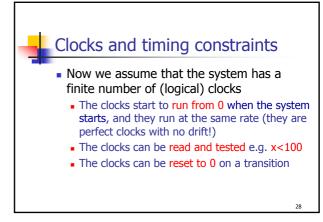


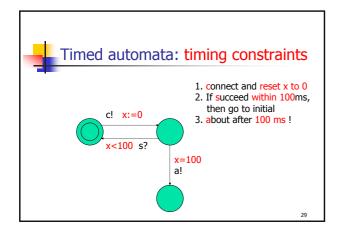


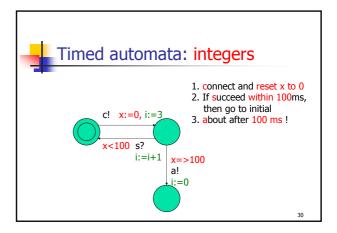


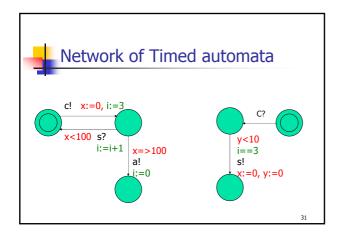


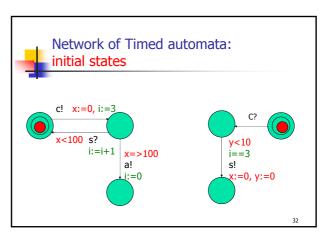


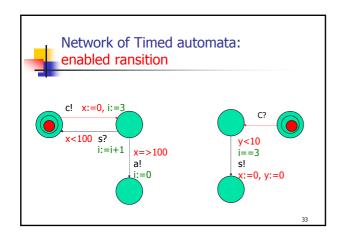


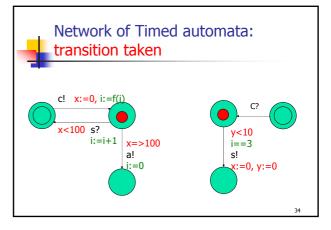


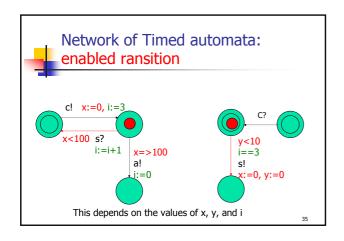


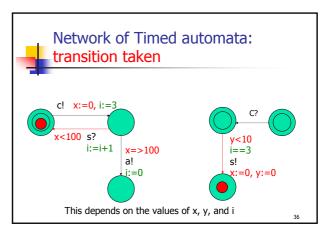














Timed automata (definition)

- a timed automaton is a finite graph
 - a finite many nodes N
 - a finite many edges between nodes E
 - an edge may be labelled with three elements
 - guard
 - action (a?, a!, or nothing)
 - assignment

(they may not appear)

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- a clock constraint
 - $g ::= x \le n \mid x \ge n \mid x < n \mid x > n \mid g \land g$
 - where n is any natuaral number
- a predicate over data variables
 - "any logical expression" you may write in C

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assignment

- a clock reset: x:=0 for any clock x
- a sequence of assignments in the form i:=e

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