# **Deciding Reachability under Persistent x86-TS0**

# K Narayan Kumar, Prakash Saivasan

Parosh Aziz Abdulla, Faouzi Atig, Ahmed Bouajjani,

# **Deciding Reachability under Persistent x86-TS0**

(Program Verification: from Sequential Consistency to Weak Consistency)

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Sequential Consistency (SC) + simple & intuitive - expensive Sequential Consistency (SC) + simple & intuitive - expensive

# Program Verification (SC)



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# Program Verification (weak consistency)

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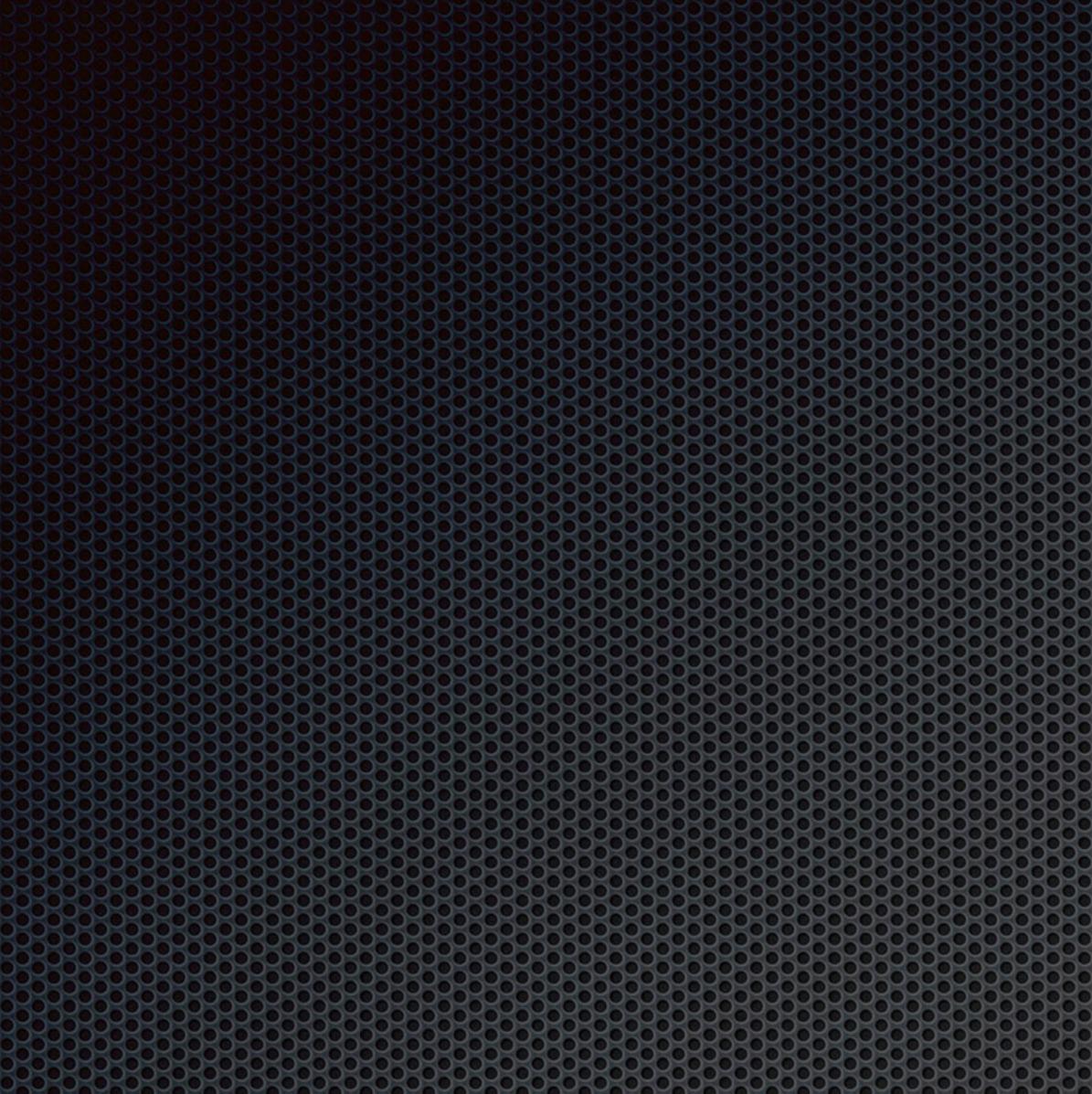
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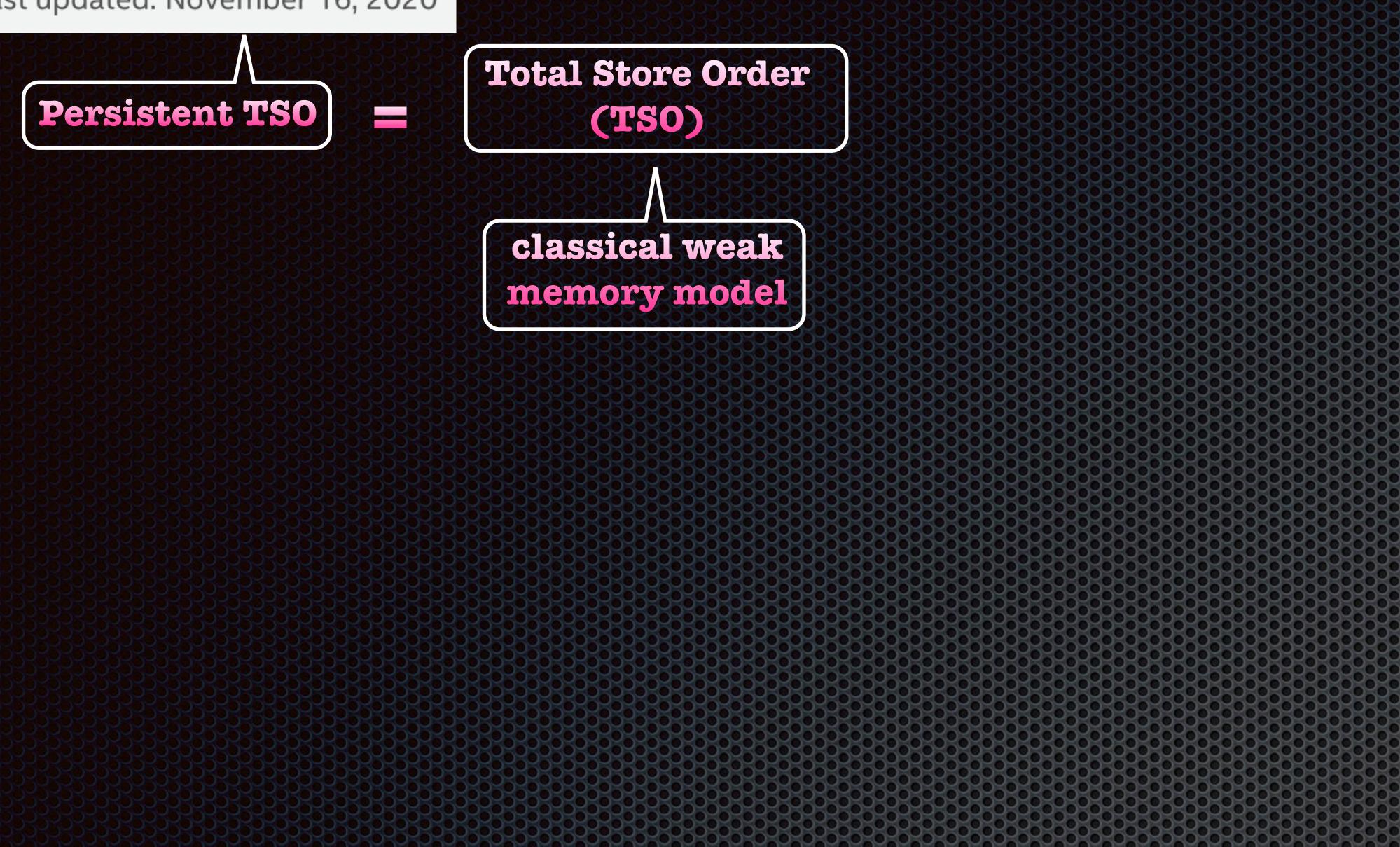






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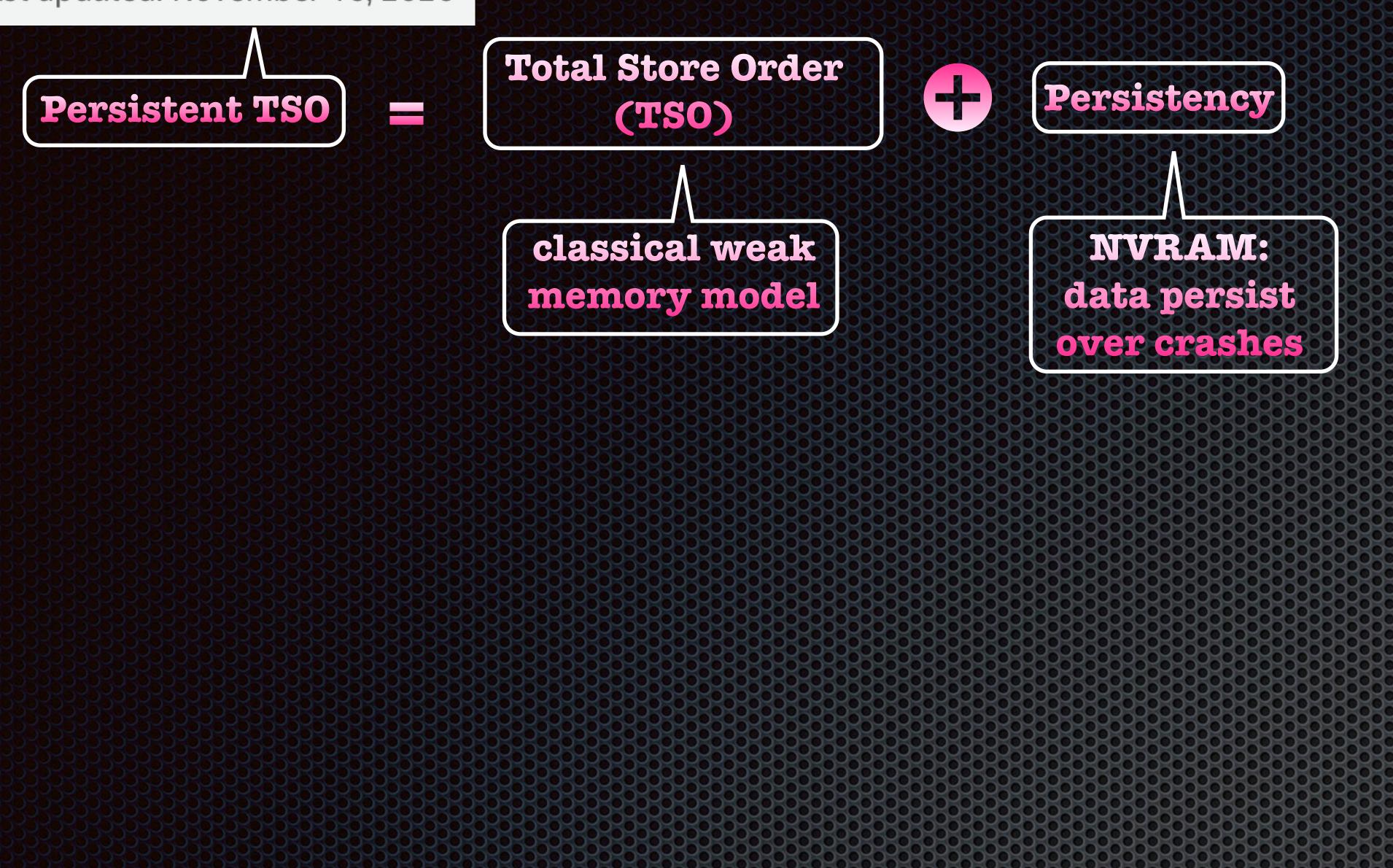


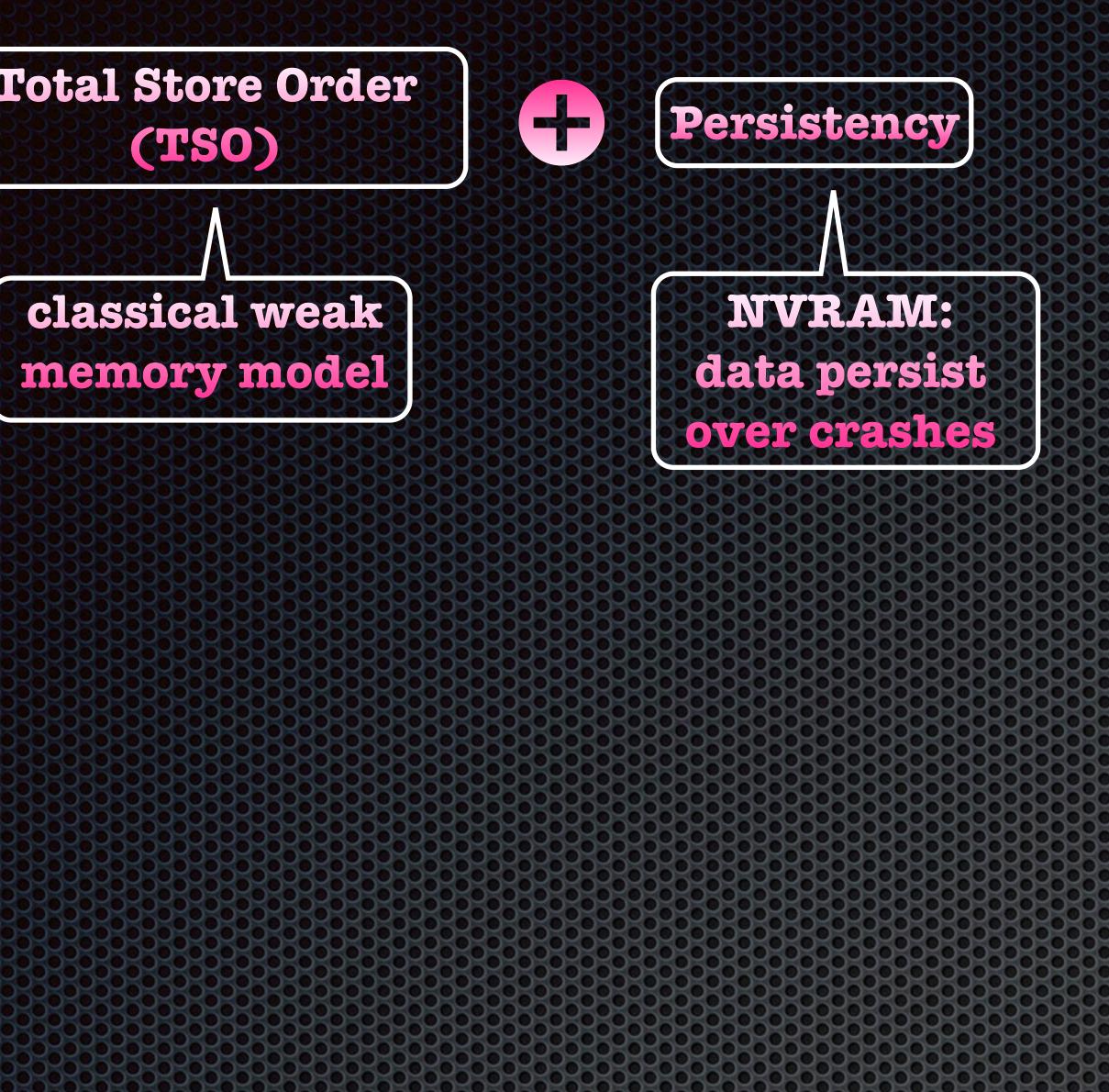




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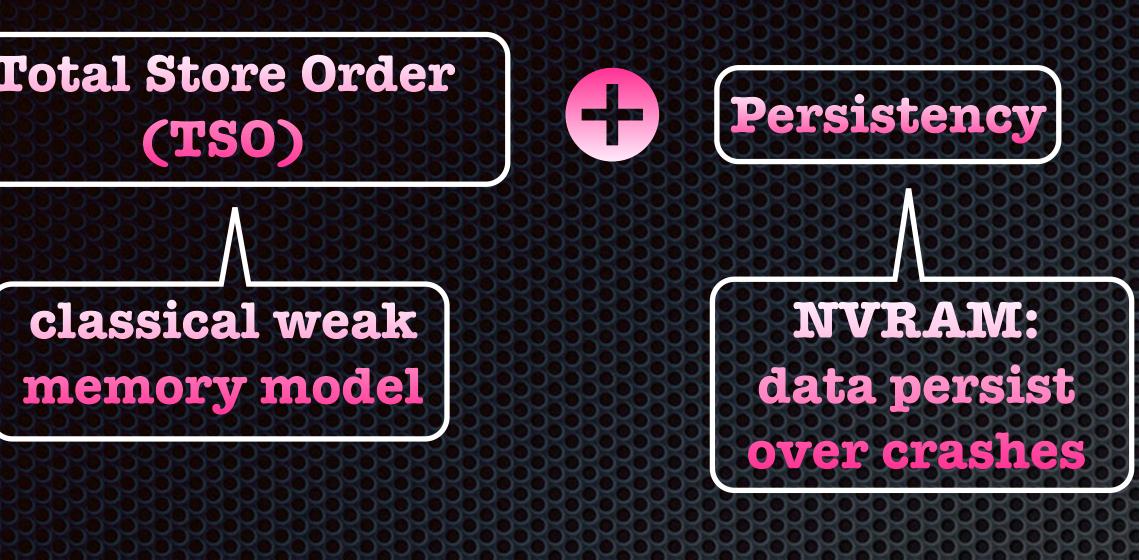




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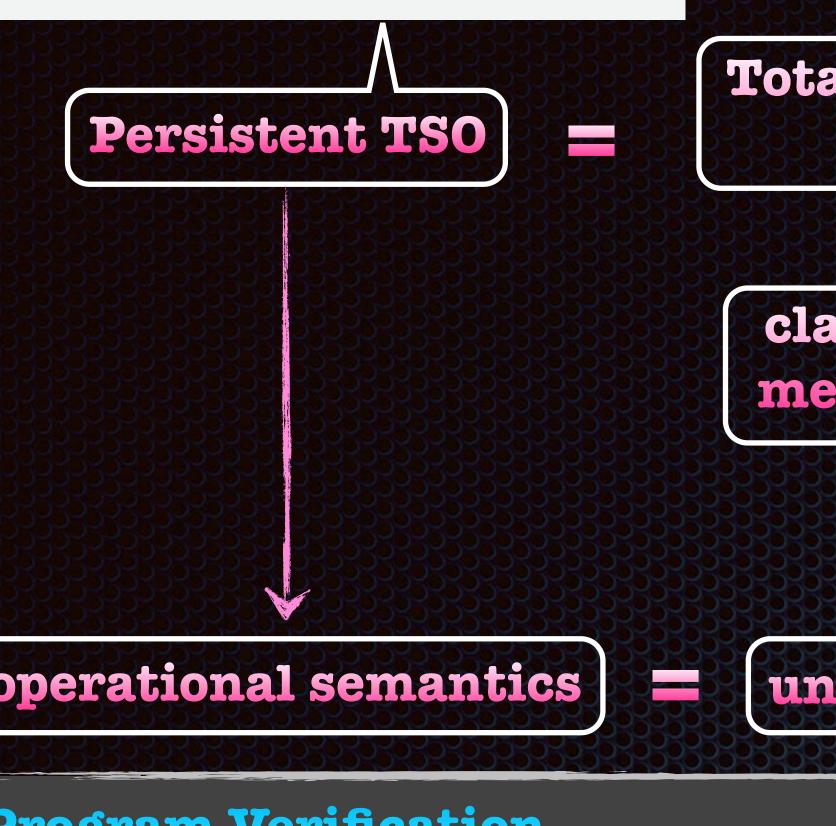
### **Program Verification** (SC)



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main stream Intel architecture: persistent x86-TSO Intel<sup>®</sup> 64 and IA-32 Architectures Software Developer's Manual Volume 1: Basic this work Architecture Last updated: November 16, 2020 **Total Store Order** Persistency -----**Persistent TSO** (TSO)classical weak **NVRAM:** data persist memory model over crashes operational semantics unbounded data structures -----



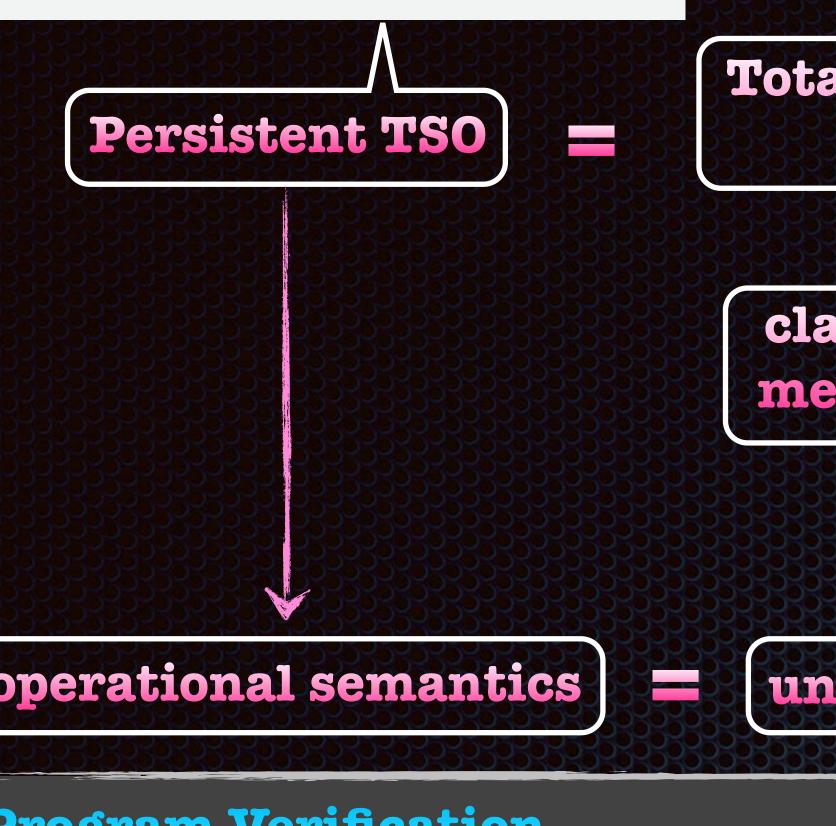


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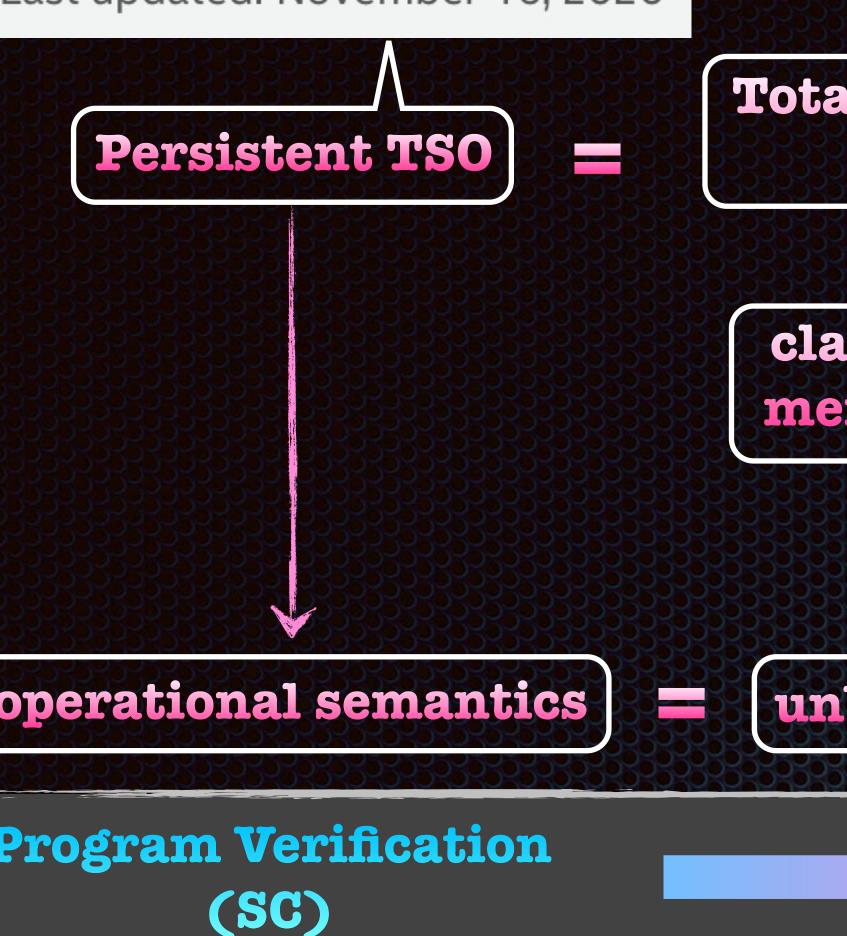


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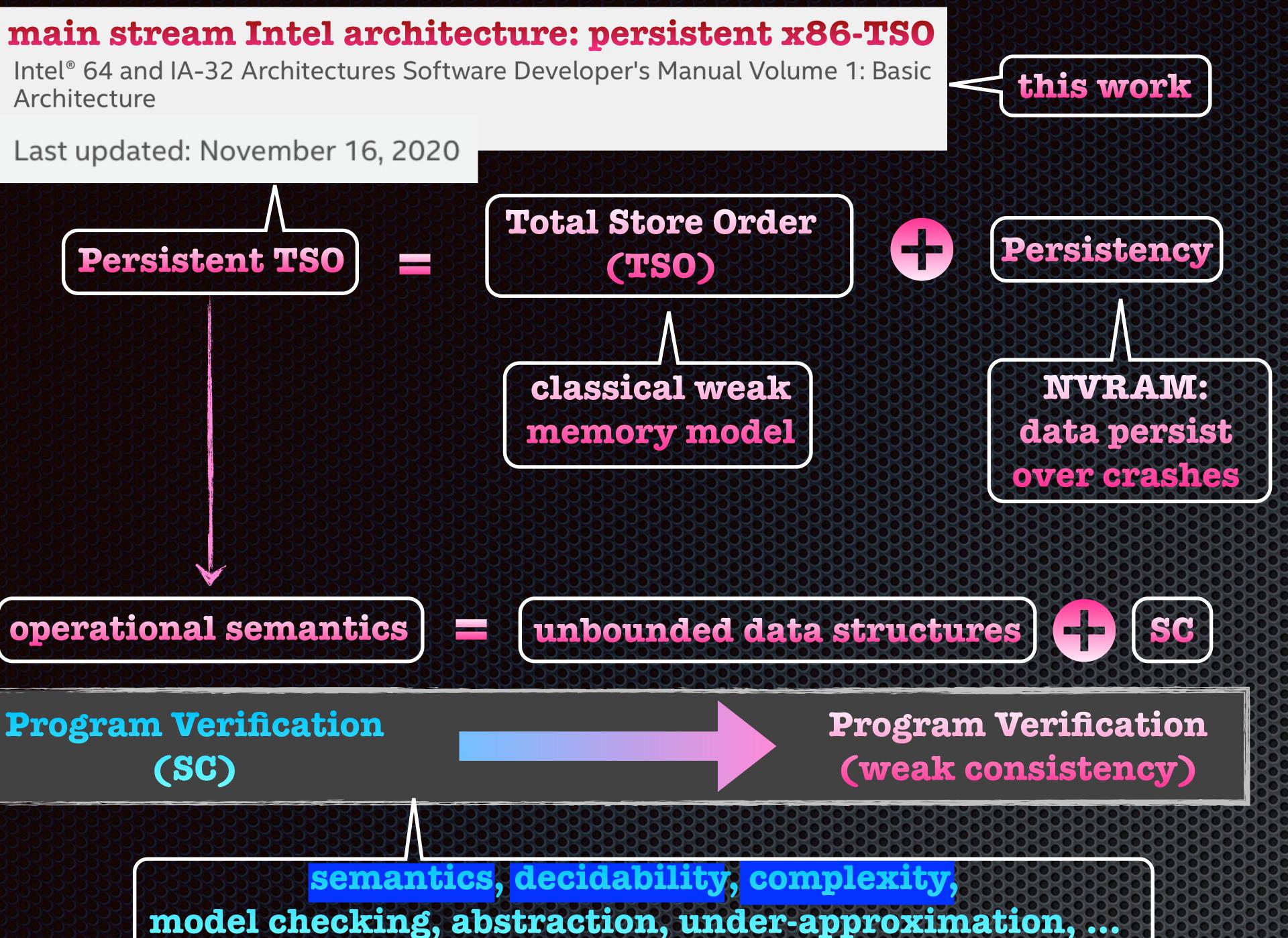




model checking, abstraction, under-approximation, ...

Architecture

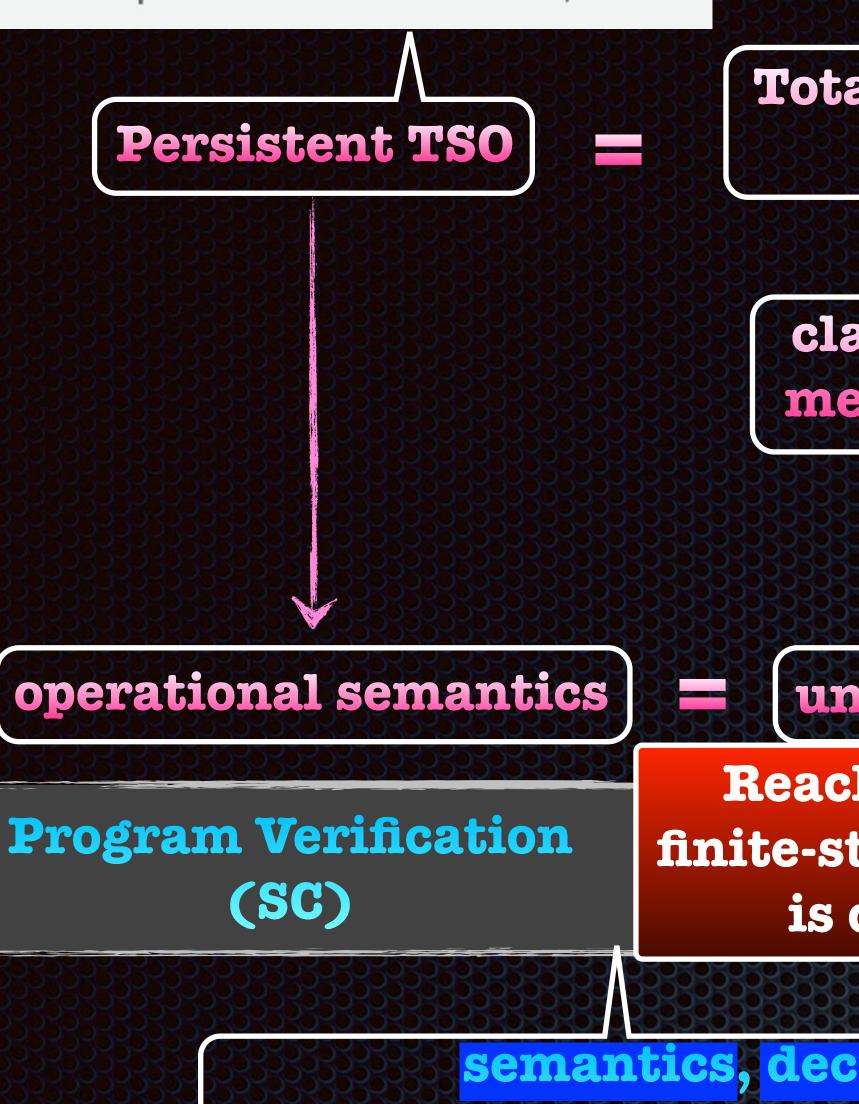






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unbounded data structures

**Reachability for** finite-state programs is decidable

**Program Verification** (weak consistency)

model checking, abstraction, under-approximation, ...





# adapting SC techniques semantics decidability



AZALEA RAAD, MPI-SWS, Germany JOHN WICKERSON, Imperial College London, UK GIL NEIGER, Intel Labs, US VIKTOR VAFEIADIS, MPI-SWS, Germany

Emerging non-volatile memory (NVM) technologies promise the durability of disks with the performance of RAM. To describe the persistency guarantees of NVM, several memory persistency models have been proposed in the literature. However, the persistency semantics of the ubiquitous x86 architecture remains unexplored to date. To close this gap, we develop the Px86 ('persistent x86') model, formalising the persistency semantics of Intel-x86 for the first time. We formulate Px86 both operationally and declaratively, and prove that the two characterisations are equivalent. To demonstrate the application of Px86, we develop two persistent libraries over Px86: a persistent transactional library, and a persistent variant of the Michael-Scott queue. Finally, we encode our declarative Px86 model in Alloy and use it to generate persistency litmus tests automatically.

CCS Concepts: • Theory of computation → Concurrency; Semantics and reasoning.

Additional Key Words and Phrases: weak memory, memory persistency, non-volatile memory, Intel-x86

### **POPL'2020**

#### Persistency Semantics of the Intel-x86 Architecture

11

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#### Taming x86-TSO Persistency

Artem Khyzha Tel Aviv University, Ori Lahav Tel Aviv University

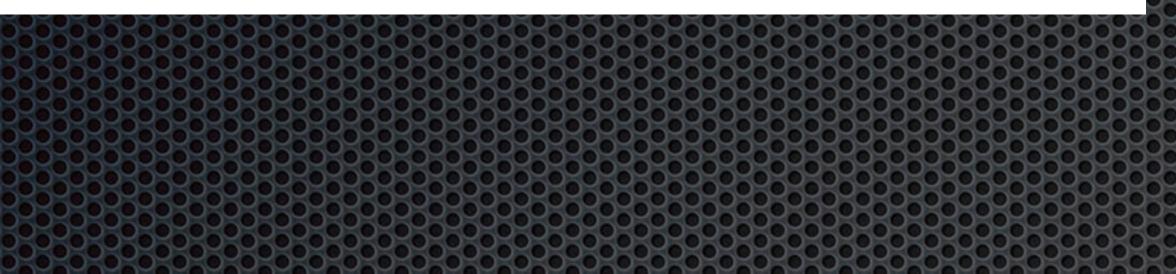
PerSeVerE: Persistency Semantics for Verification under Ext4 Michalis Kokologiannakis MPI-SWS, Germany, Ilya Kaysin National Research University Higher School of Economics, JetBrains Research, Azalea Raad Imperial College London, Viktor **POPL'2021** Vafeiadis MPI-SWS

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#### Persistency Semantics of the Intel-x86 Architecture

### **POPL'2021**





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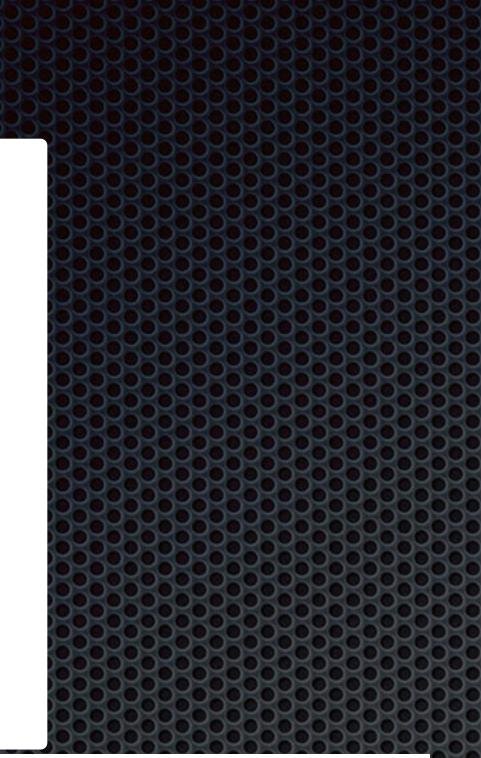


### **POPL'2020**

#### Persistency Semantics of the Intel-x86 Architecture

### **POPL'2021**





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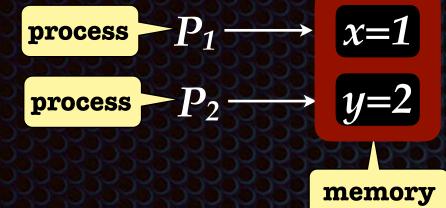
ew semantics

# adapting SC techniques





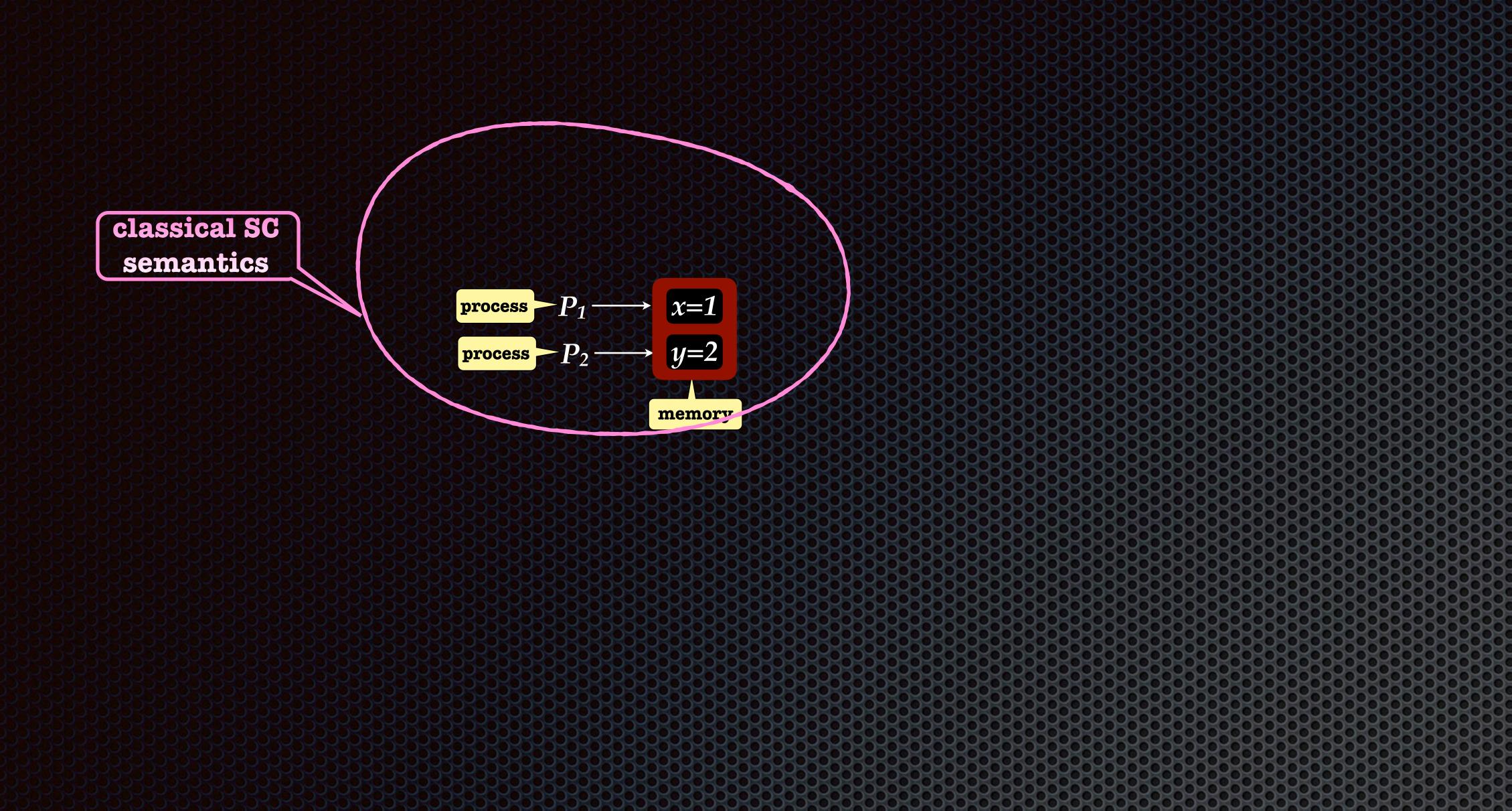
semantics decidability complexity



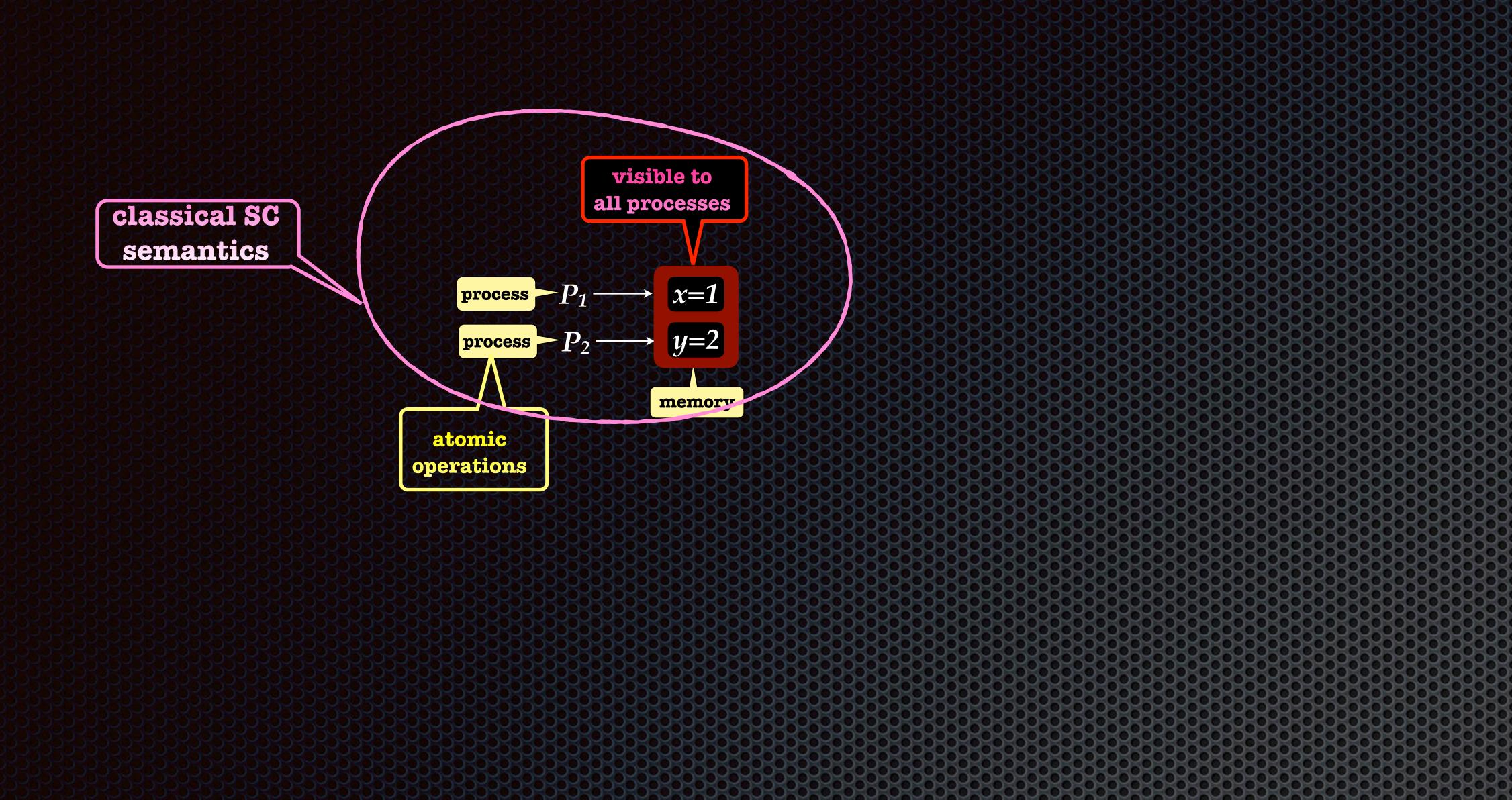








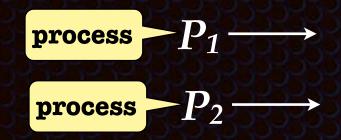


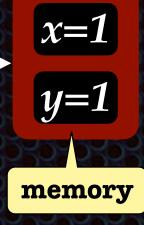






# adapting SC techniques

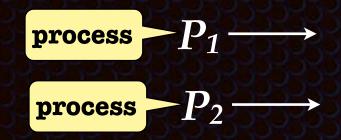


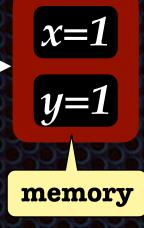




semantics decidability

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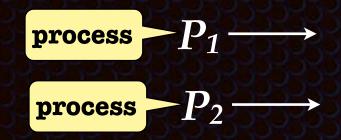


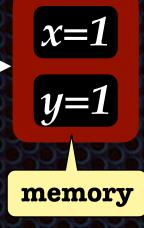


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# adapting SC techniques





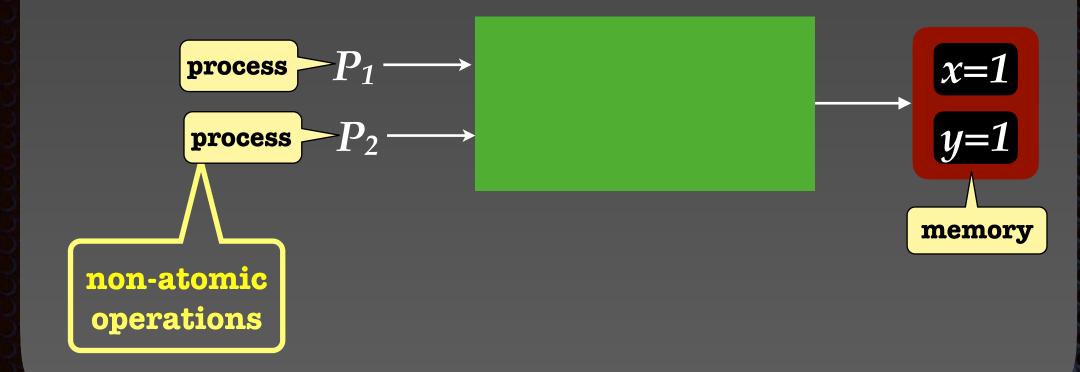


semantics decidability



# adapting SC techniques





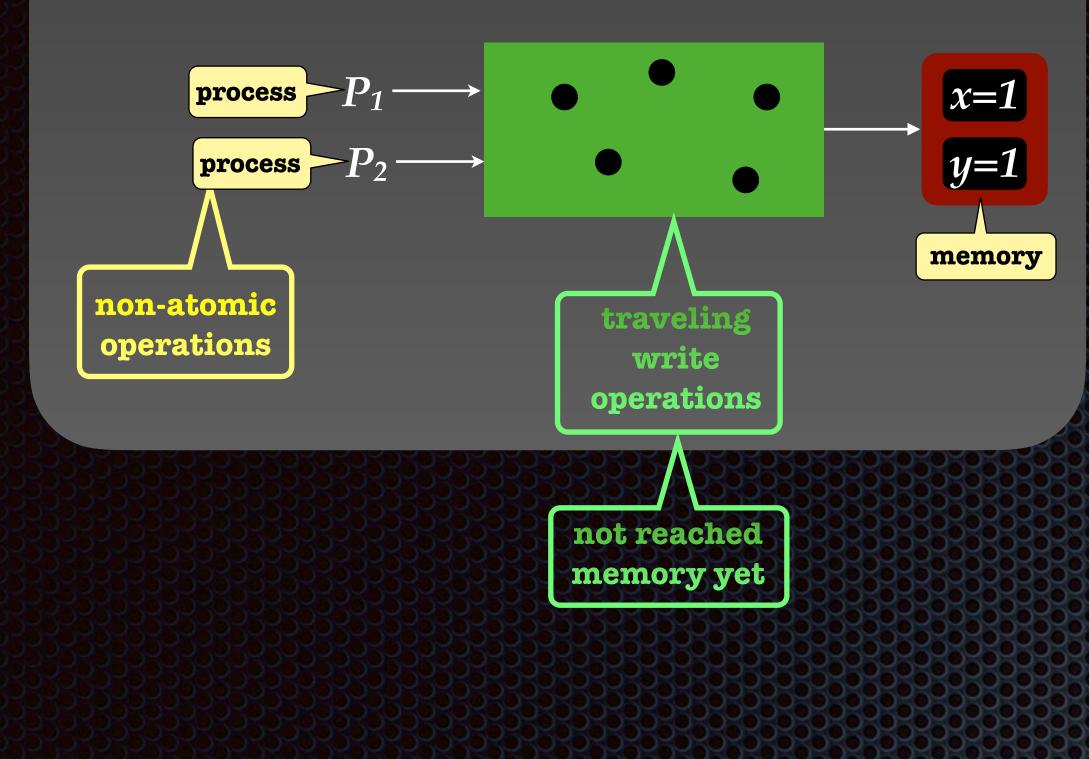


semantics decidability



# adapting SC techniques





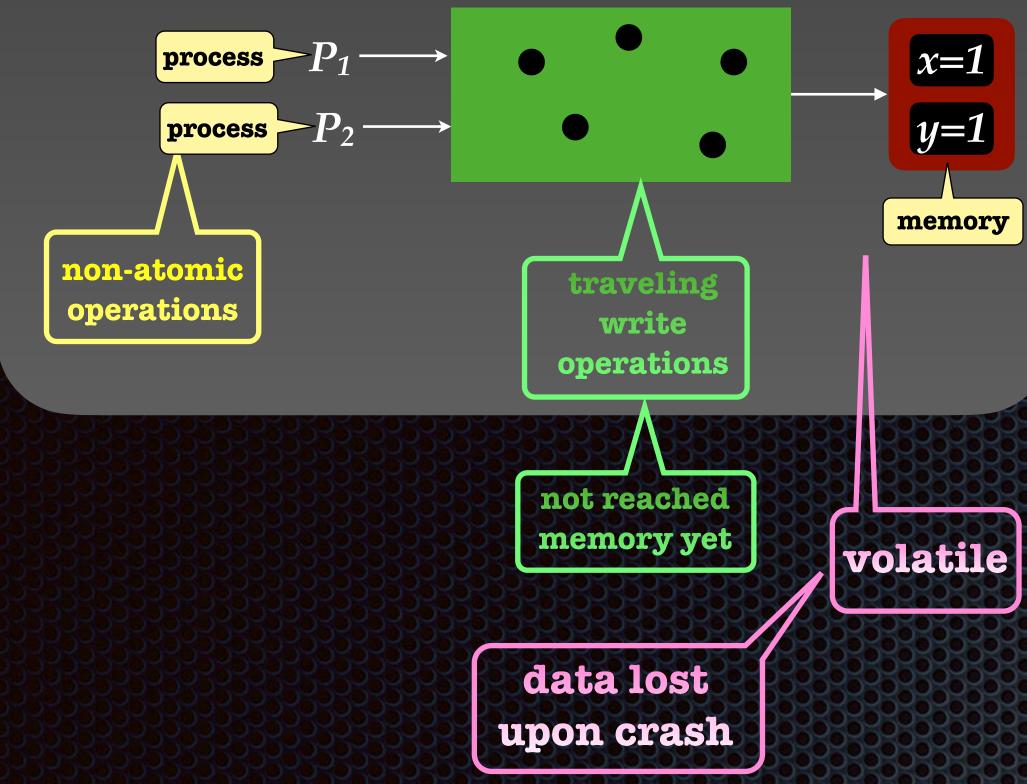


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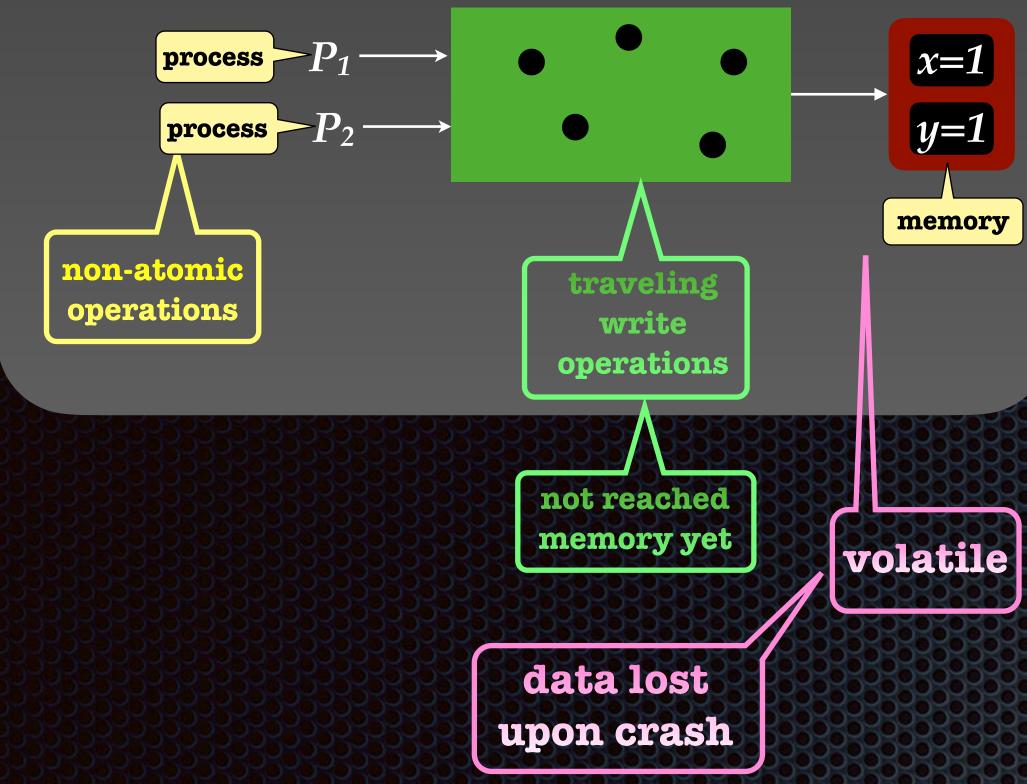


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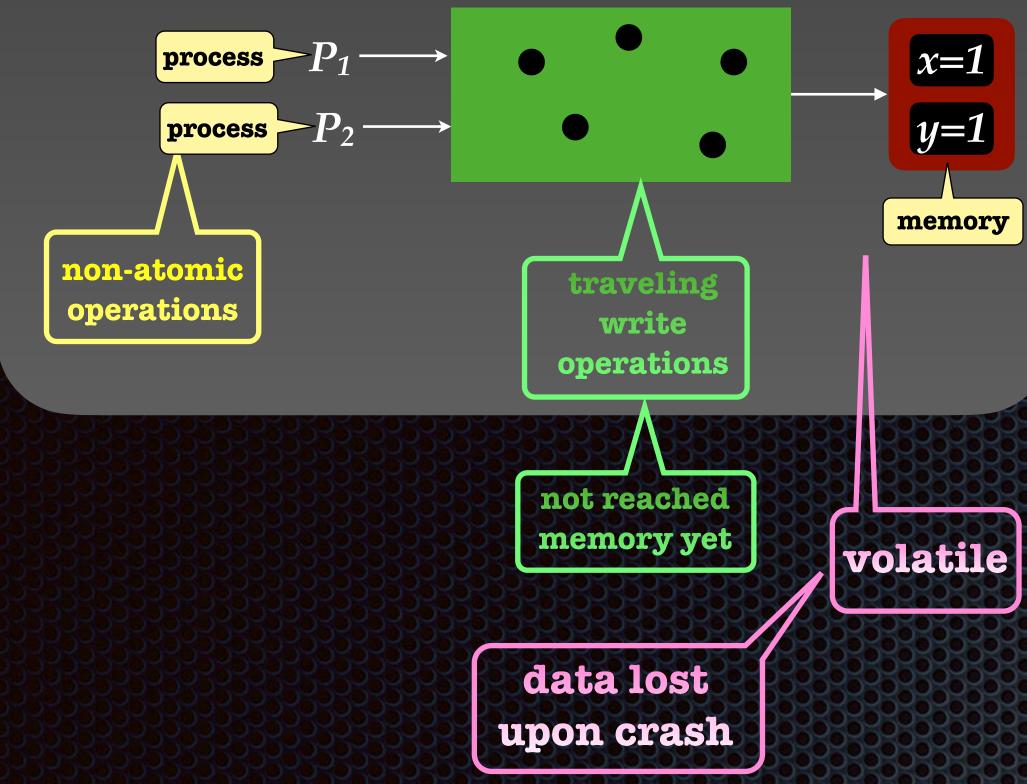


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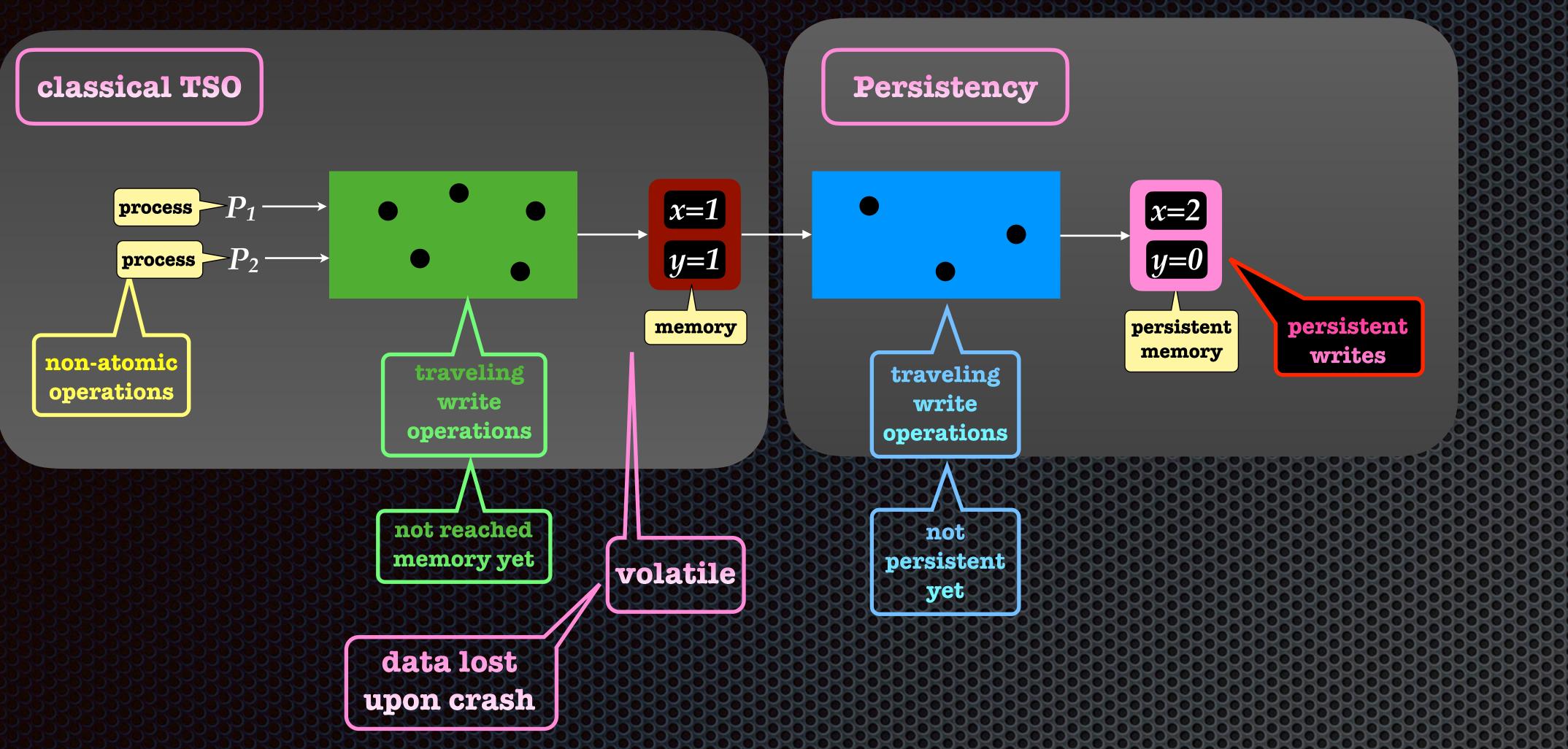


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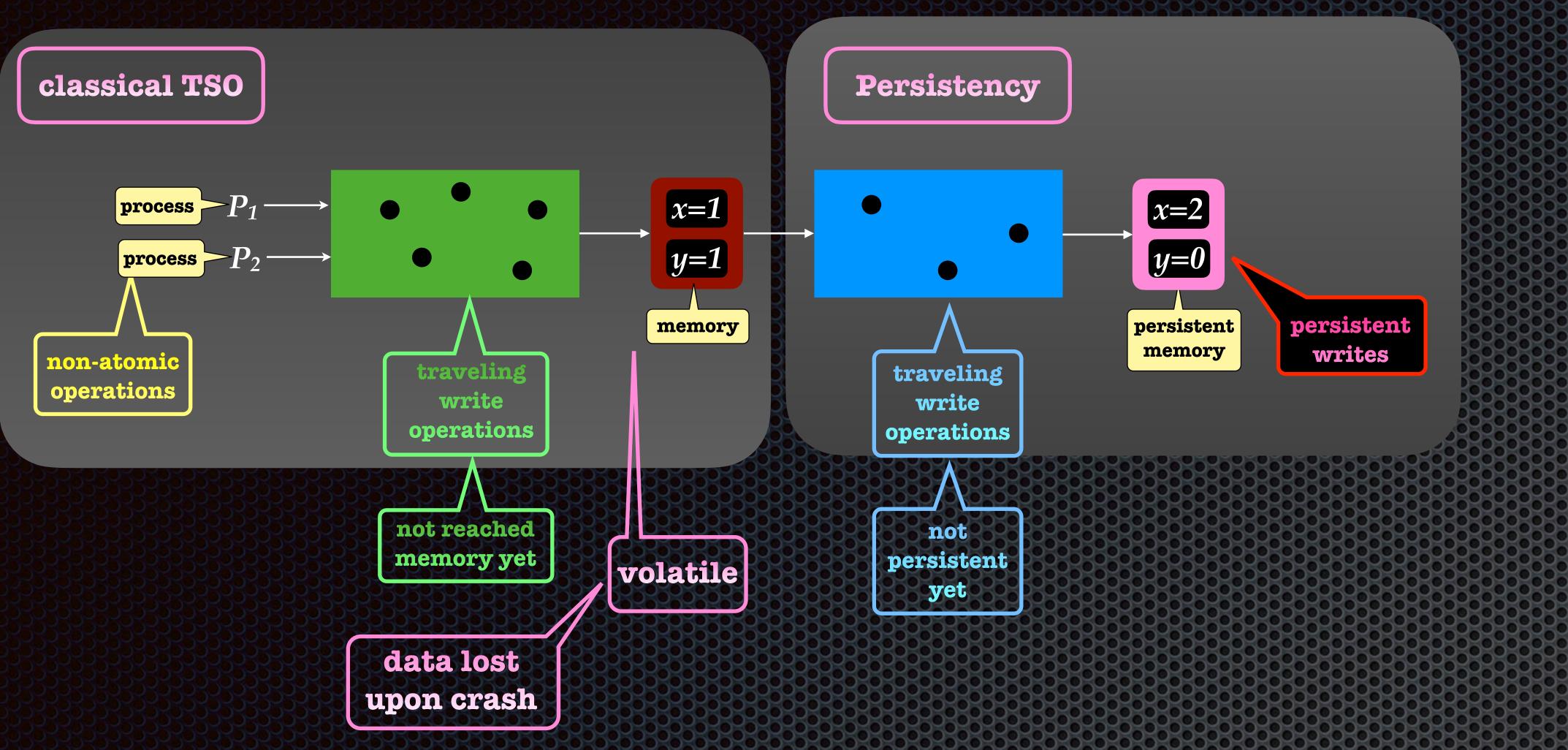






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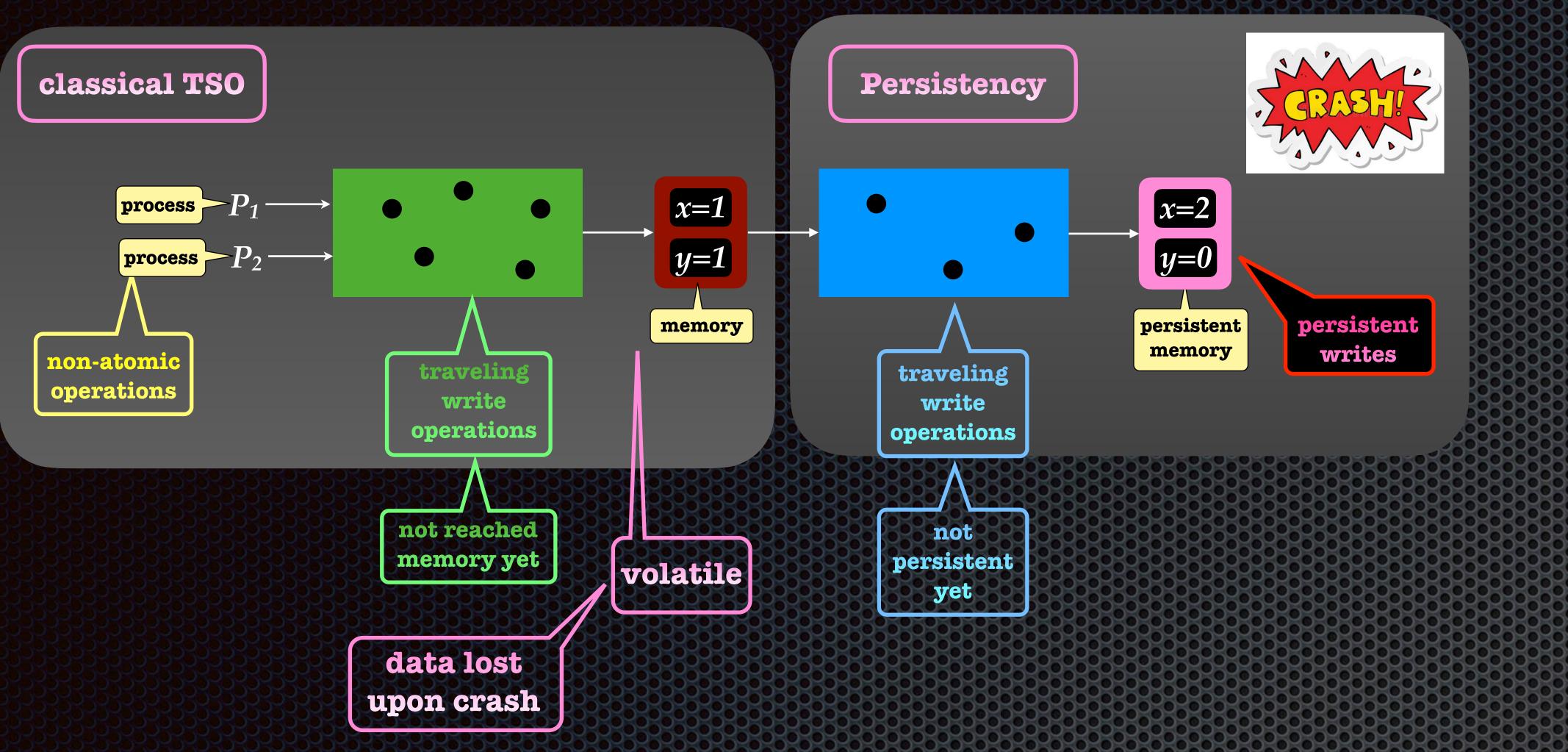






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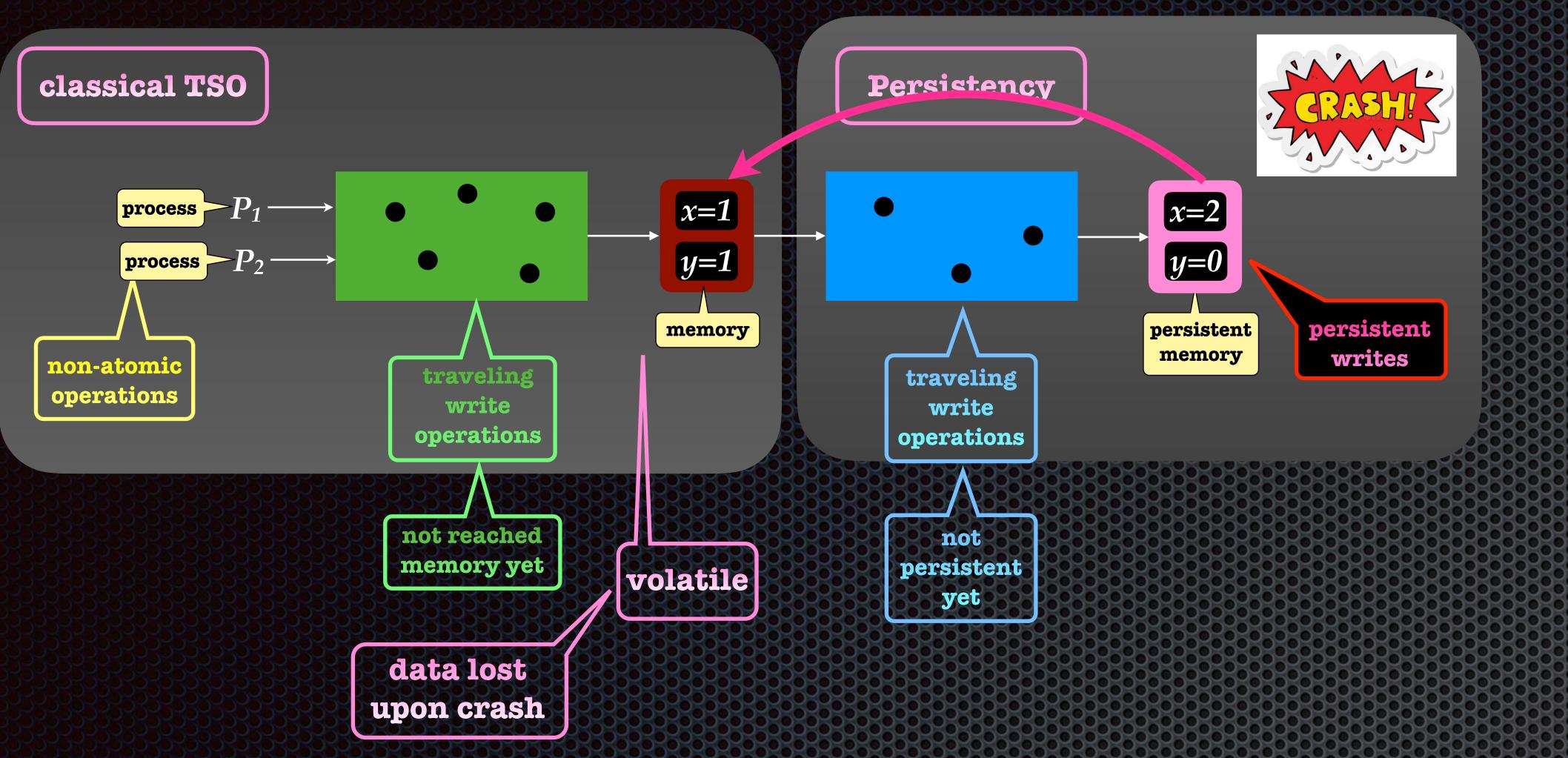






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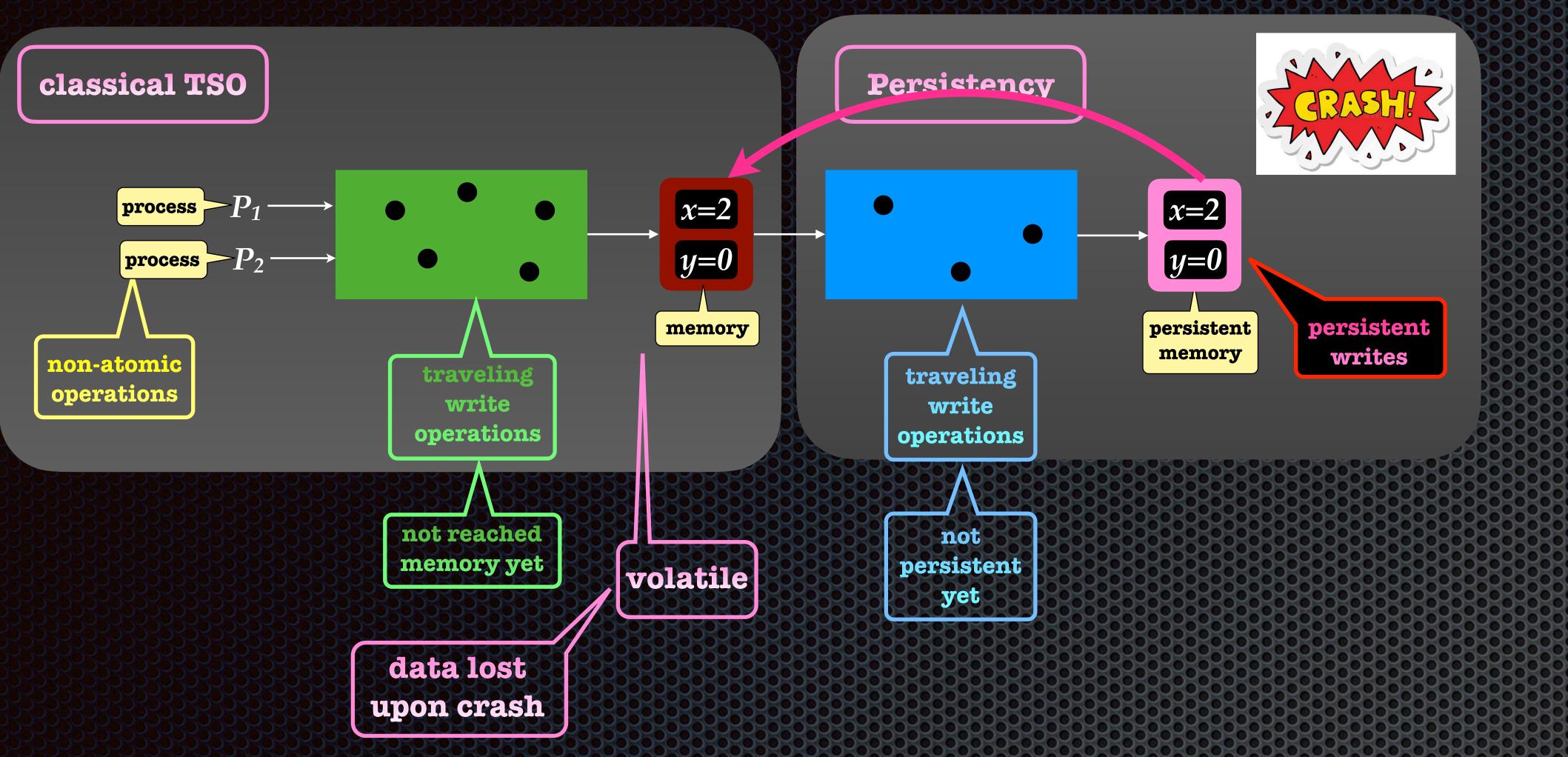






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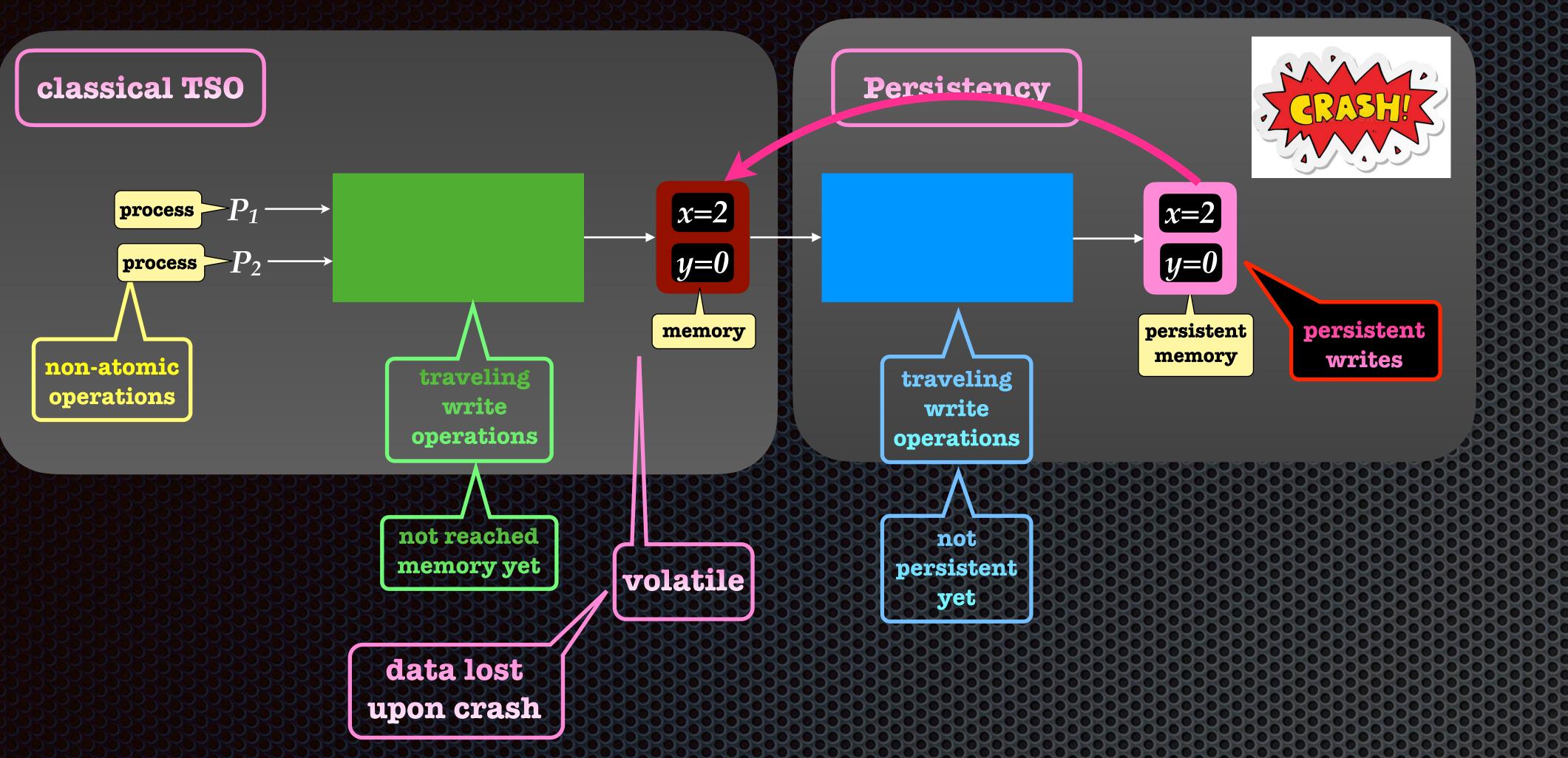






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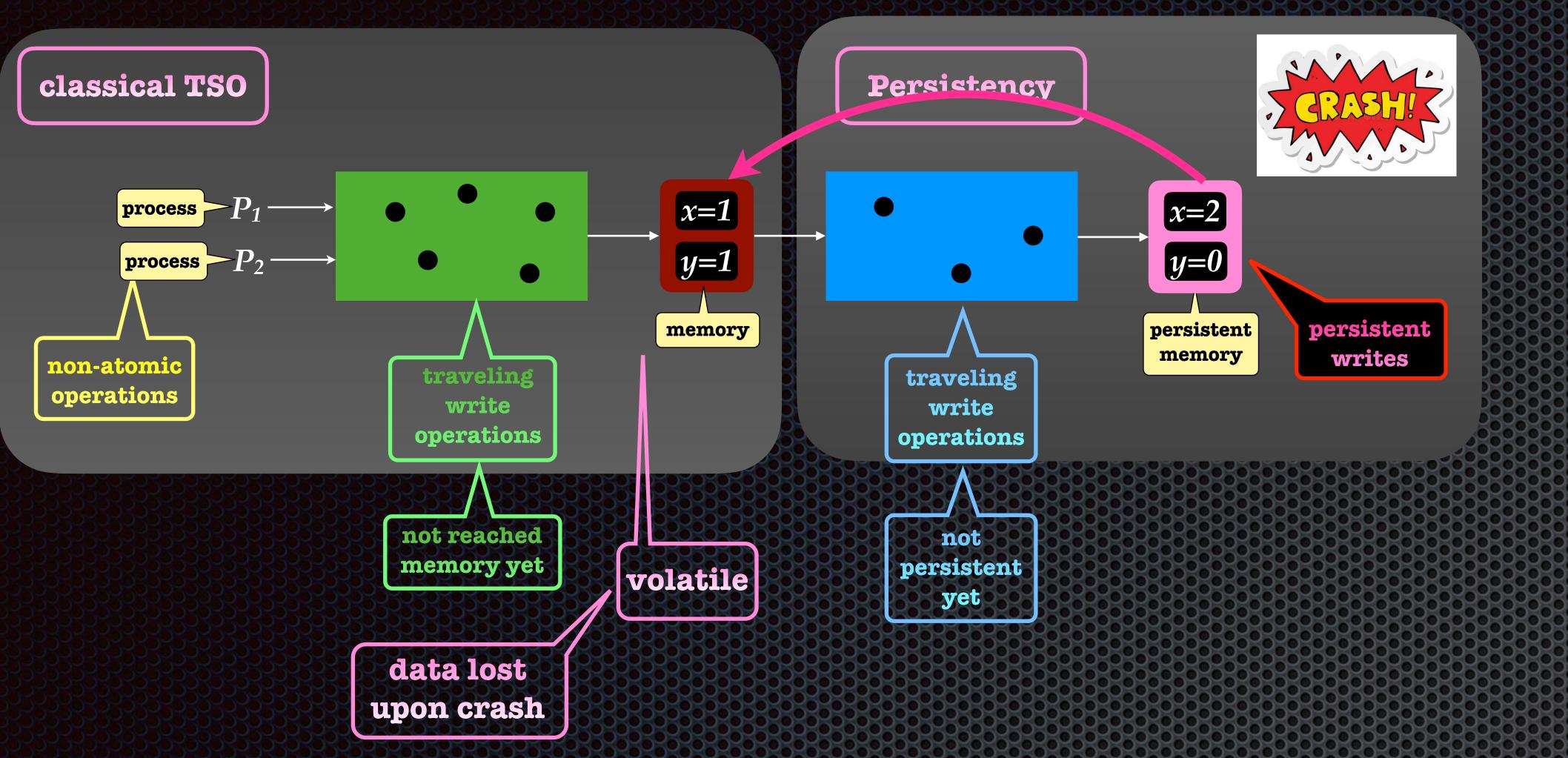






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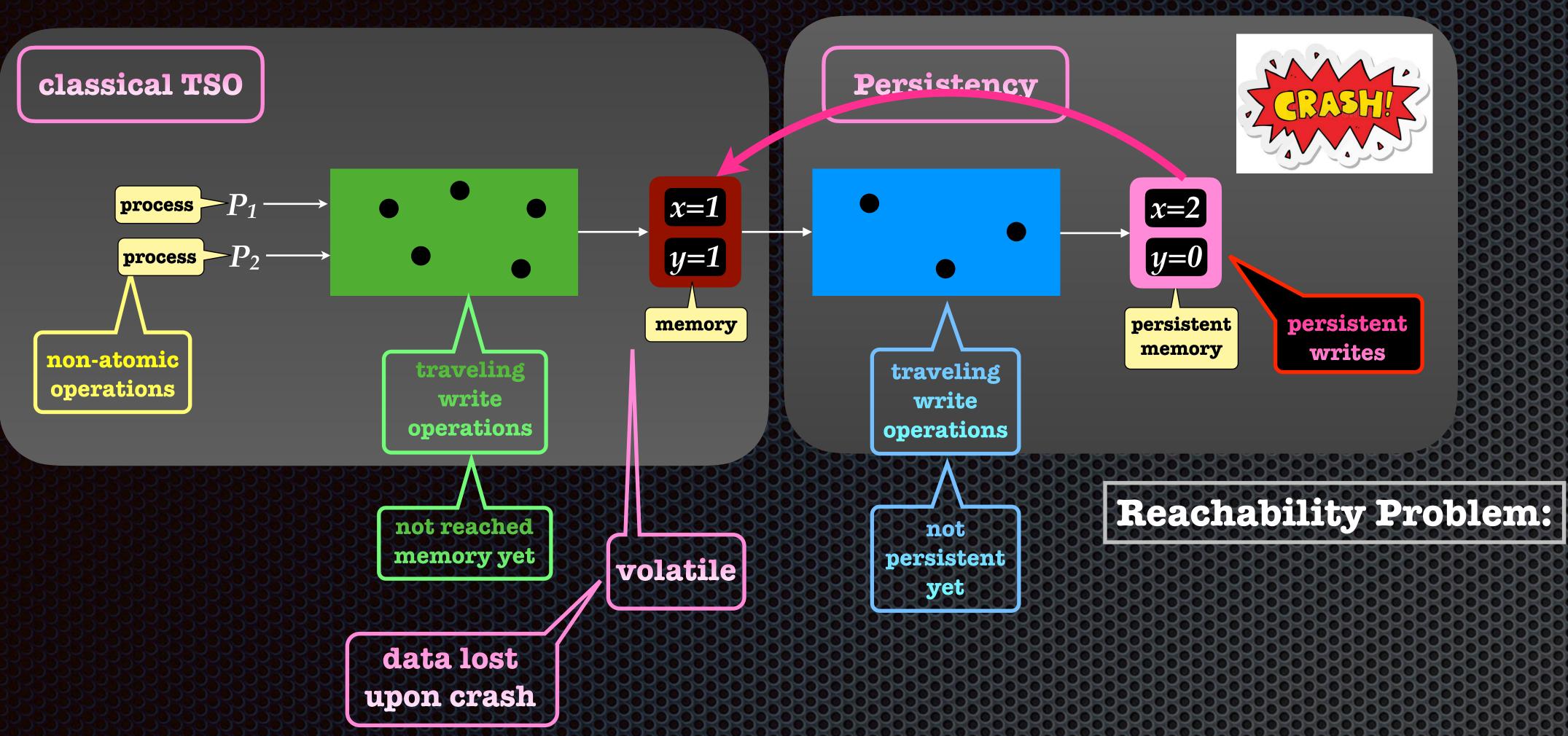






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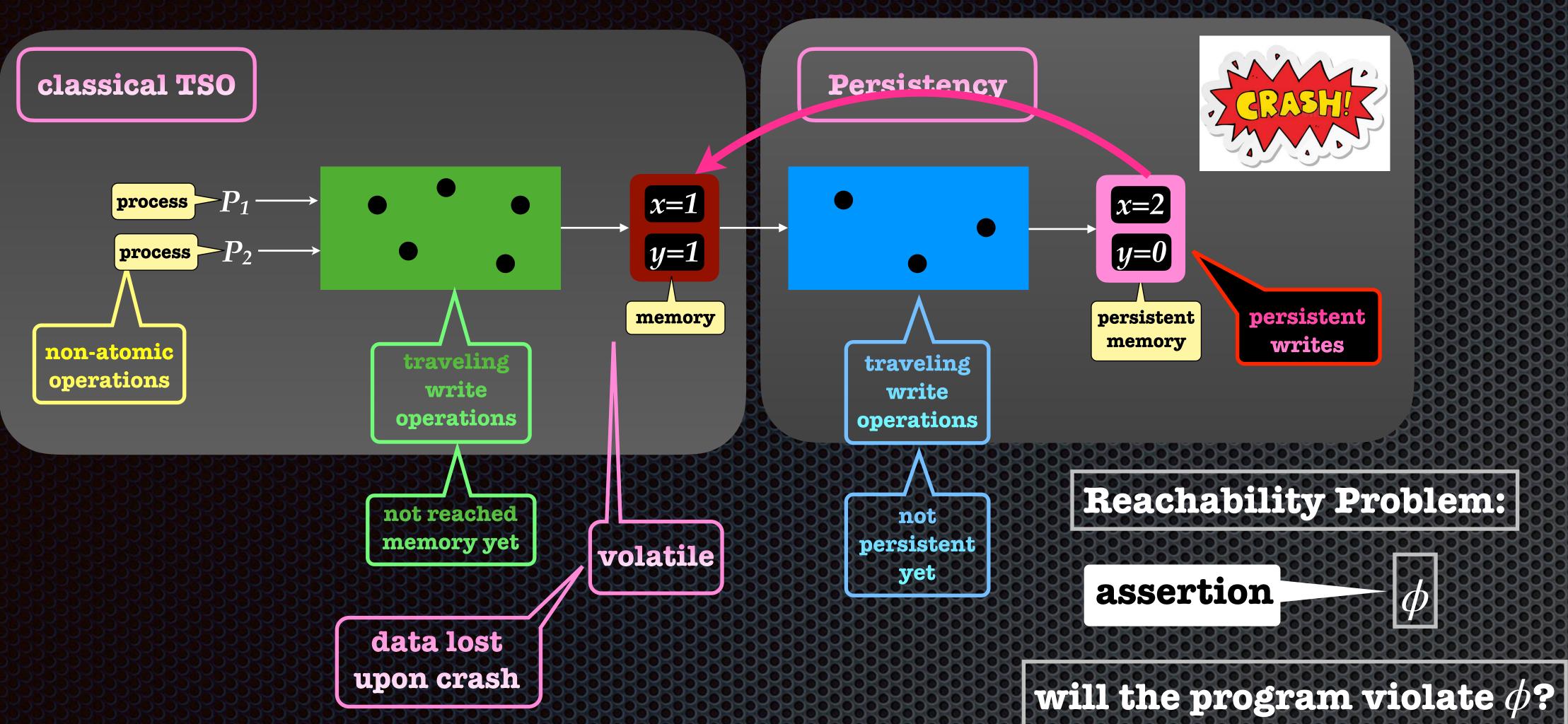






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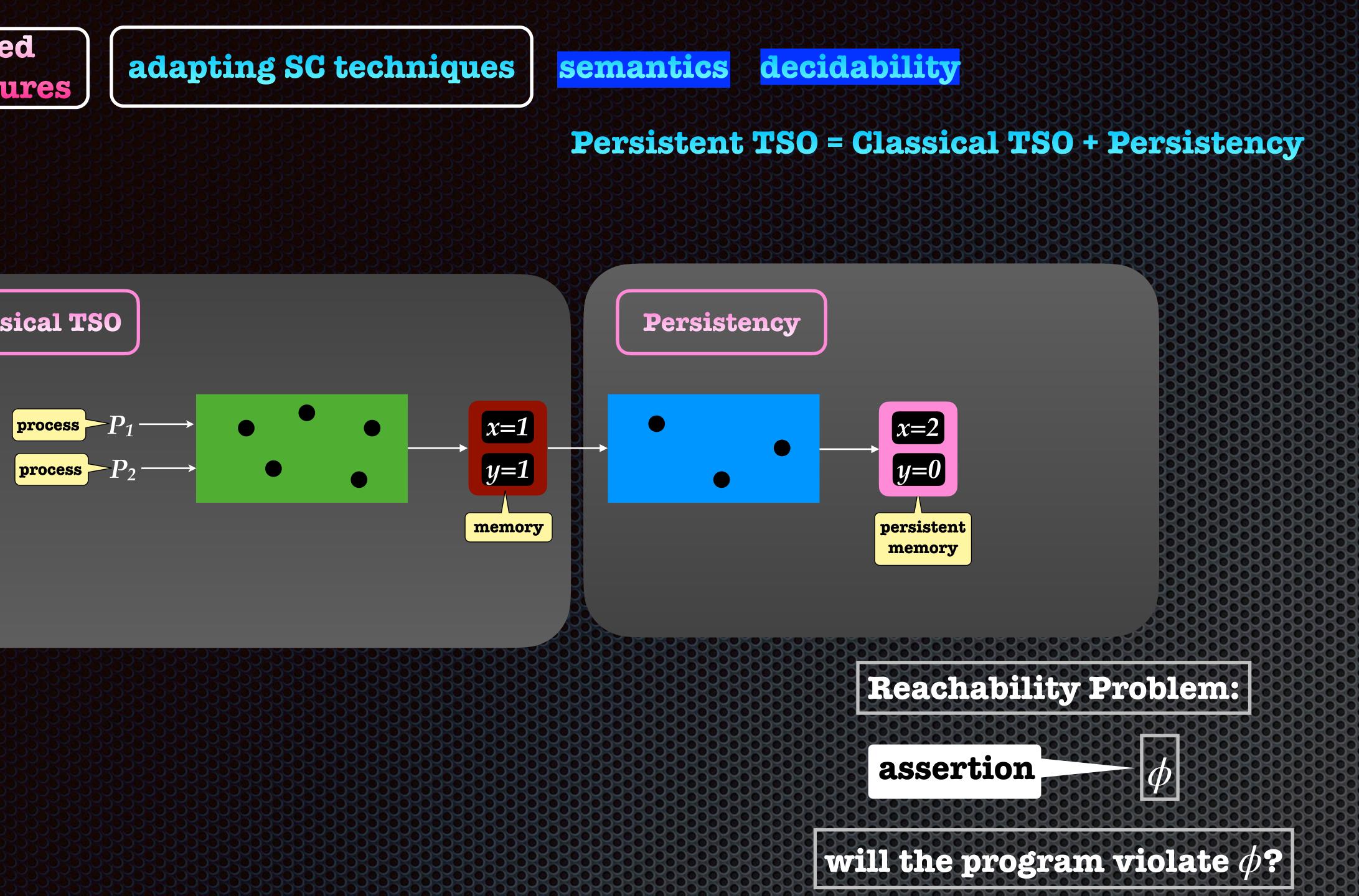


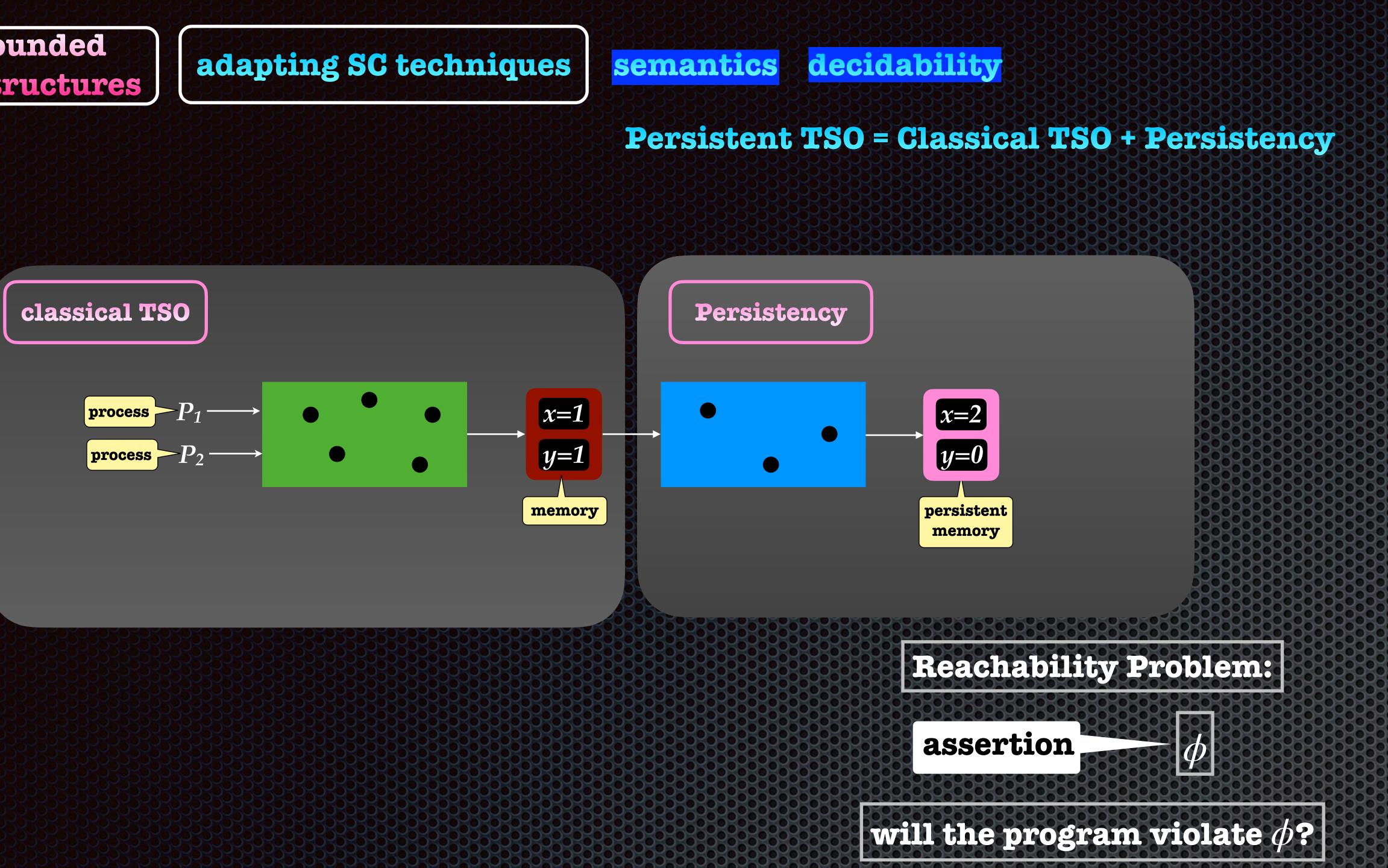






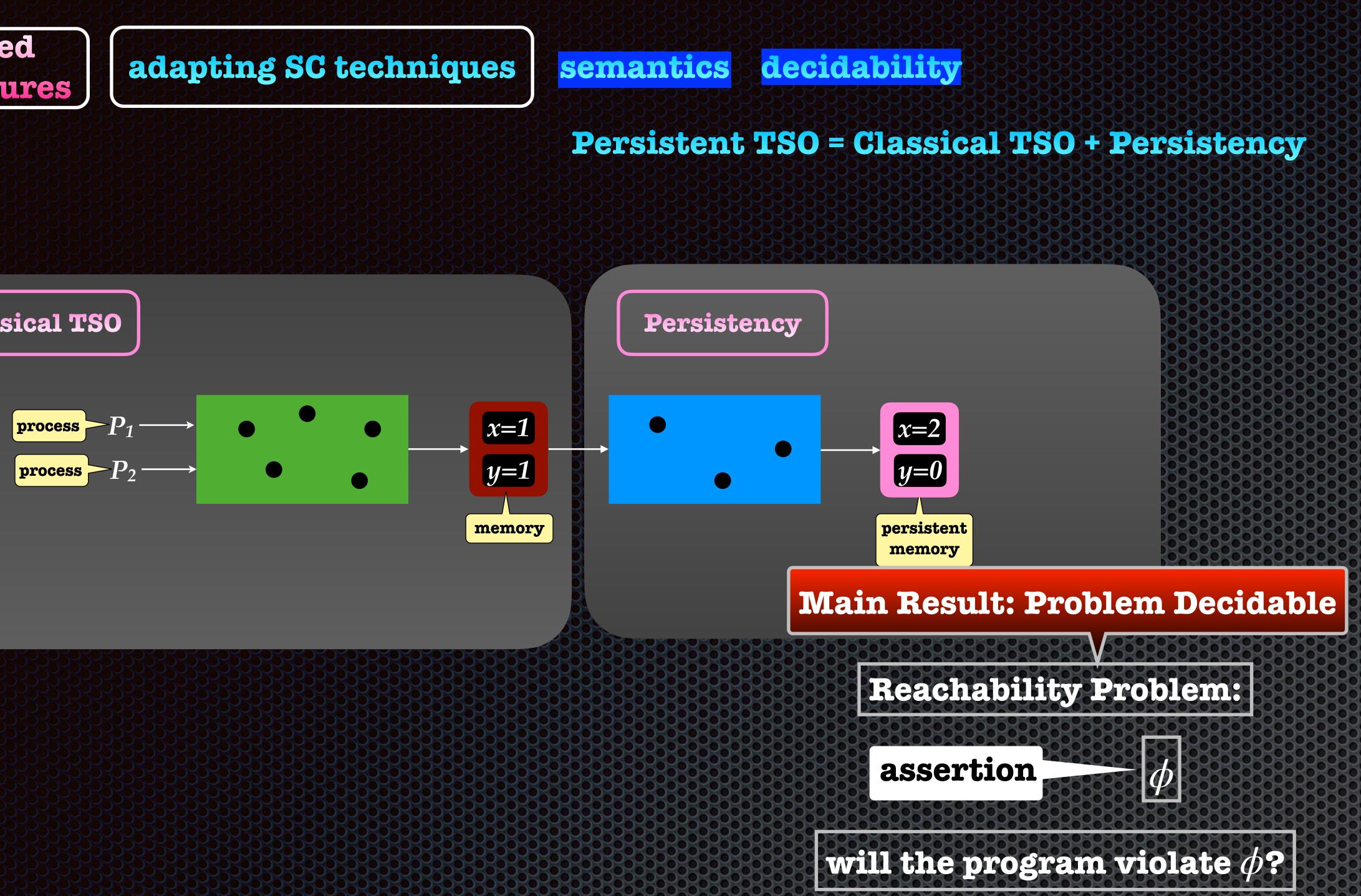


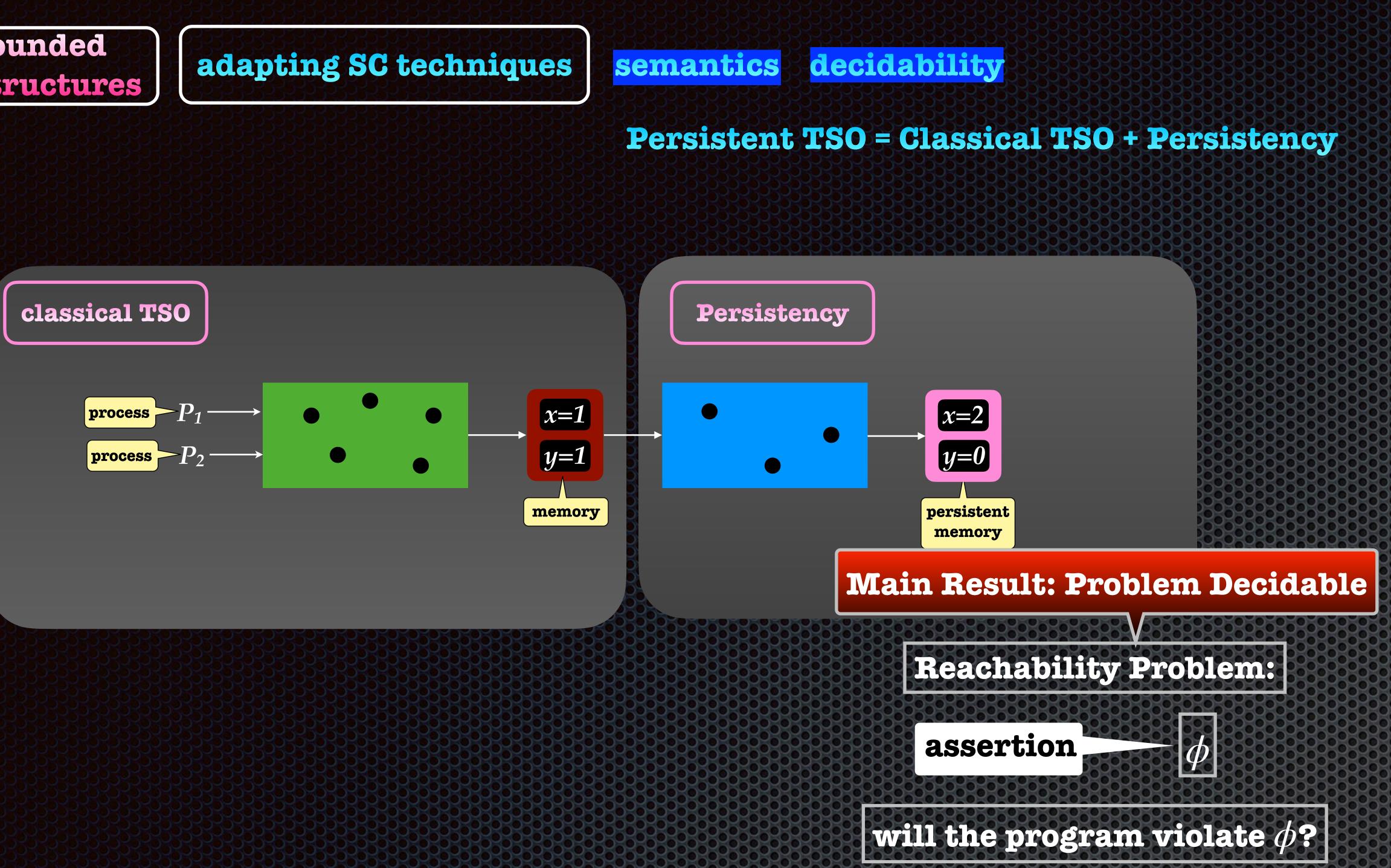






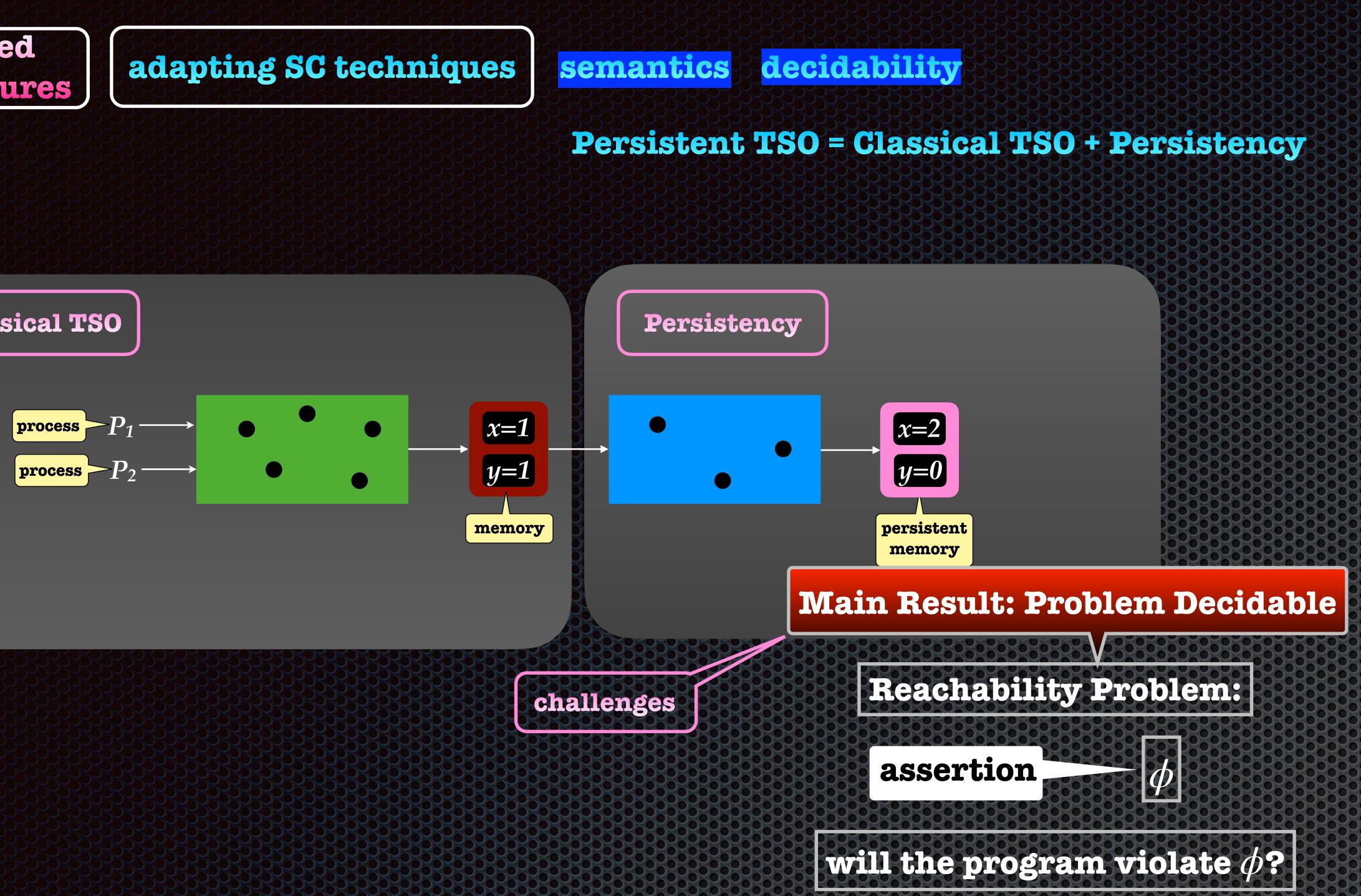


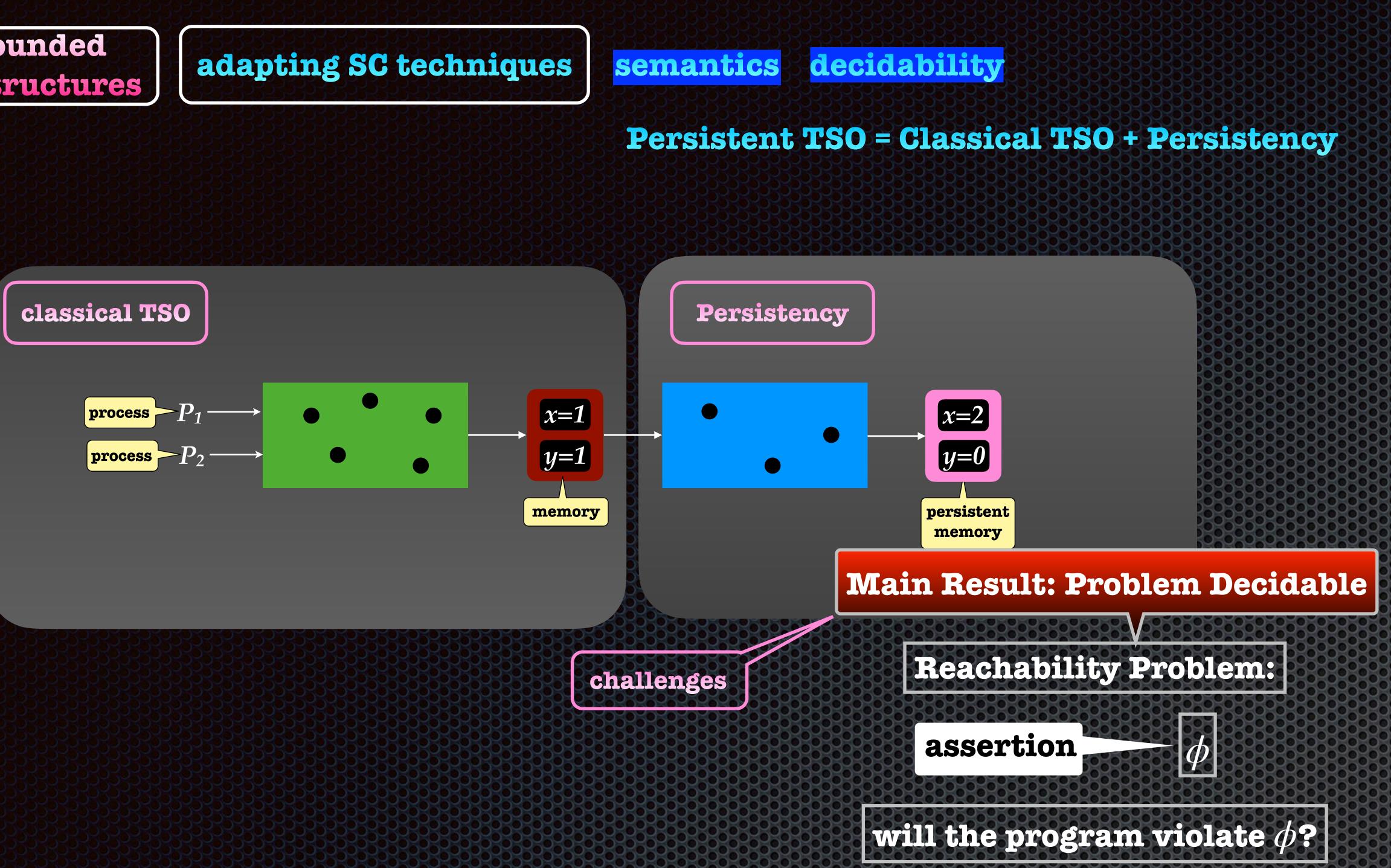






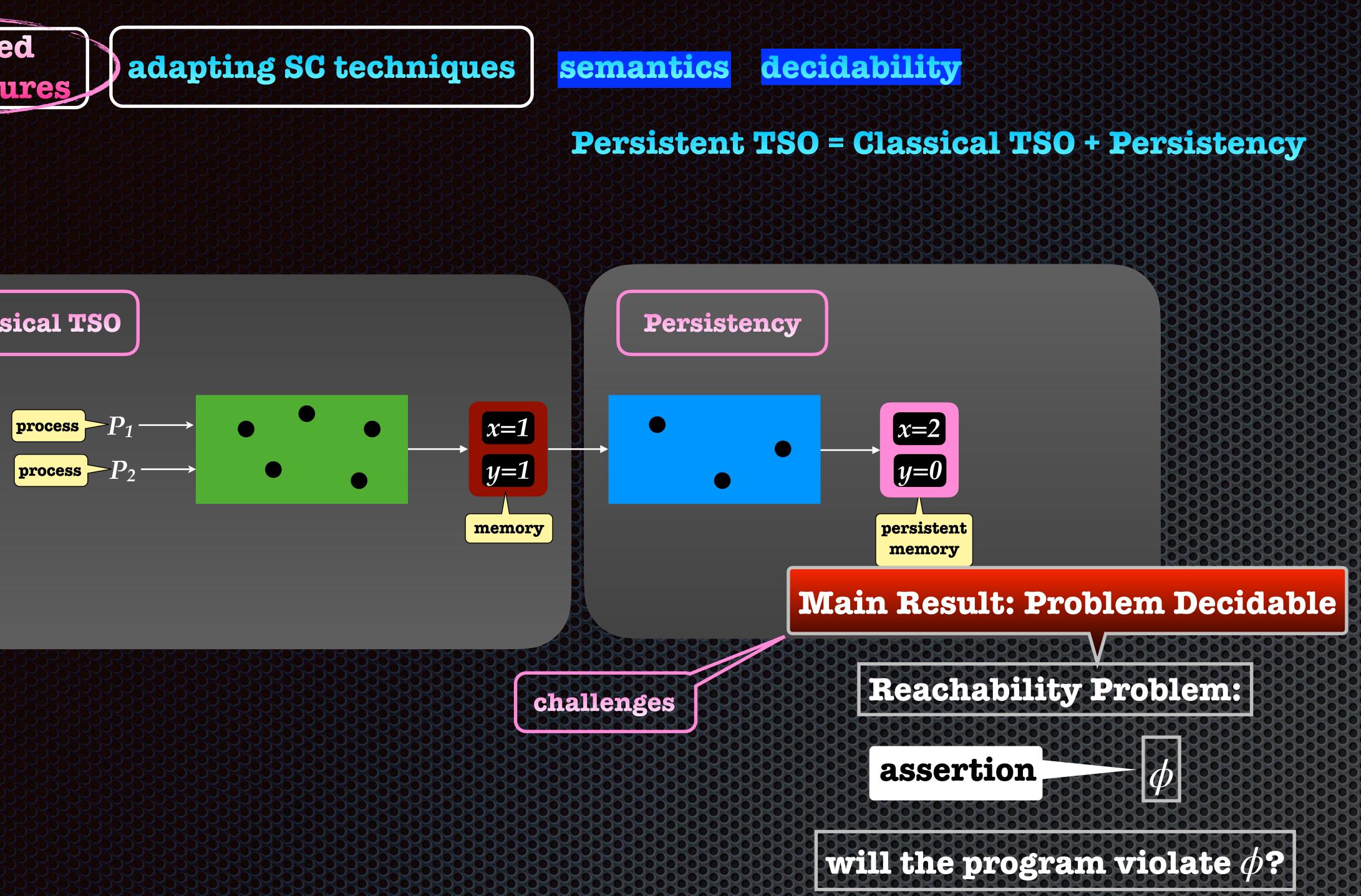






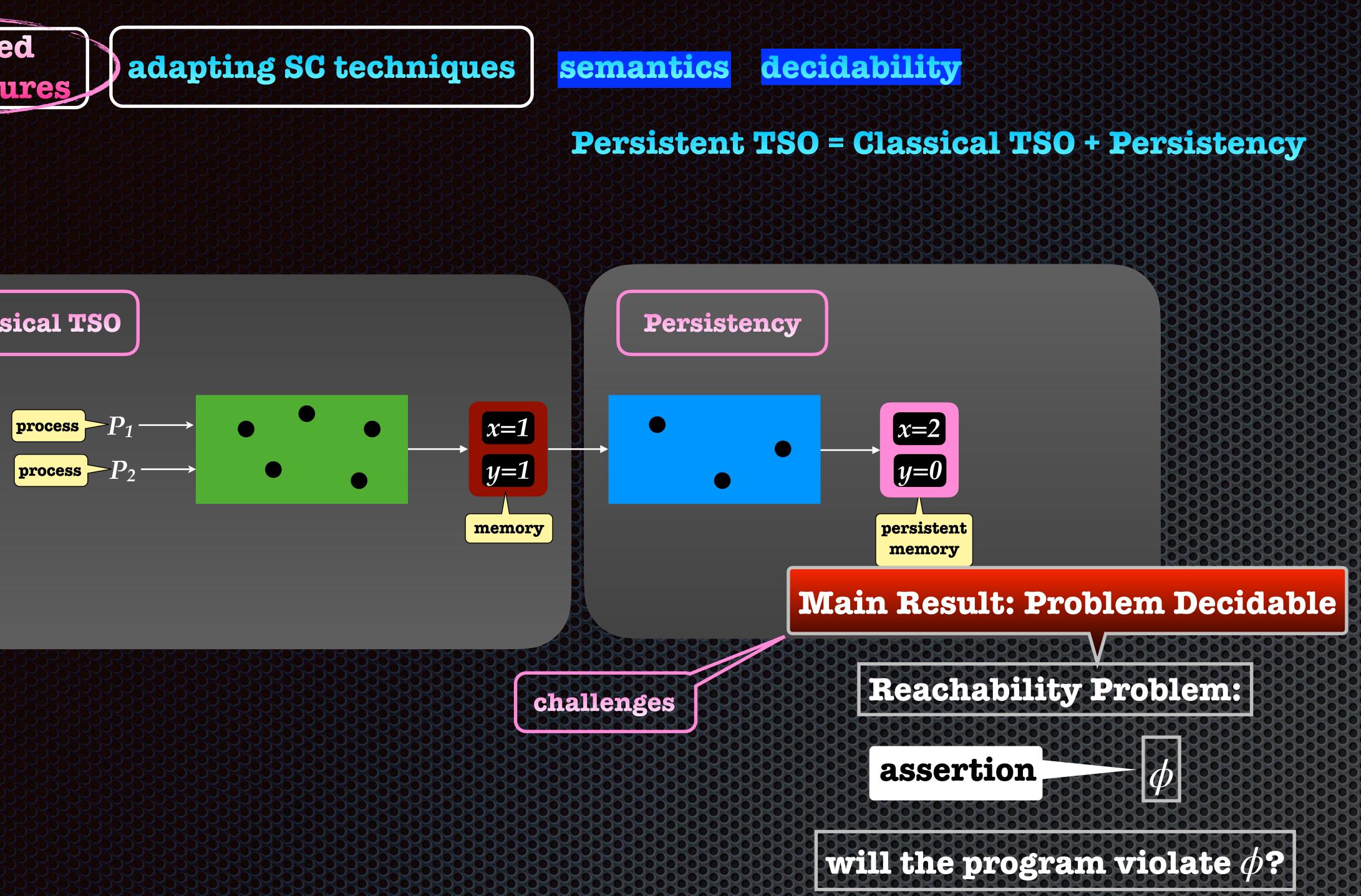






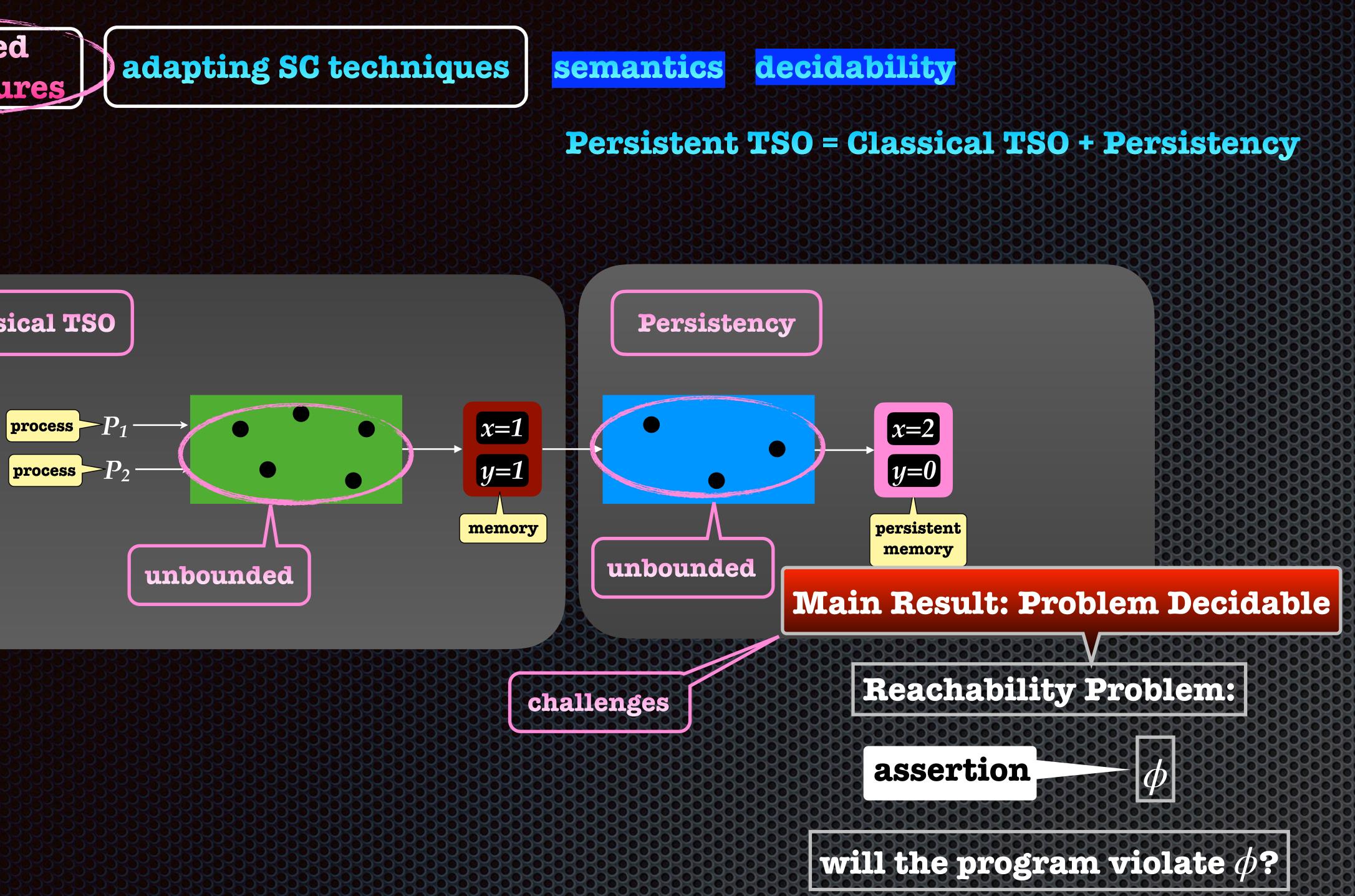


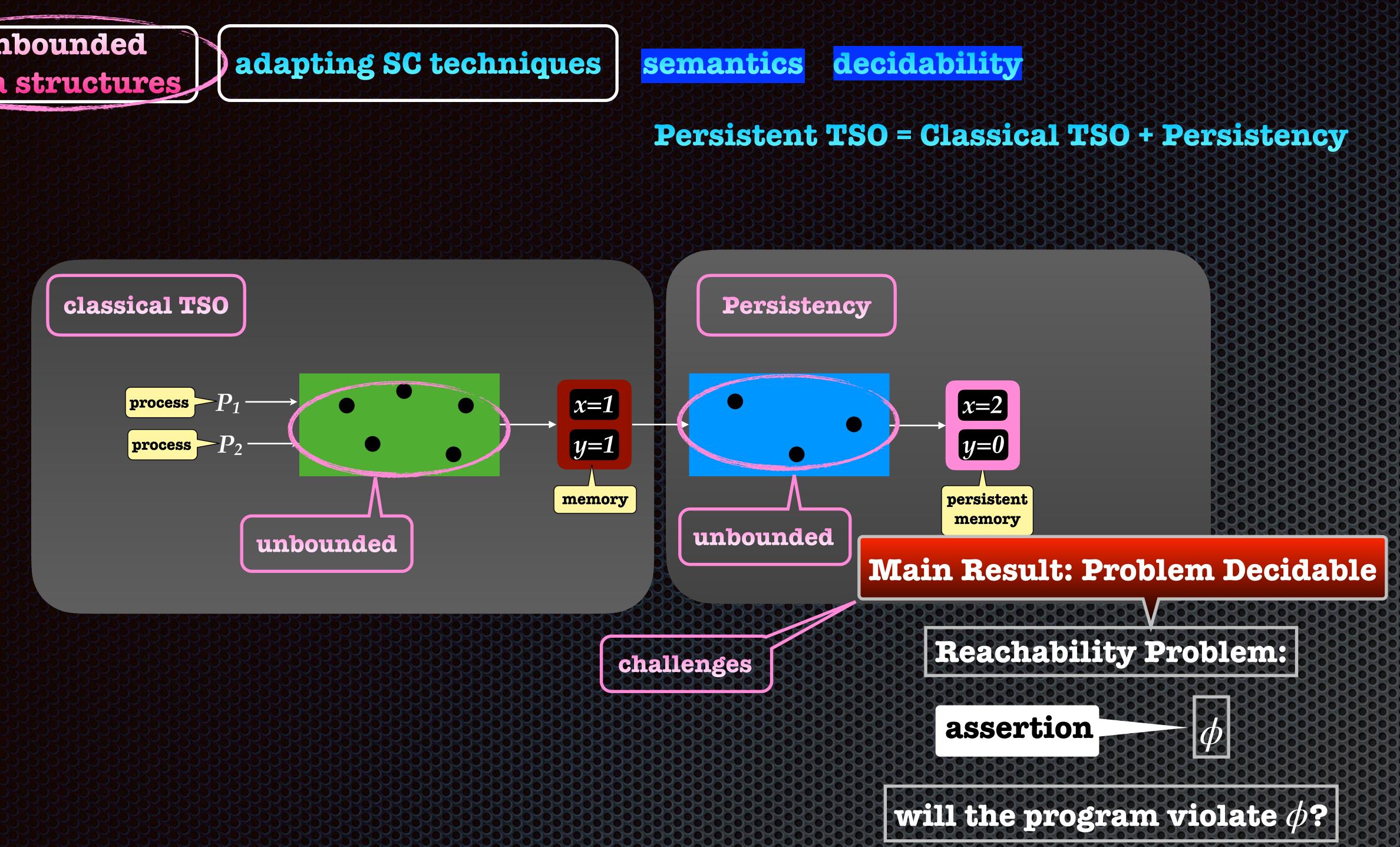






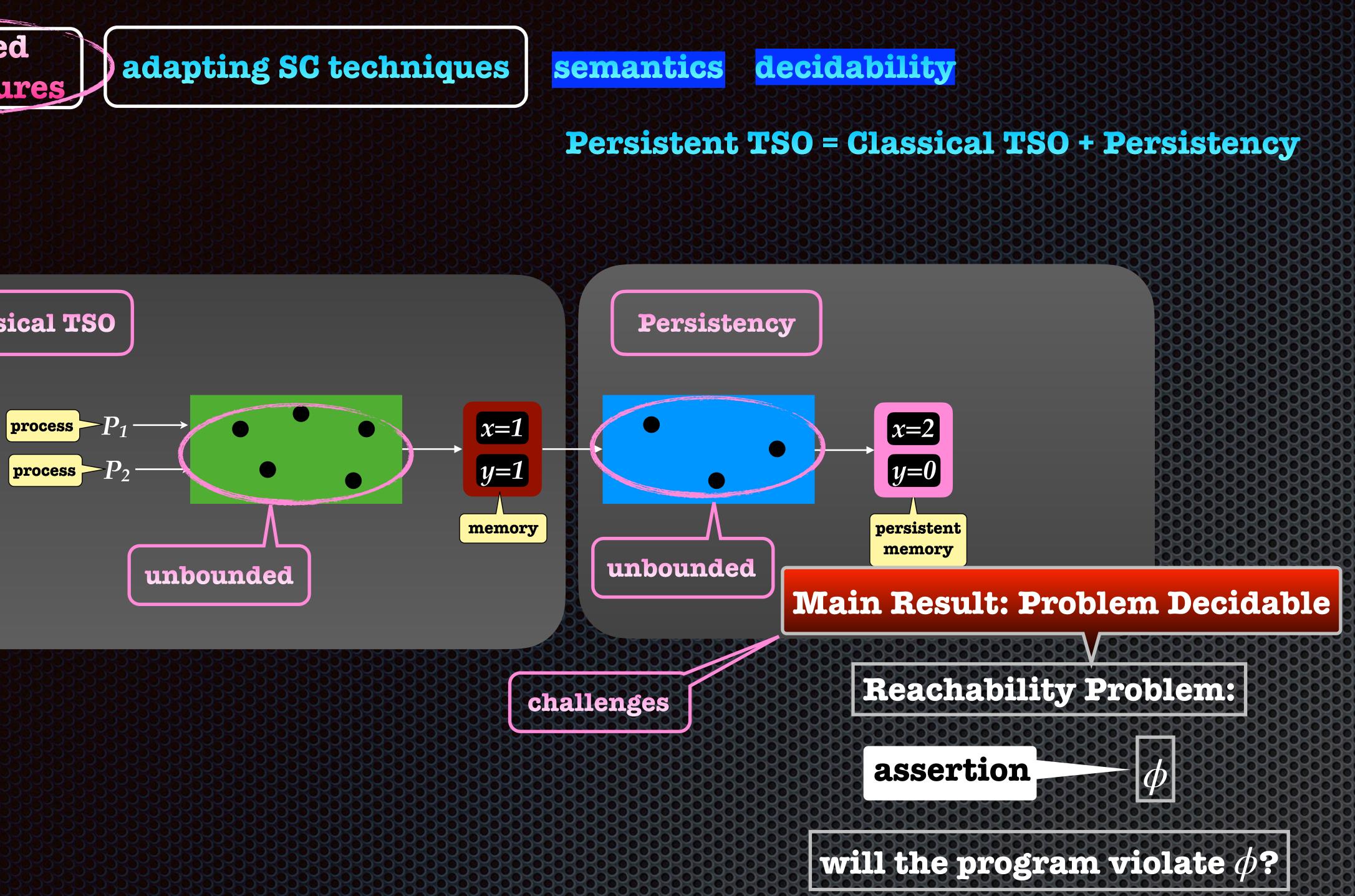


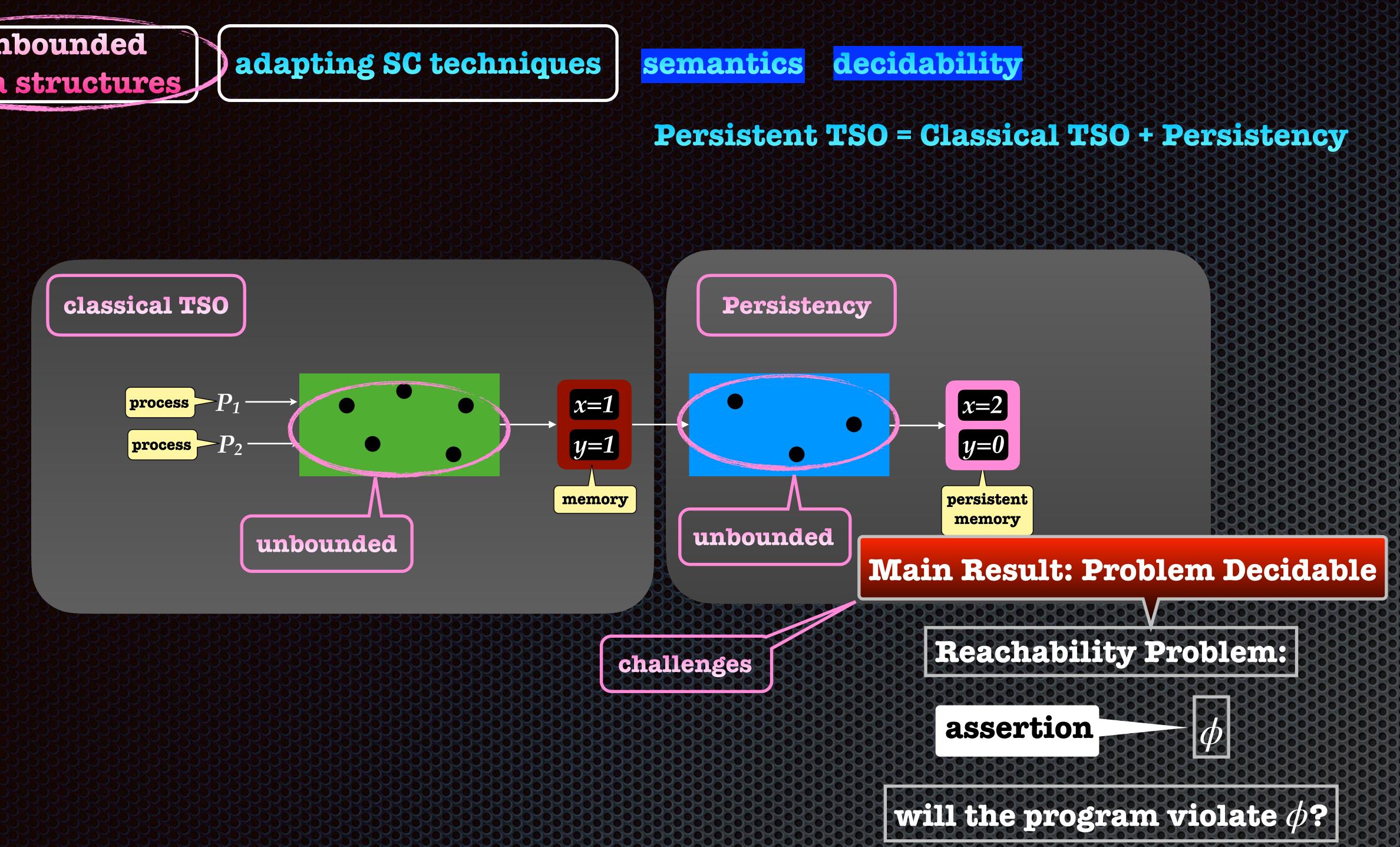






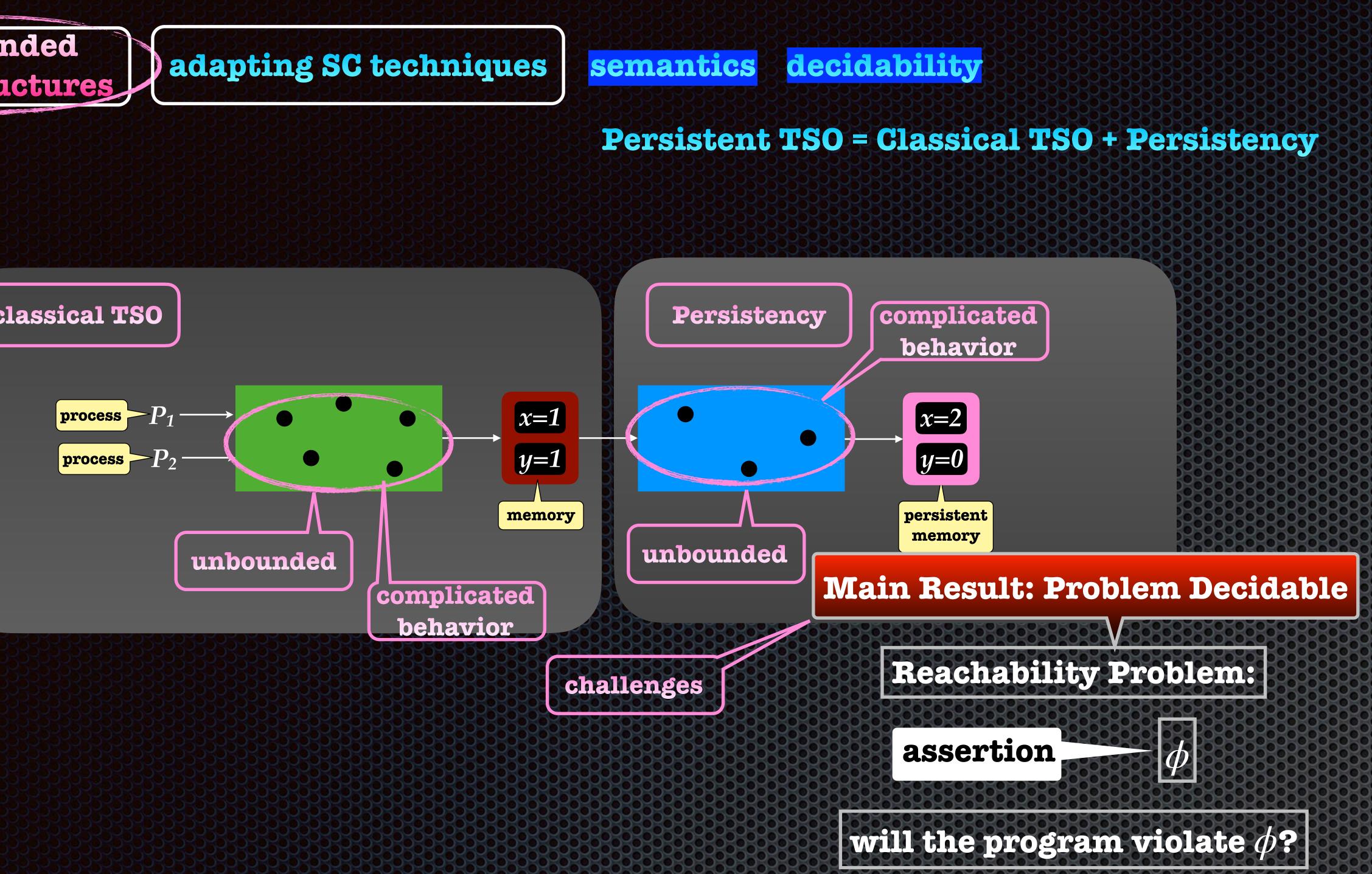






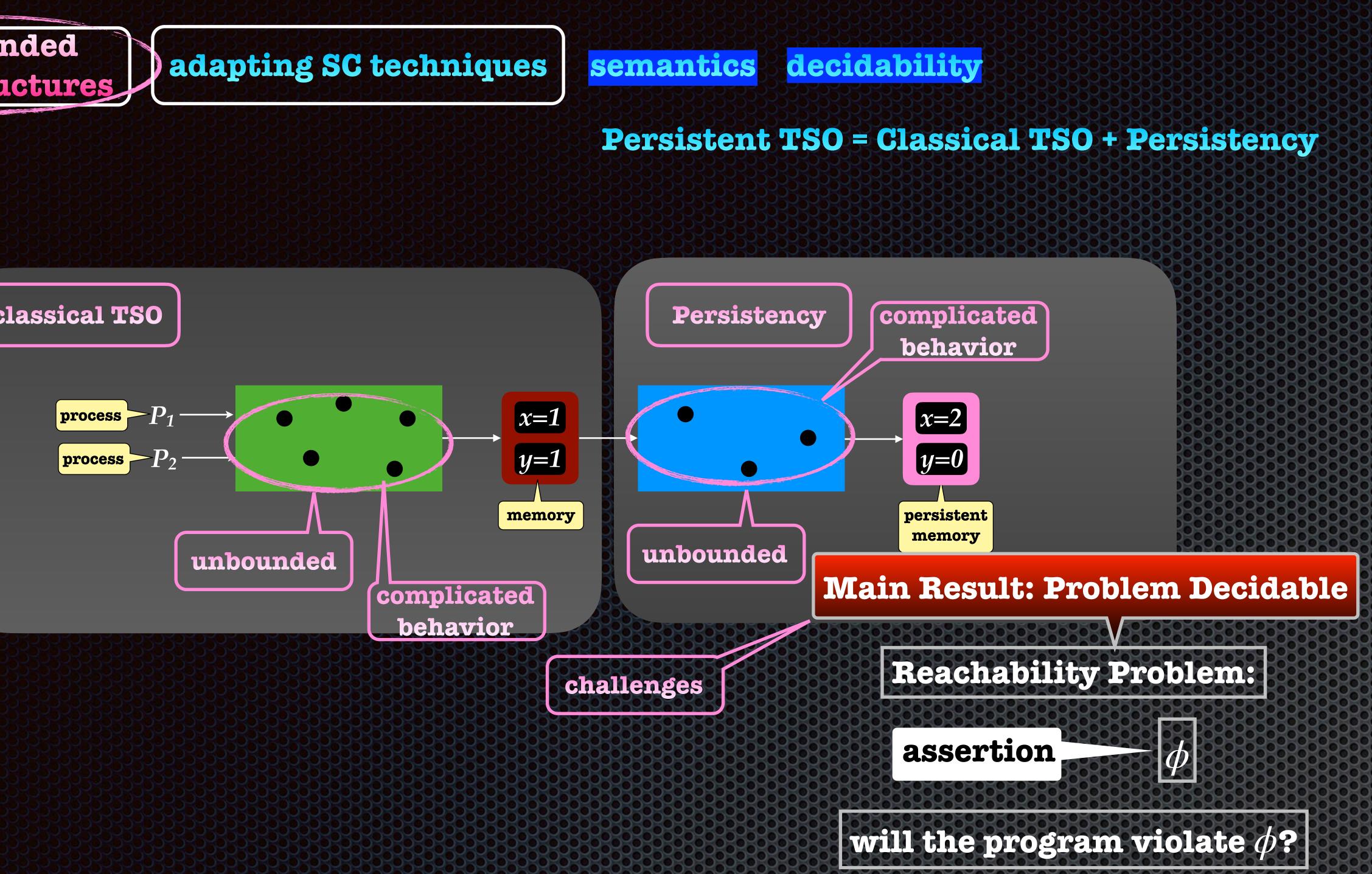




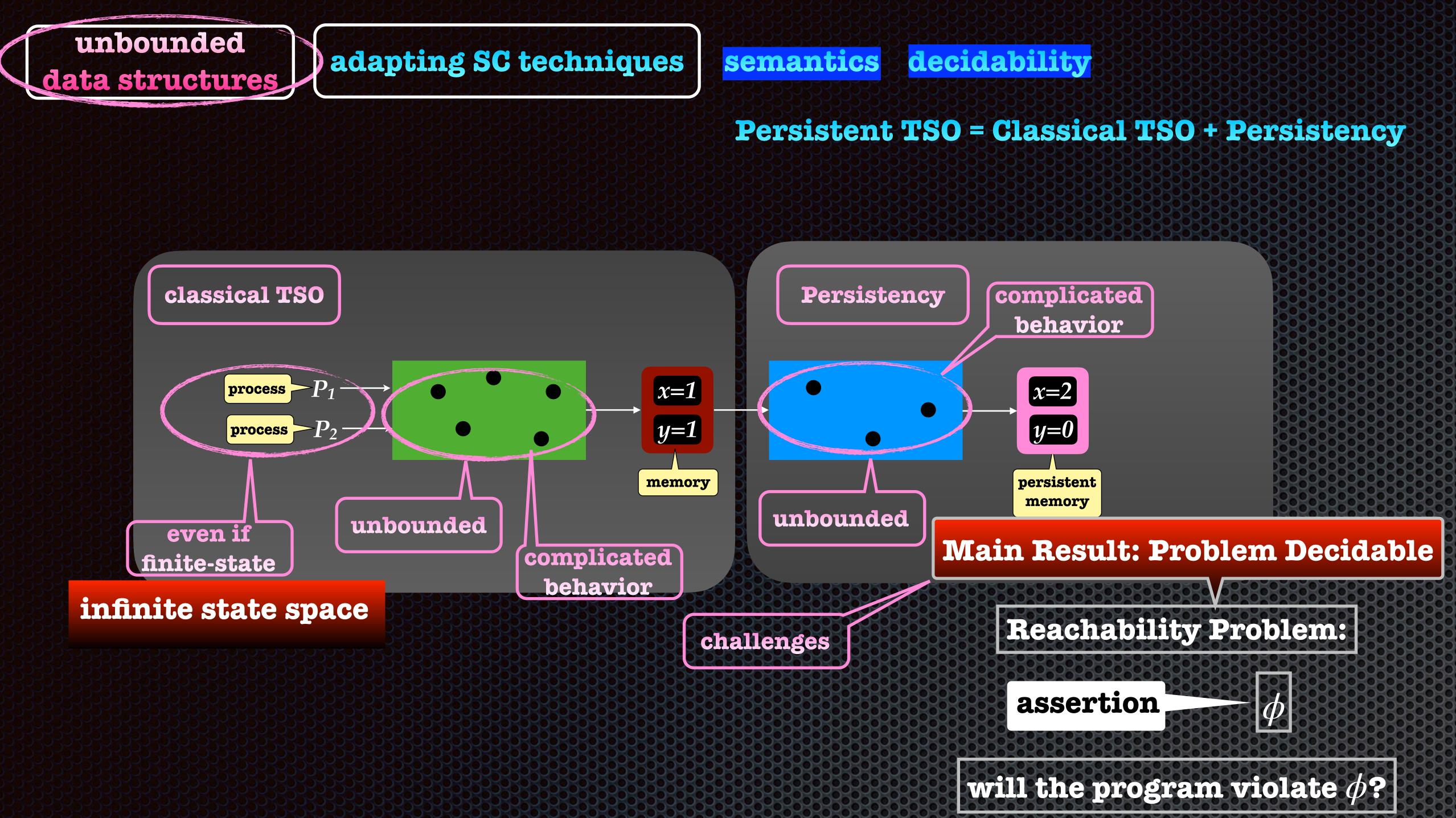








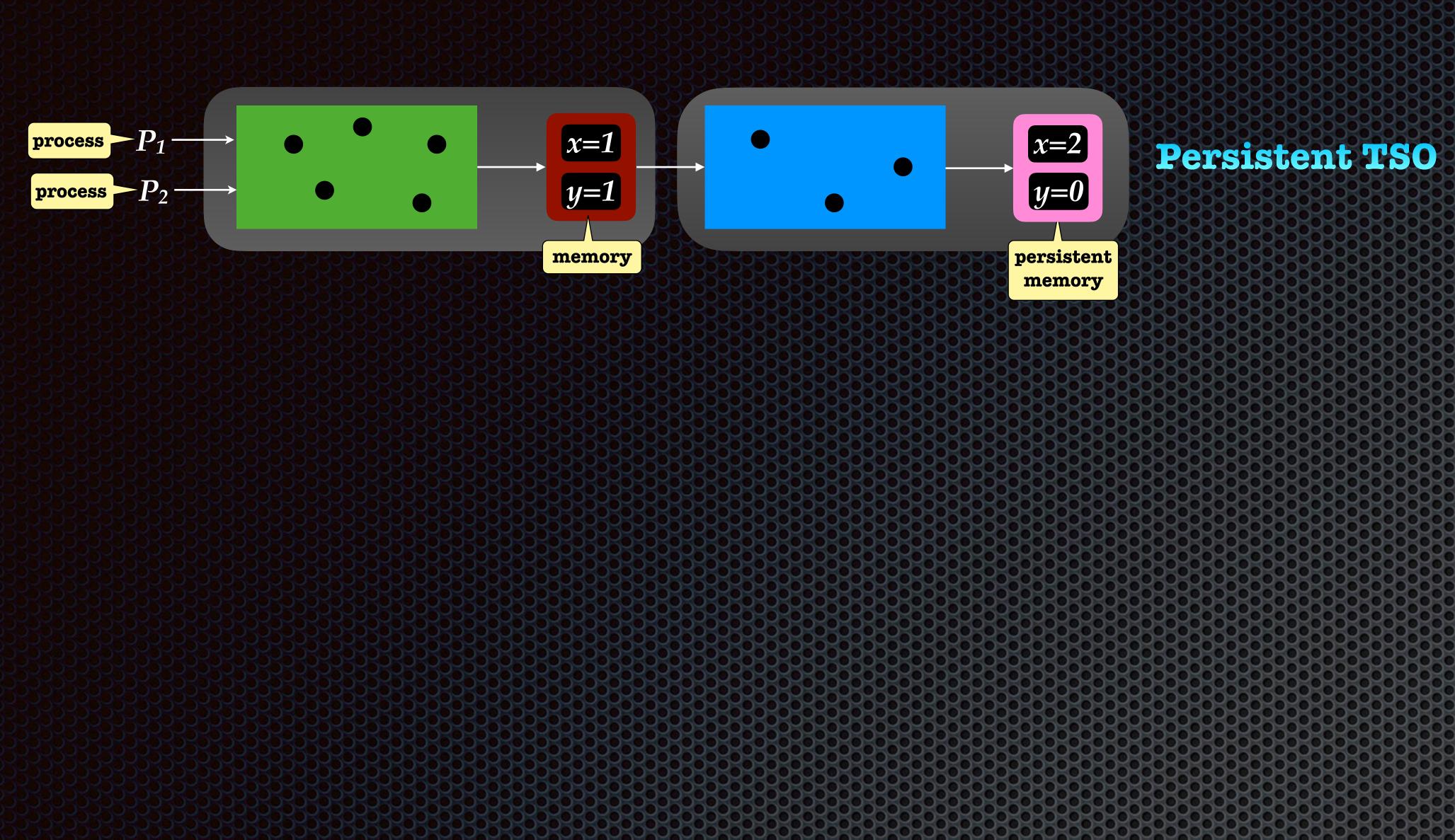






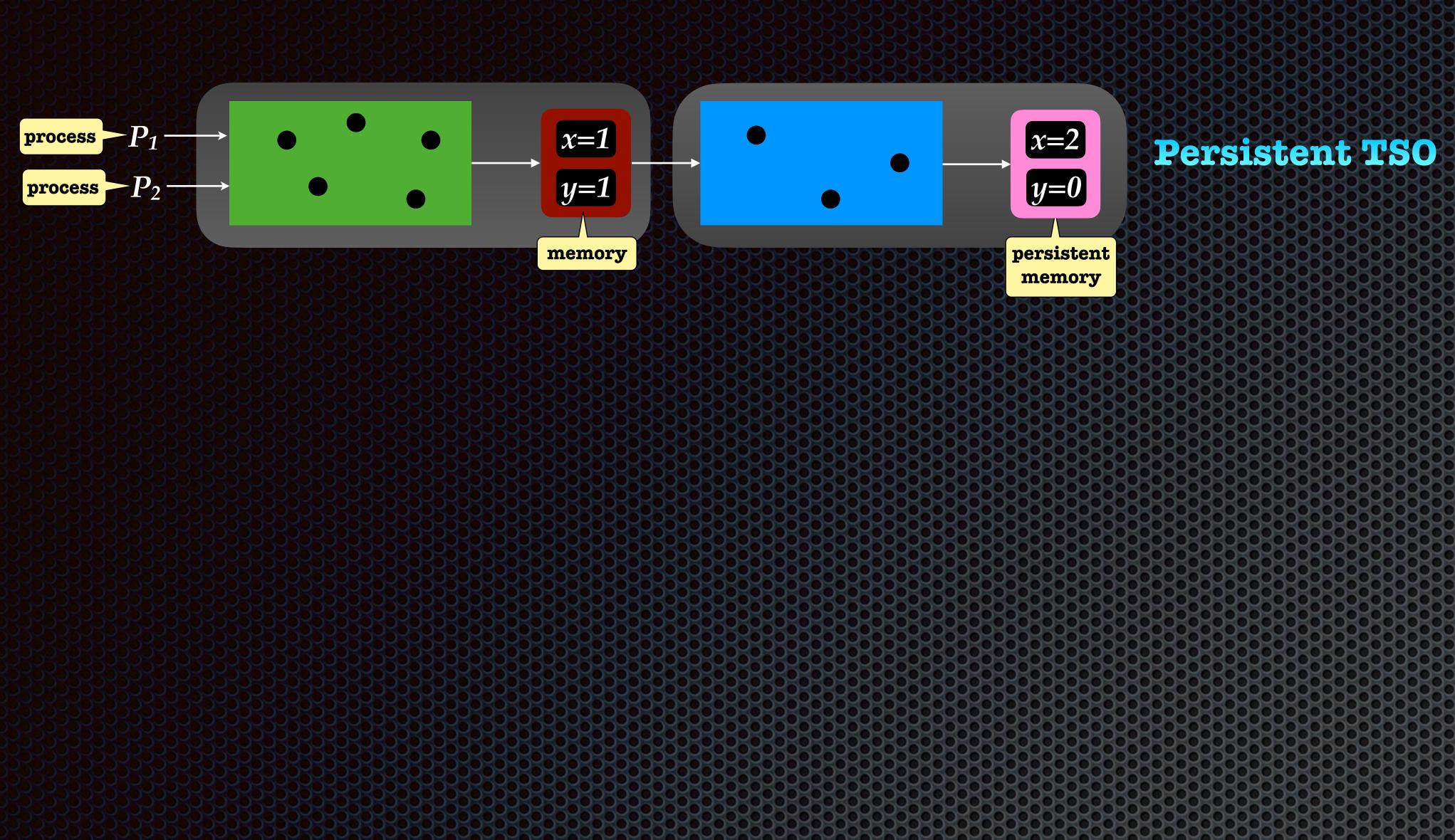


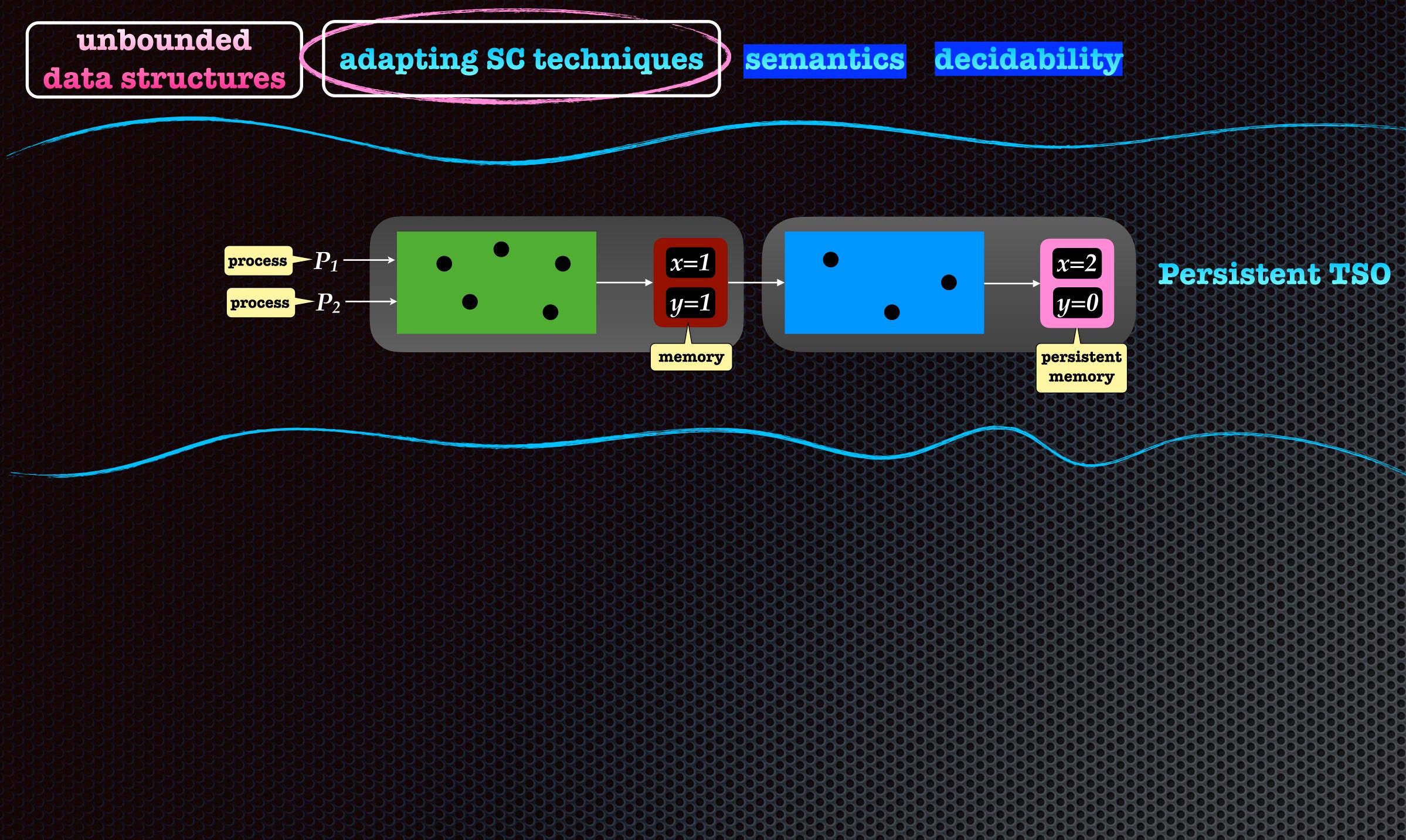
# adapting SC techniques

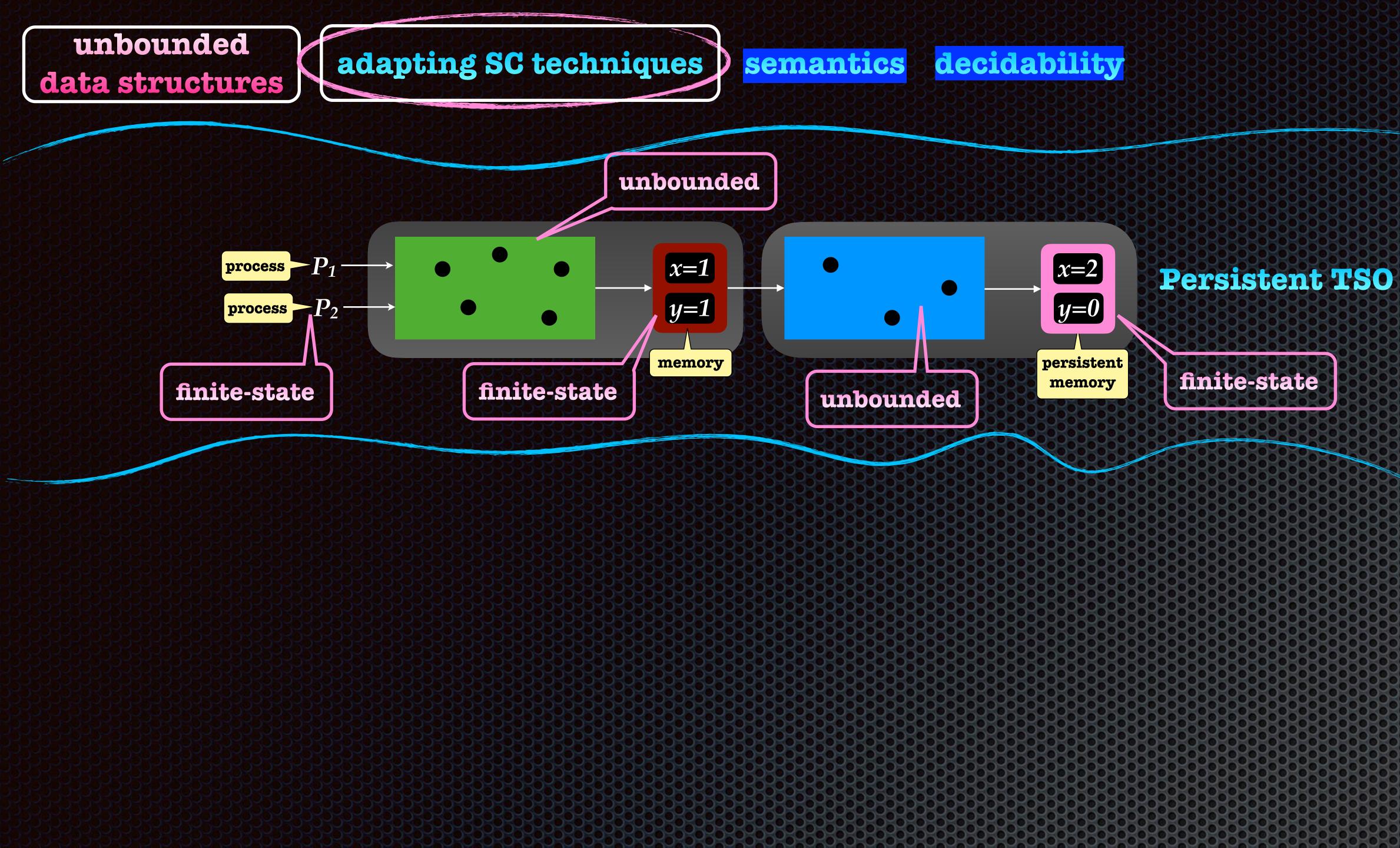


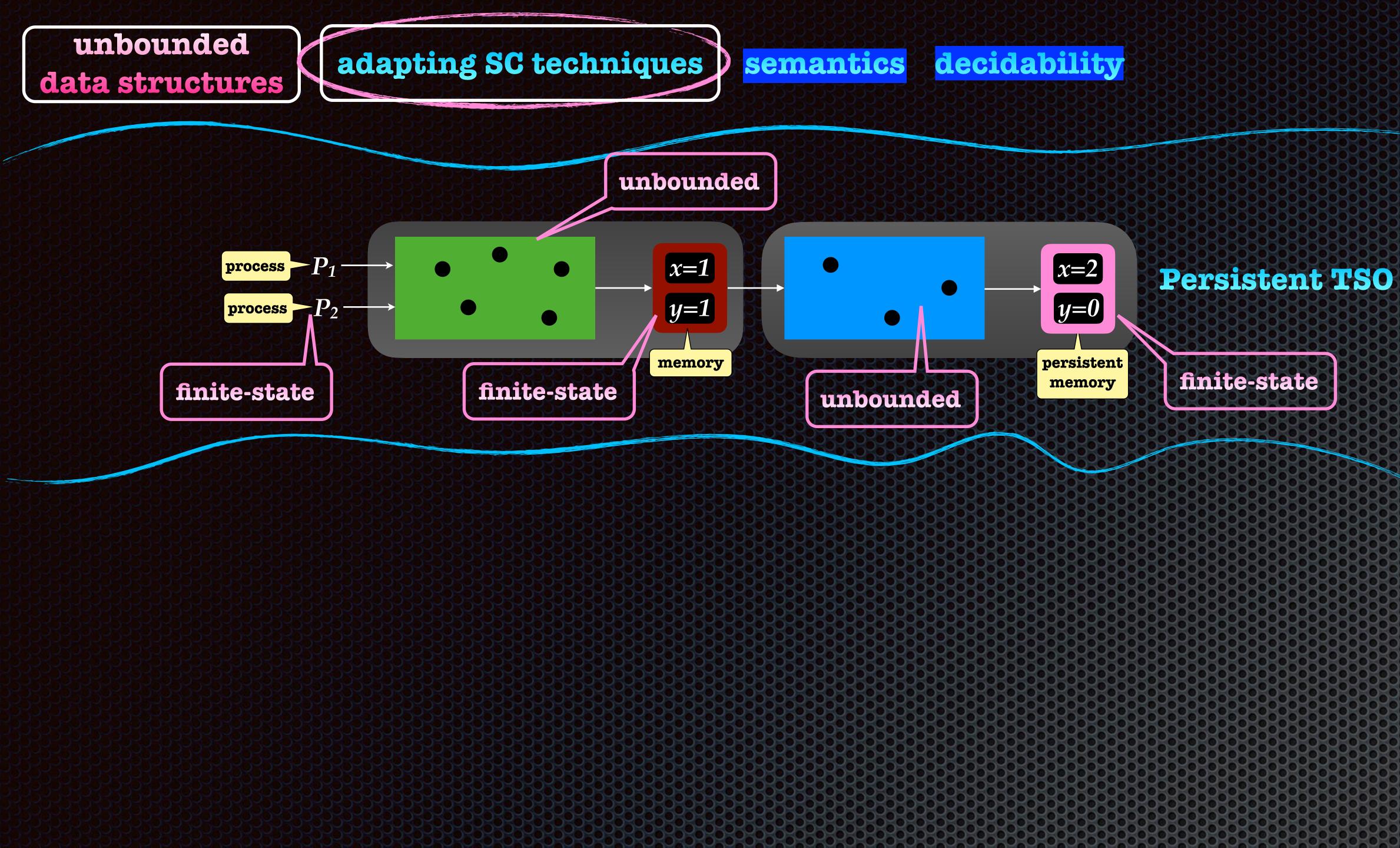


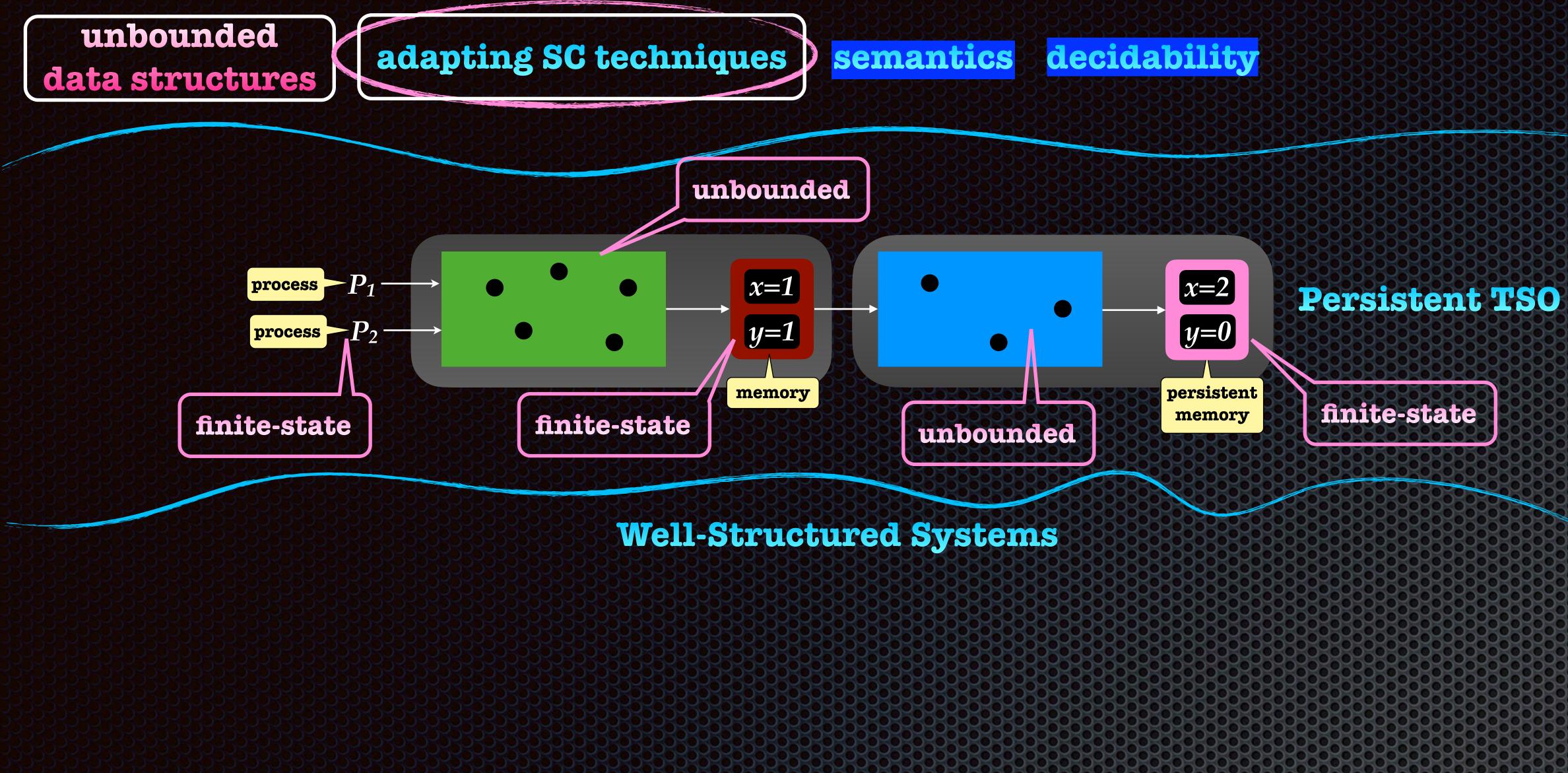


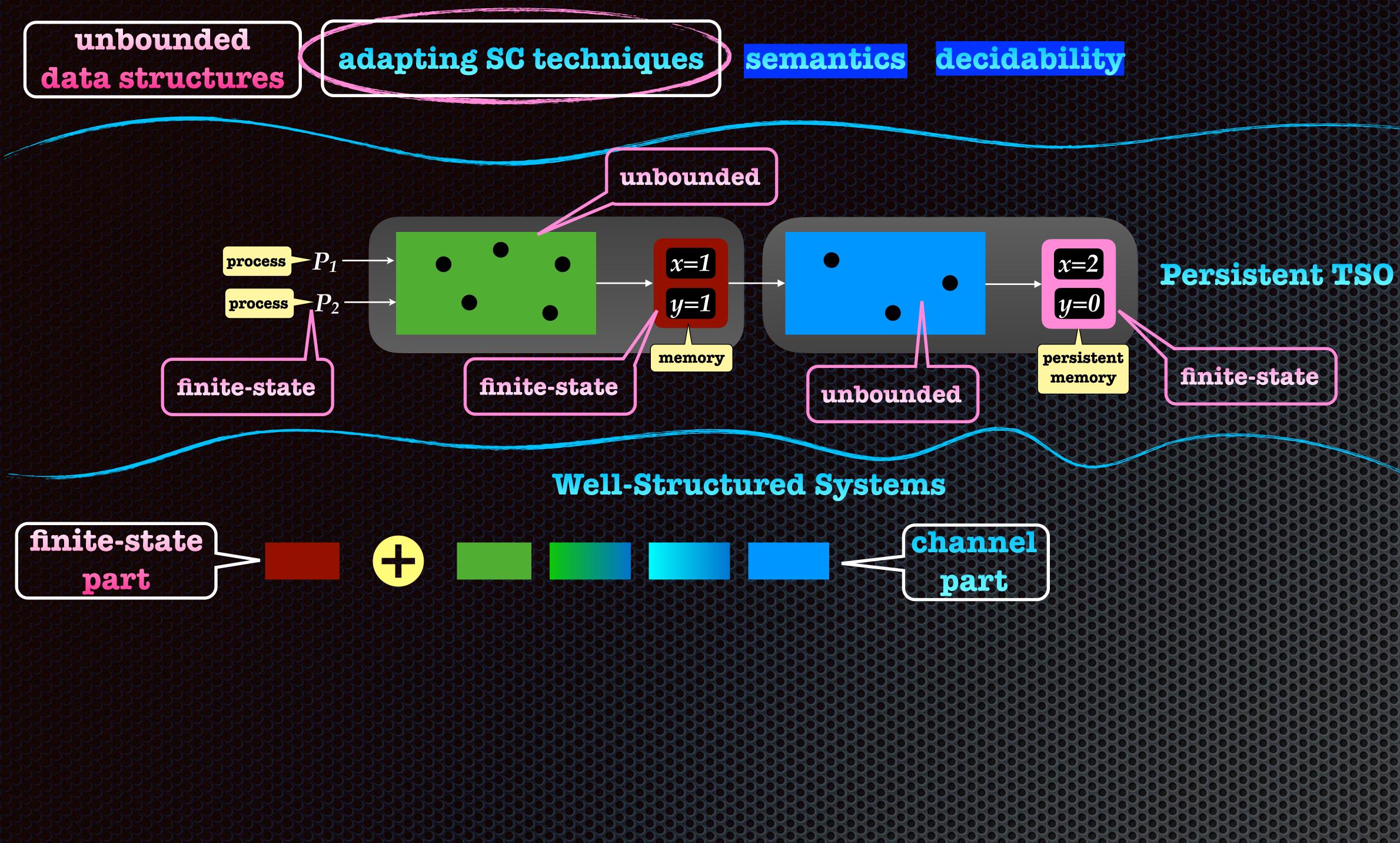


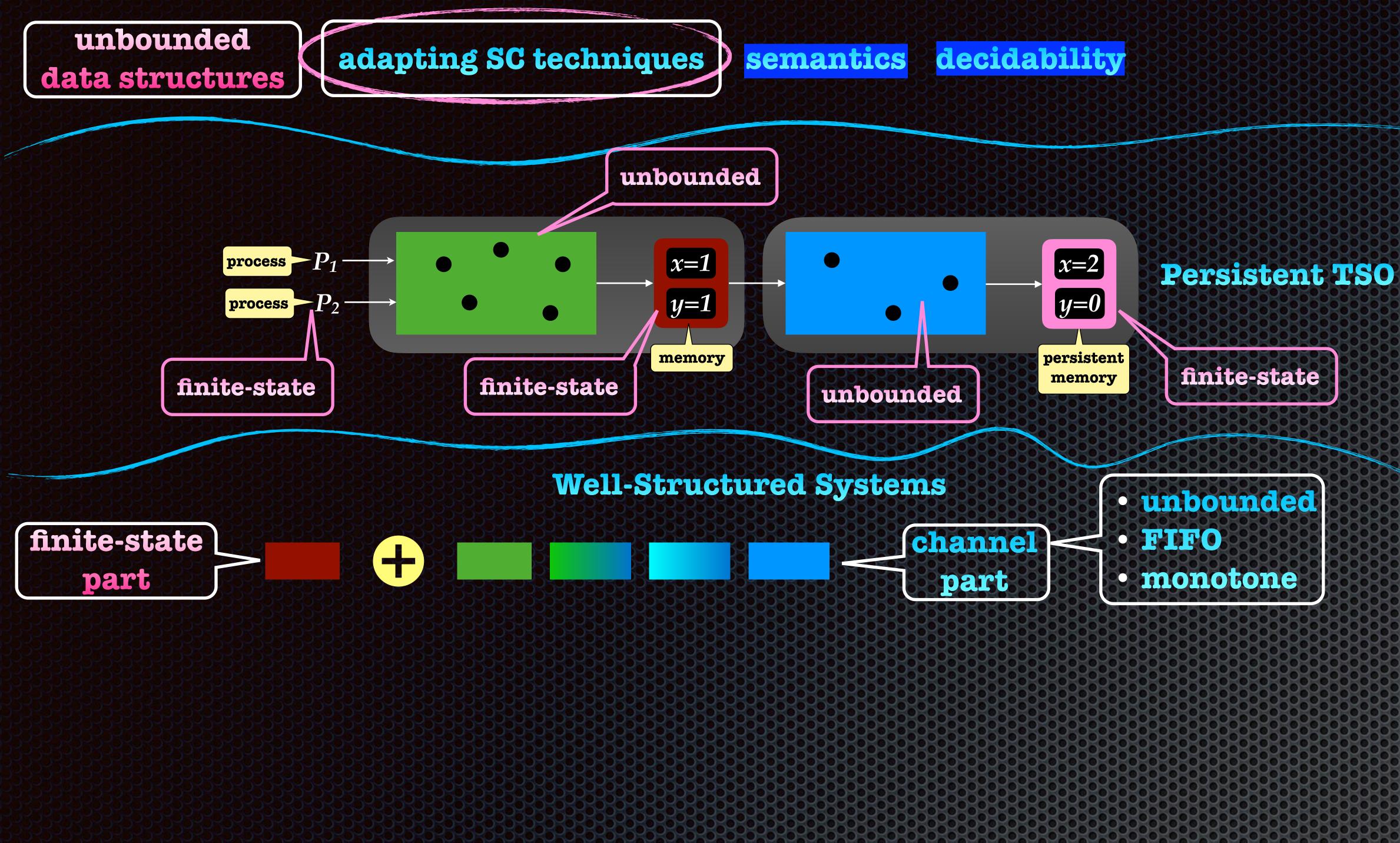


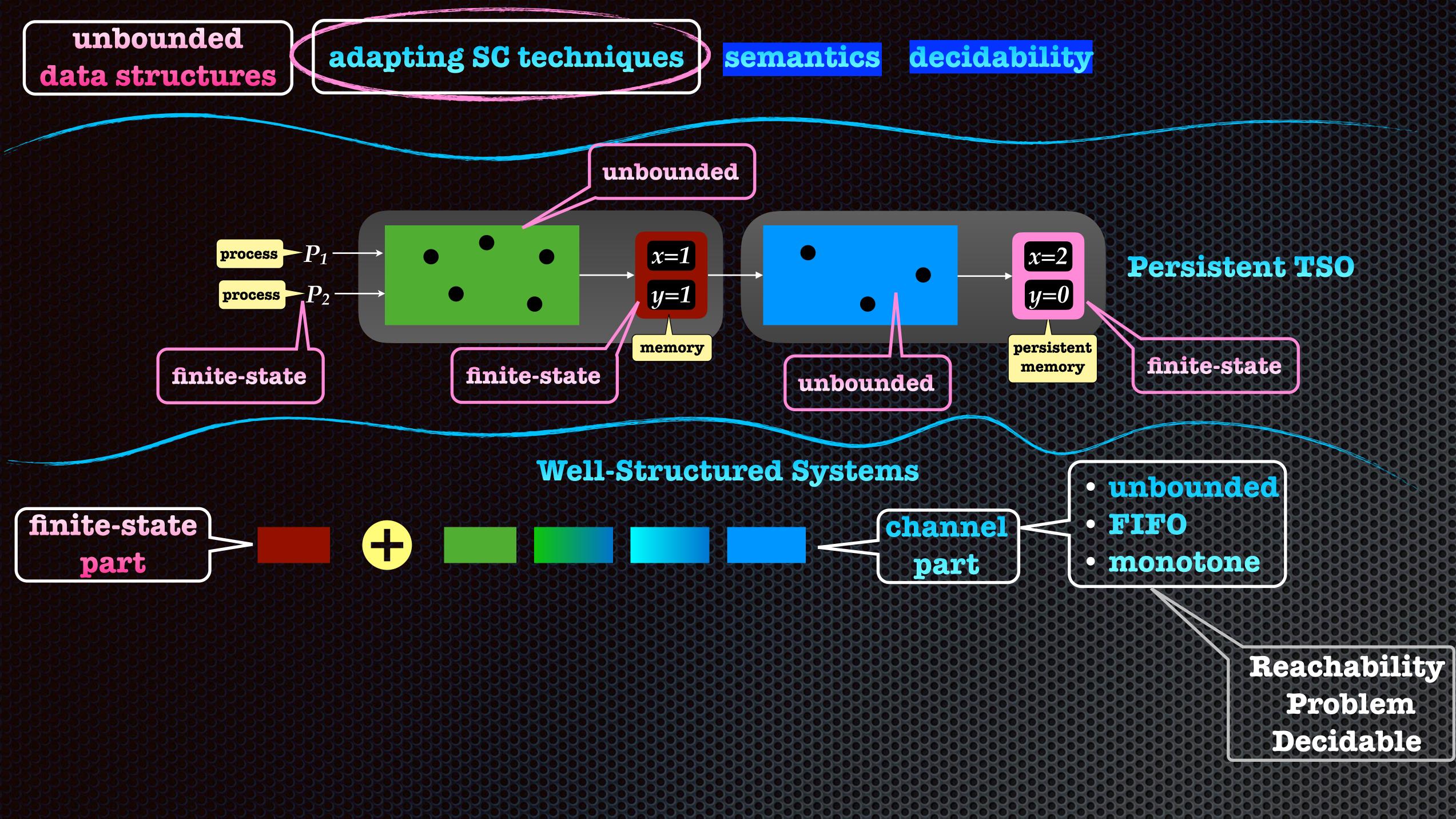




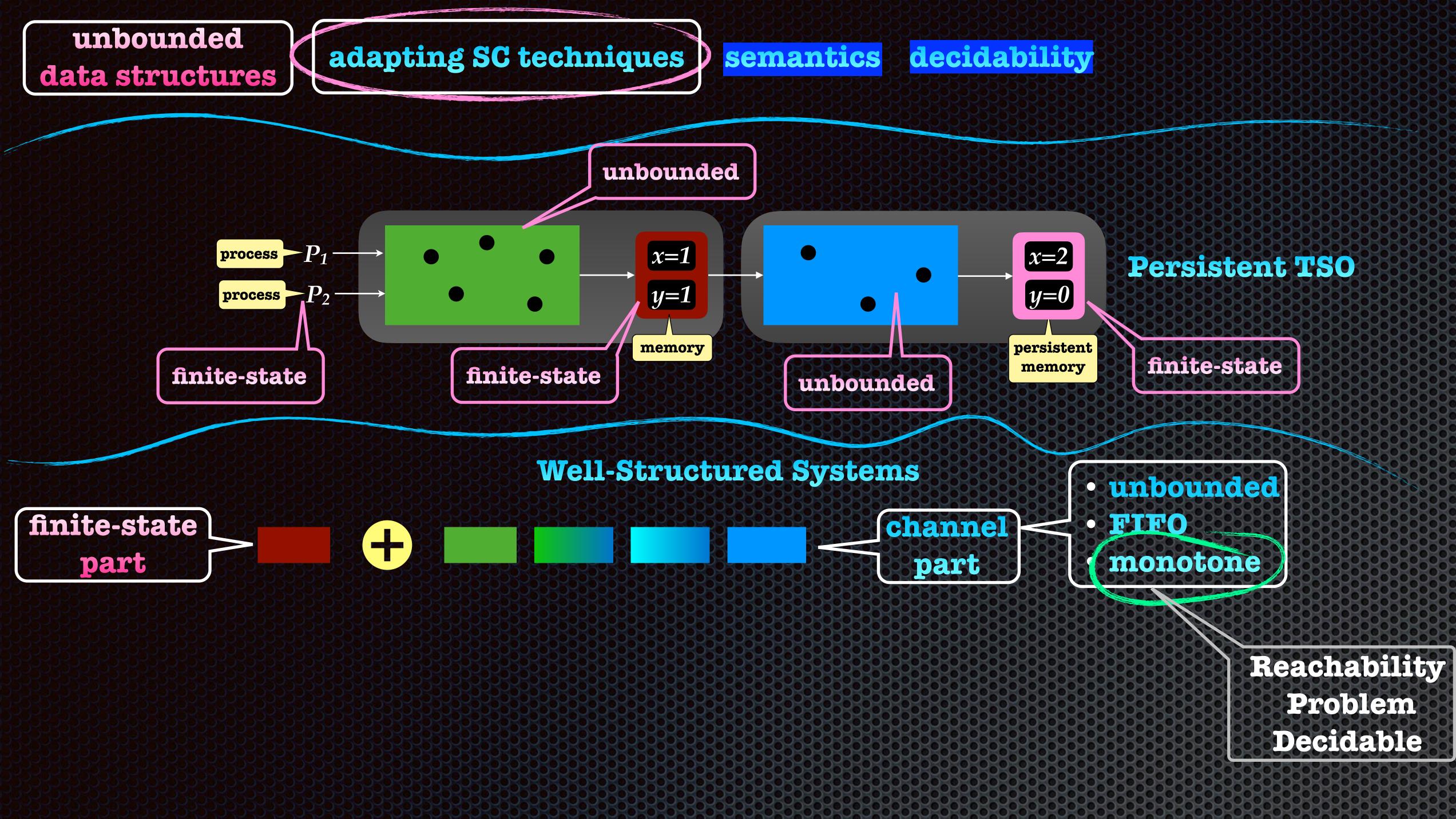




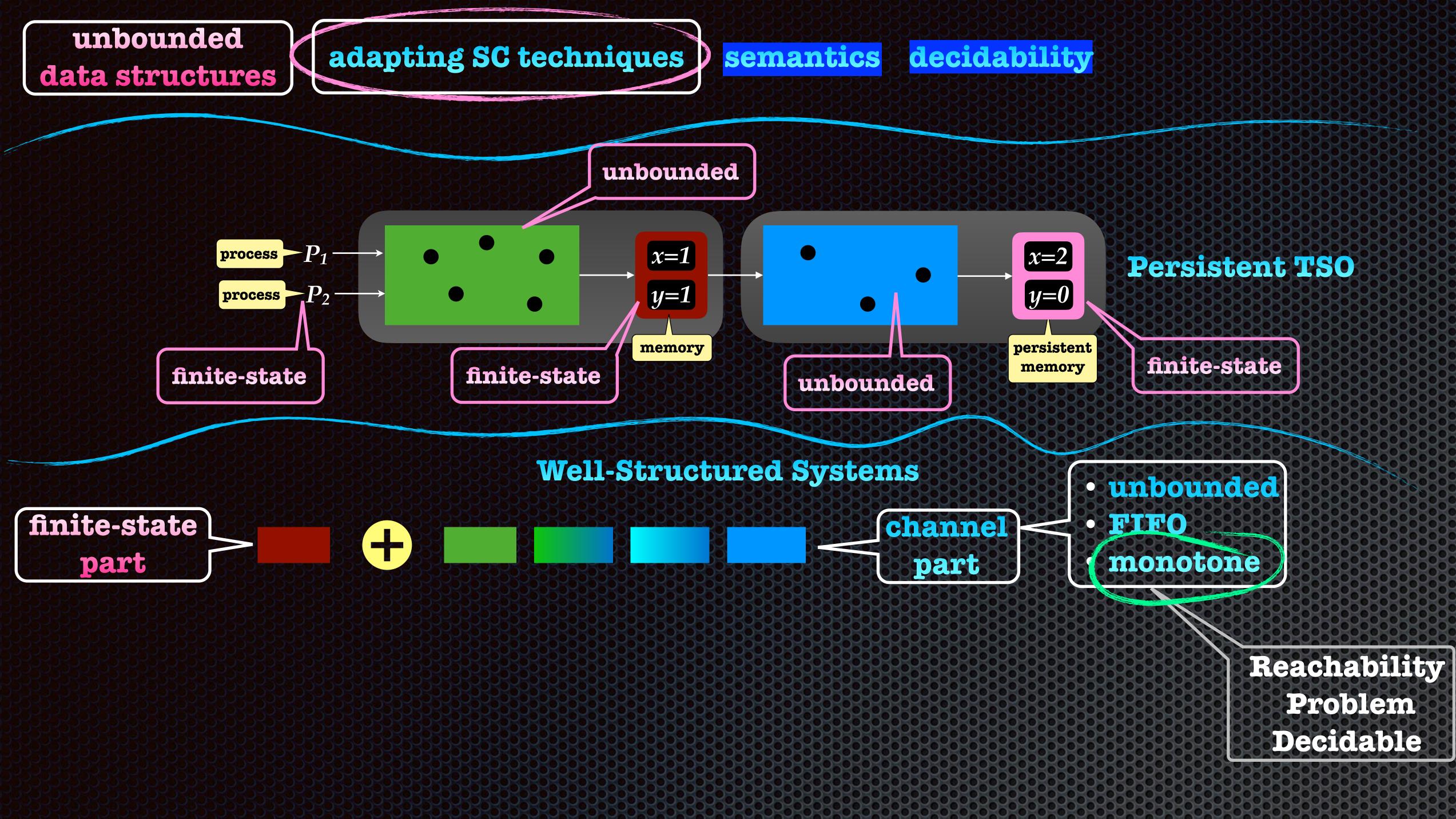




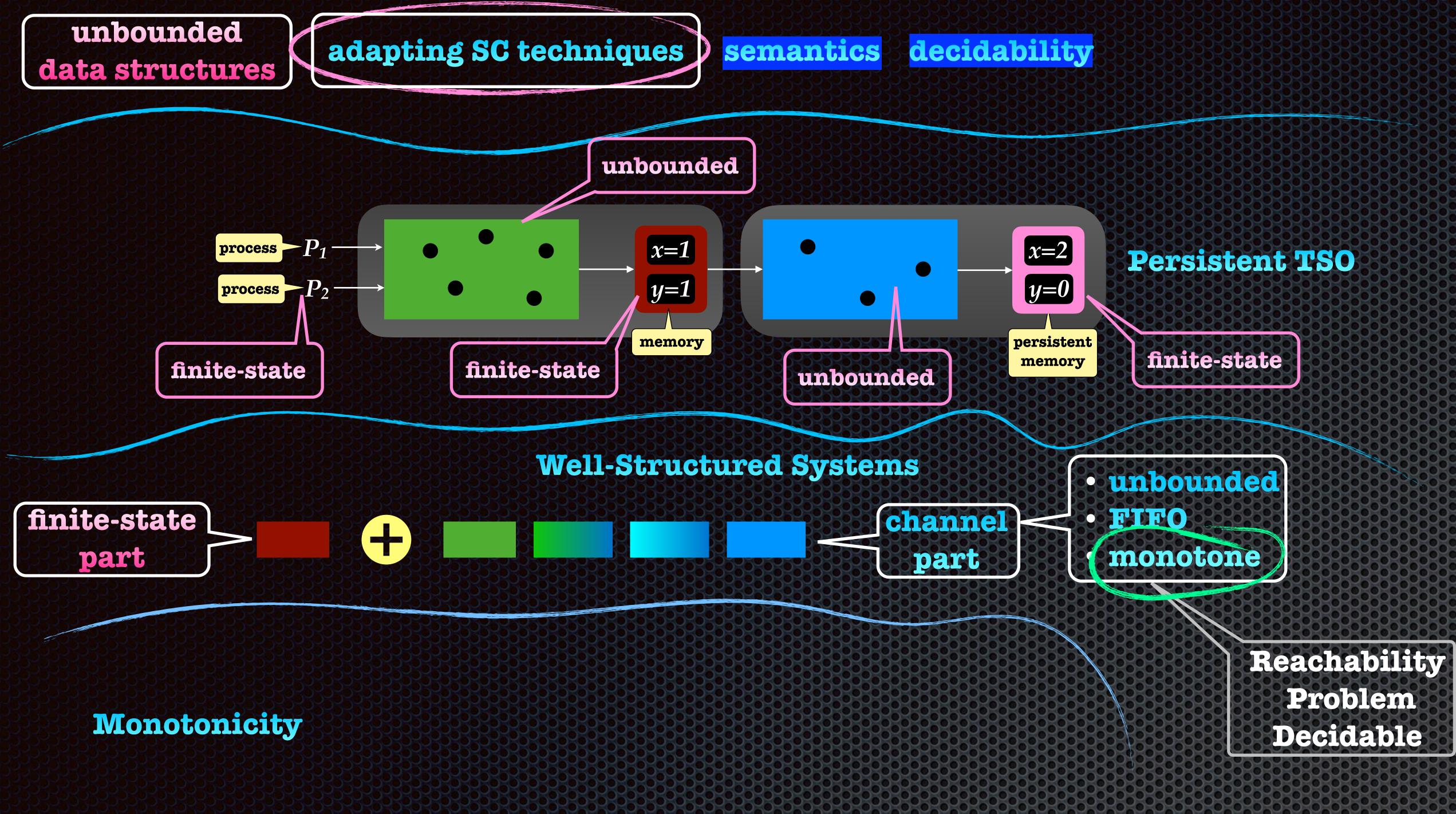




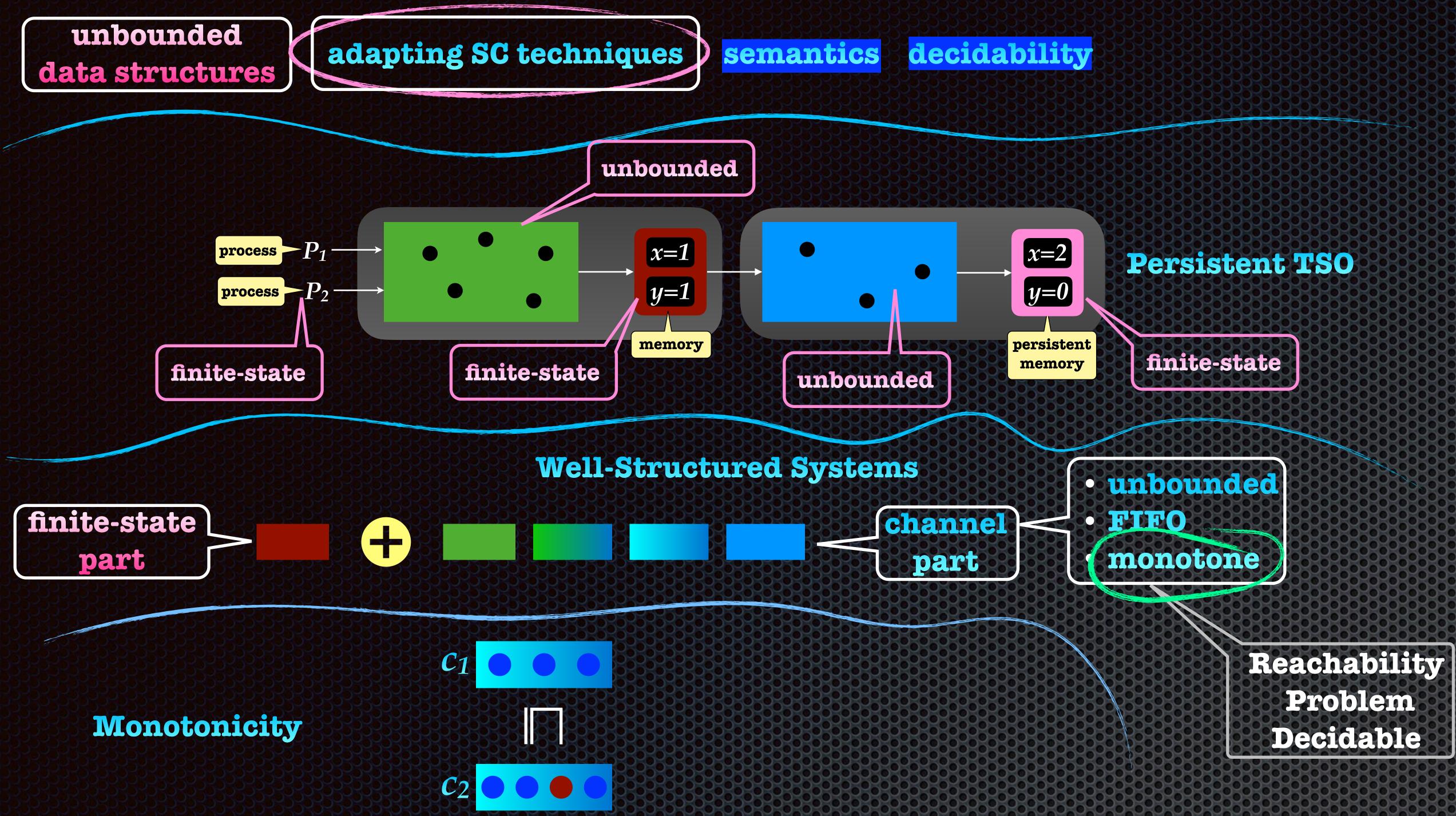




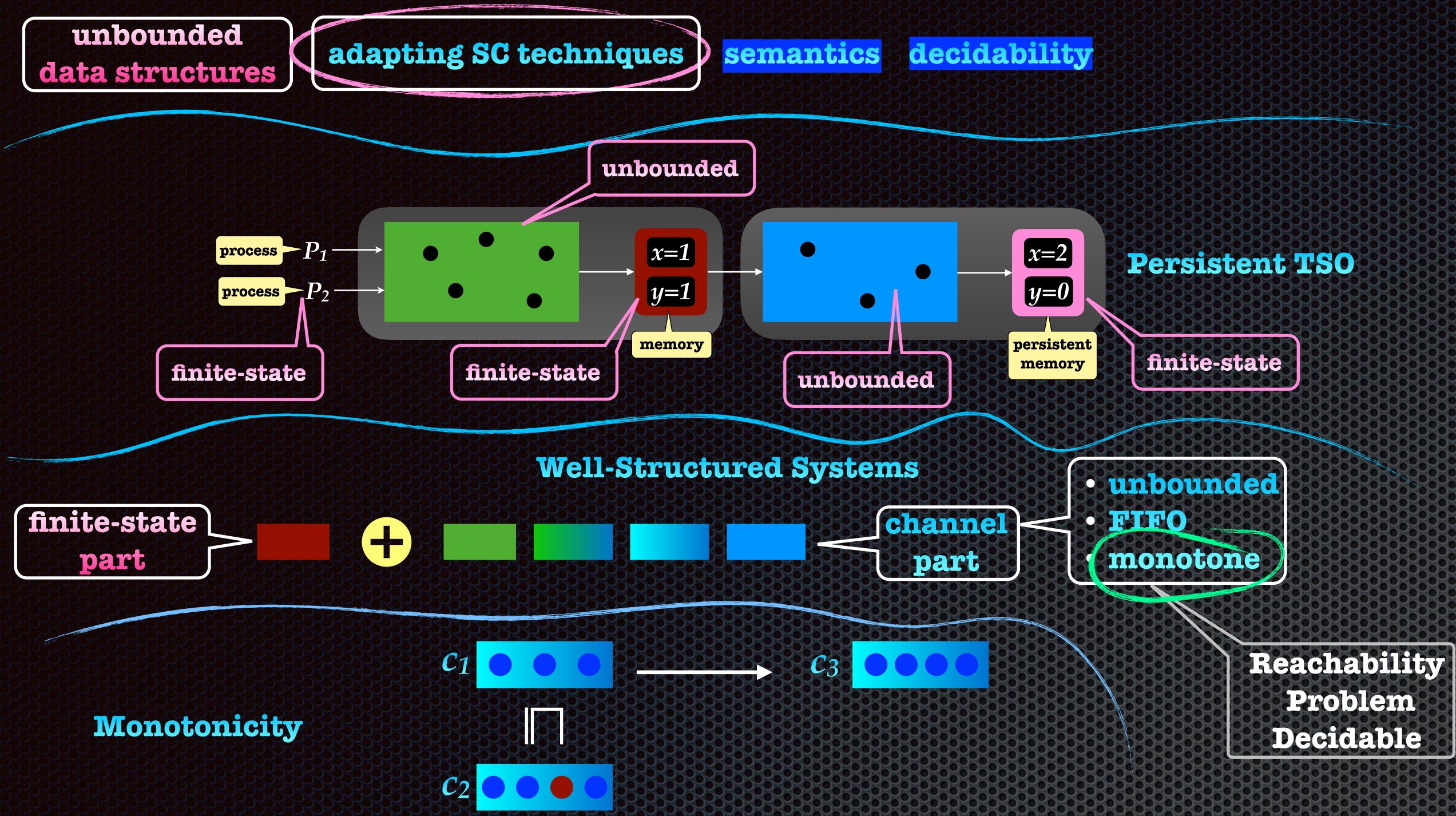




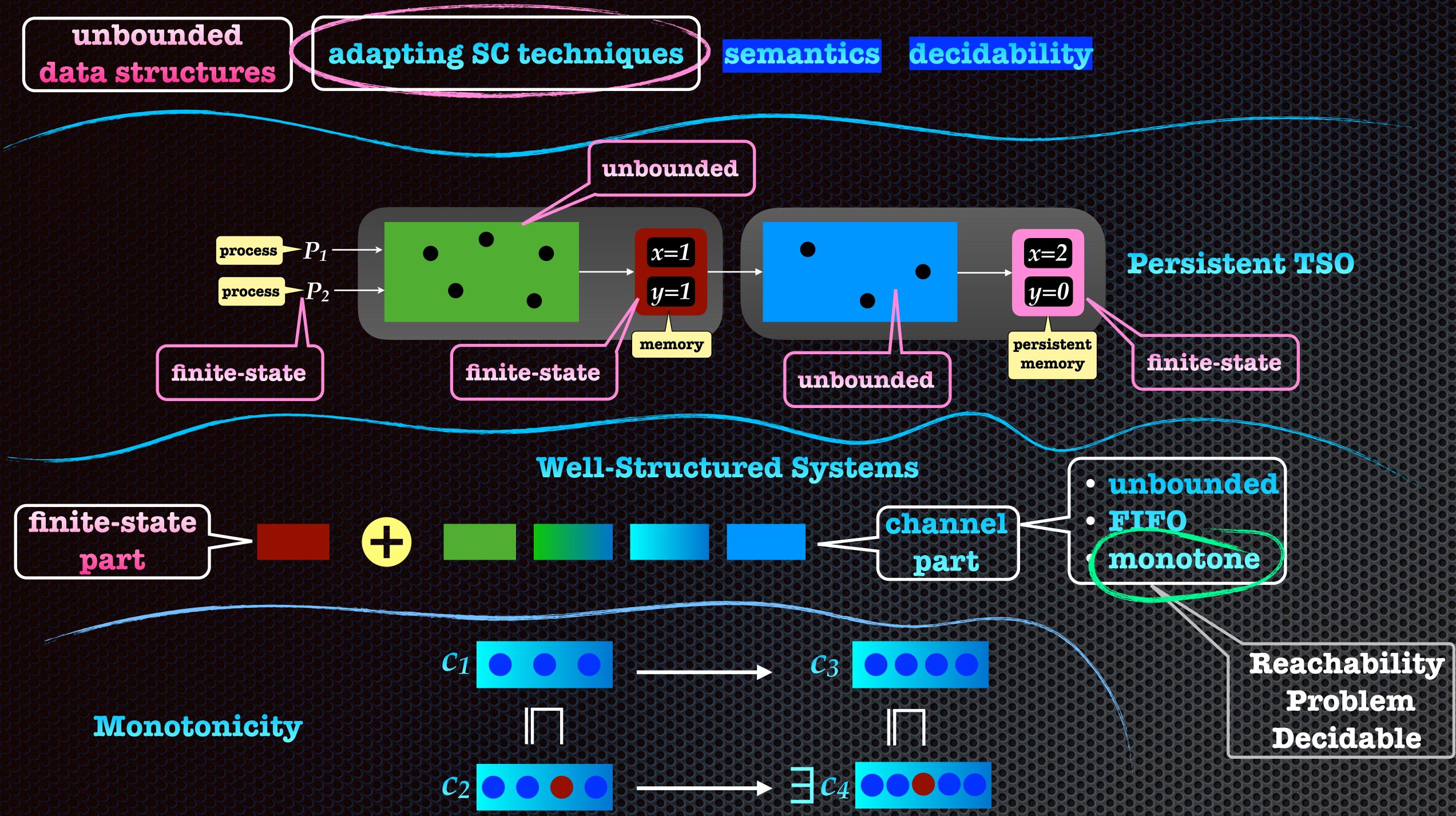




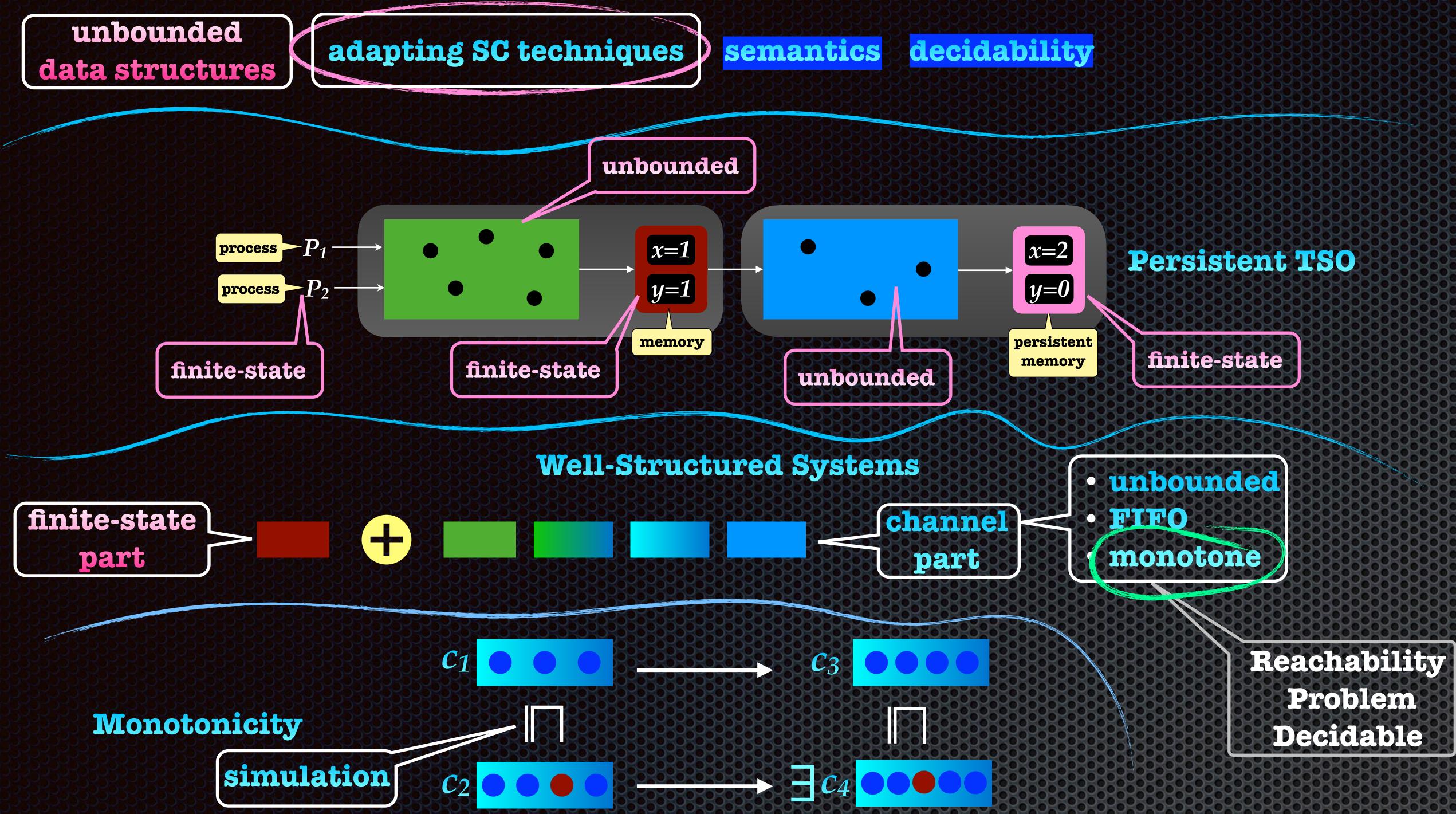




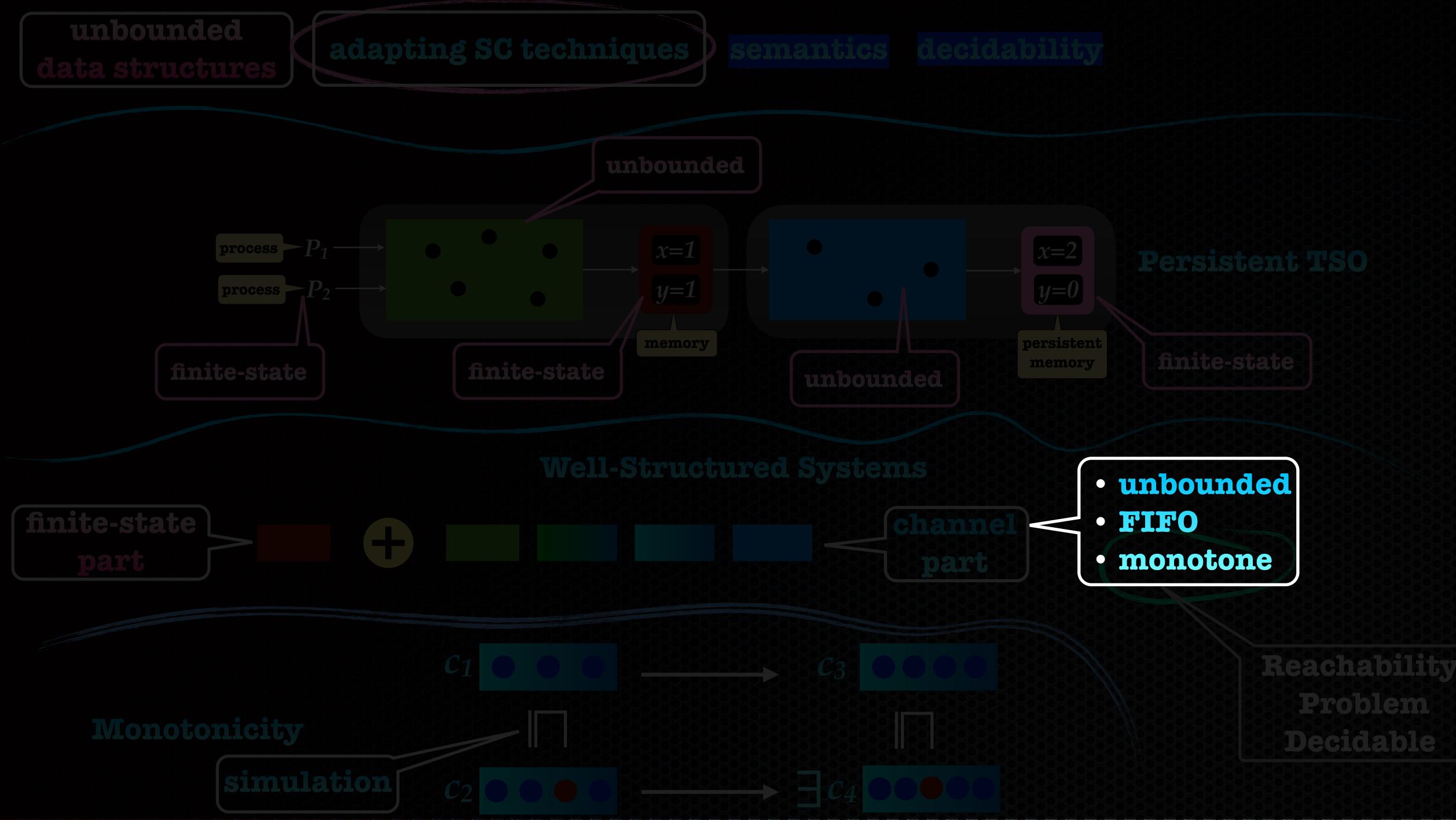




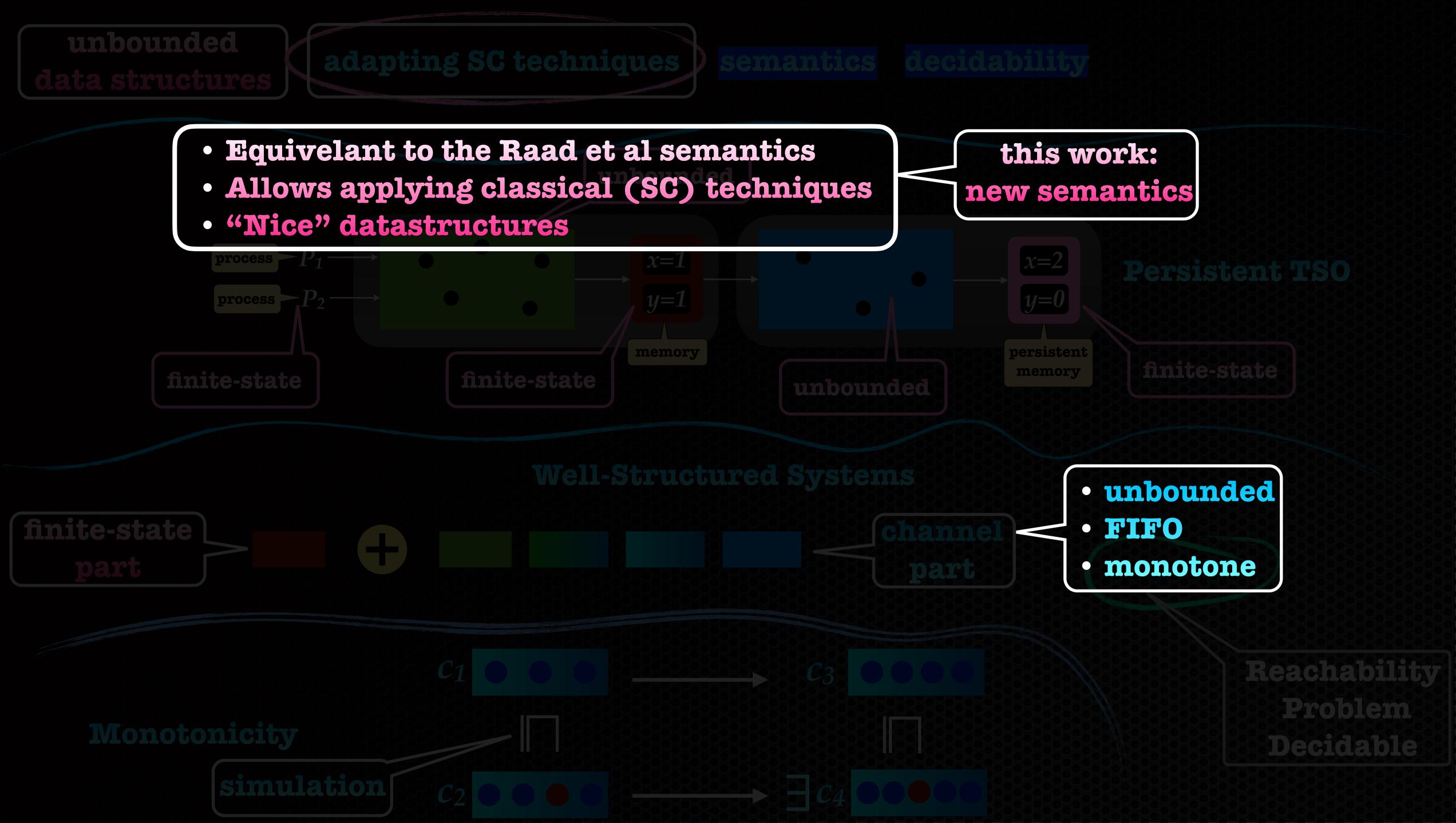






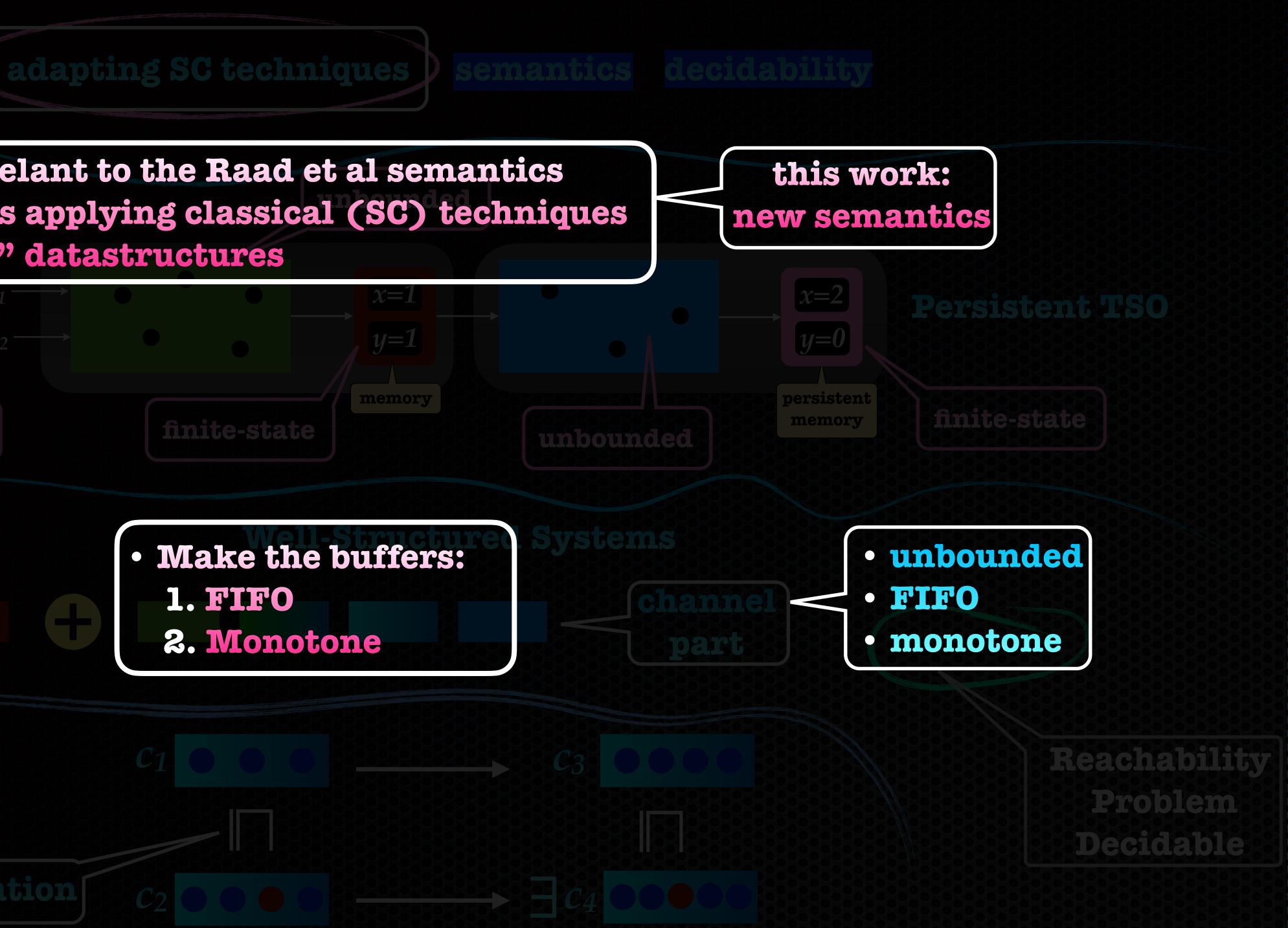


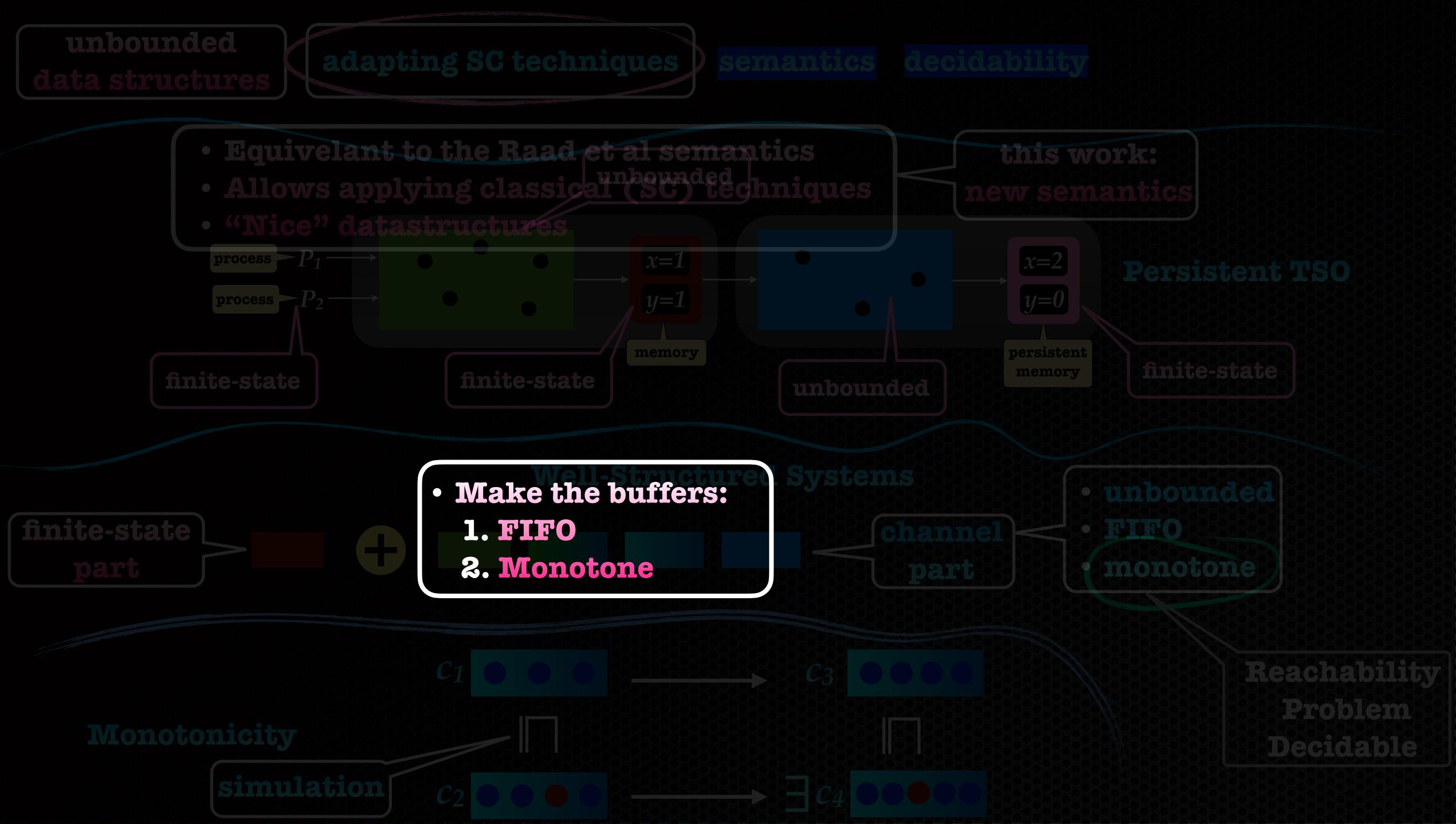




unbounded • Equivelant to the Raad et al semantics • Allows applying classical (SC) techniques • "Nice" datastructures process memory • Make the buffers: finite-state 1. FIFO 2. Monotone







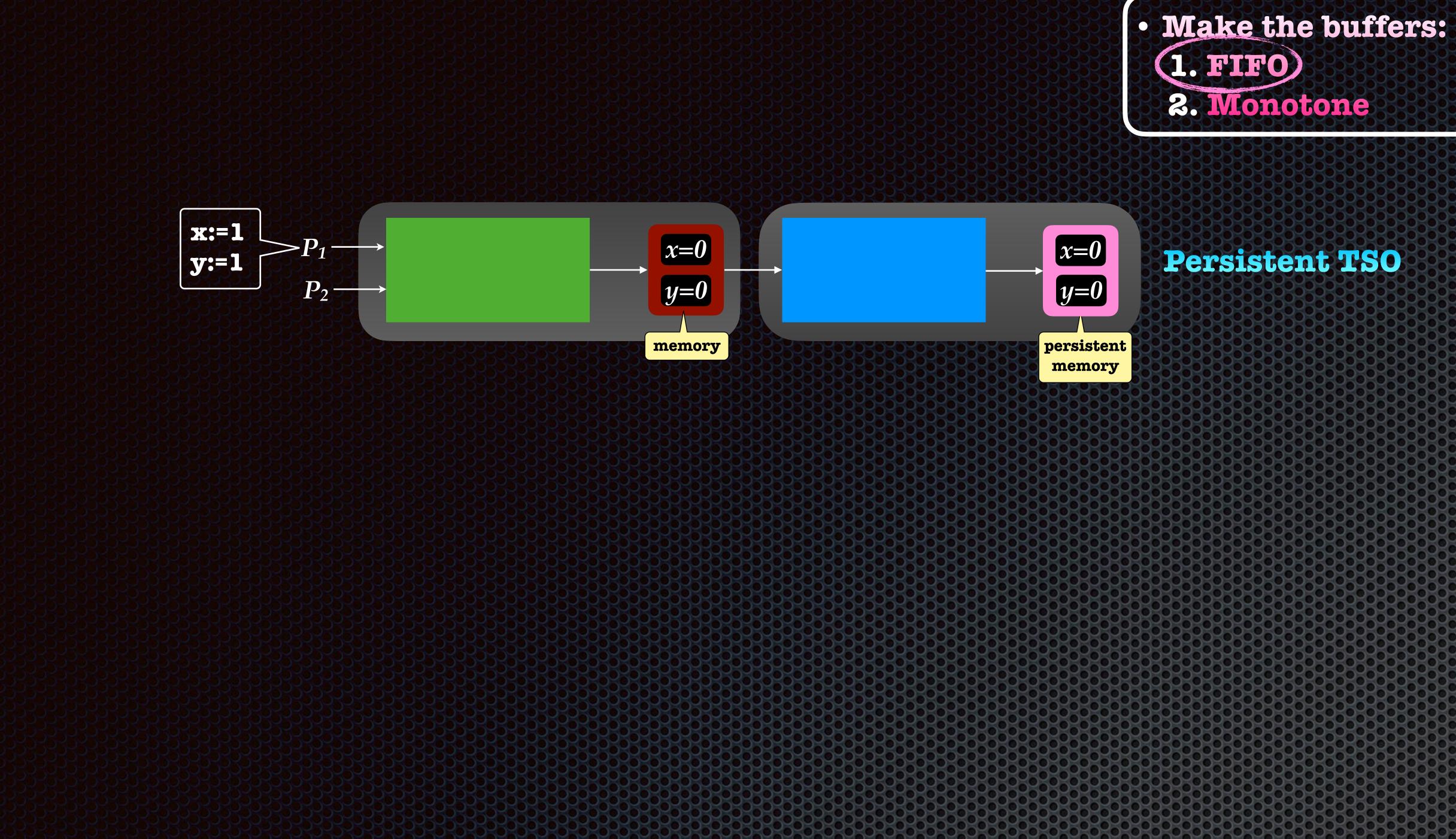




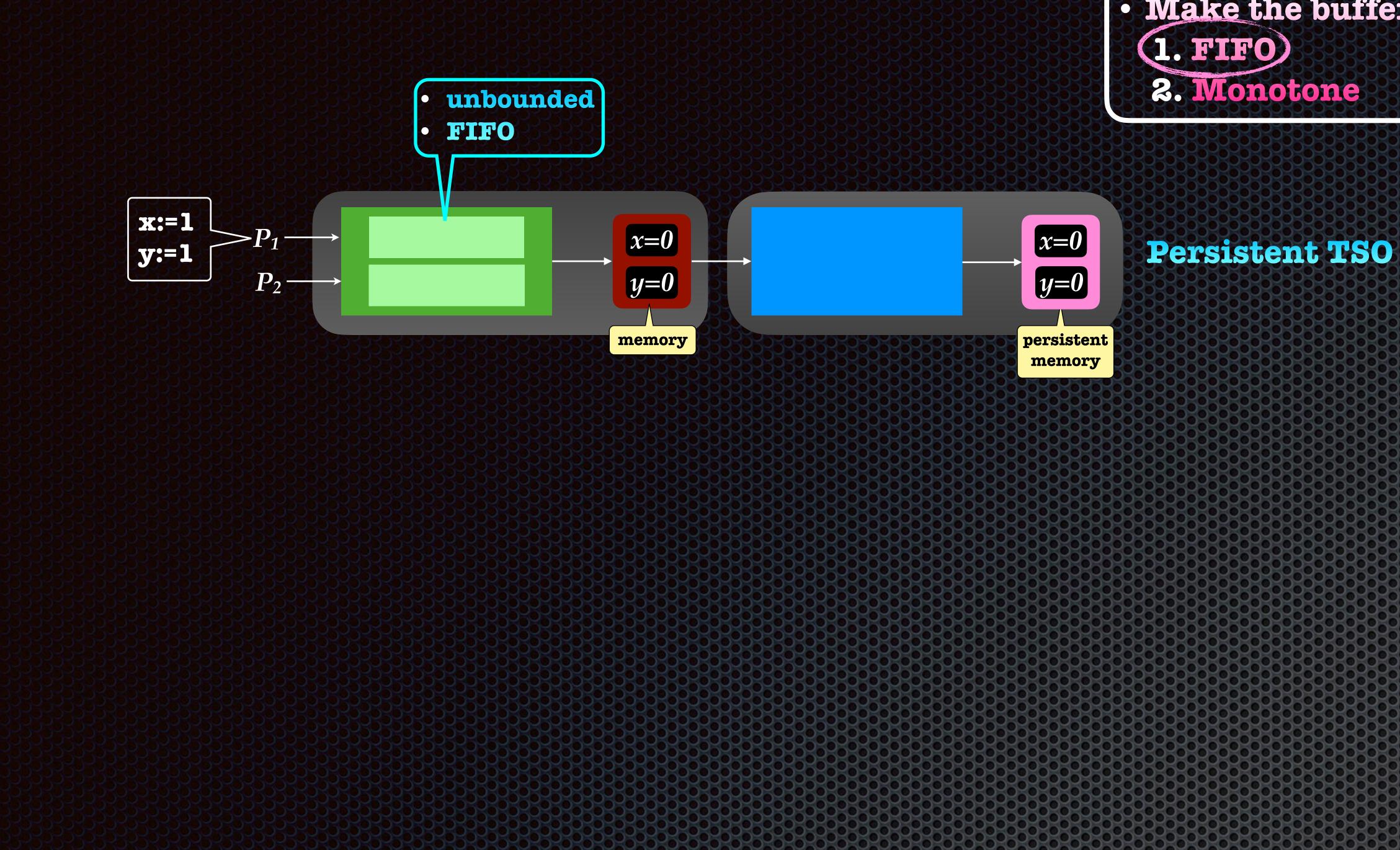




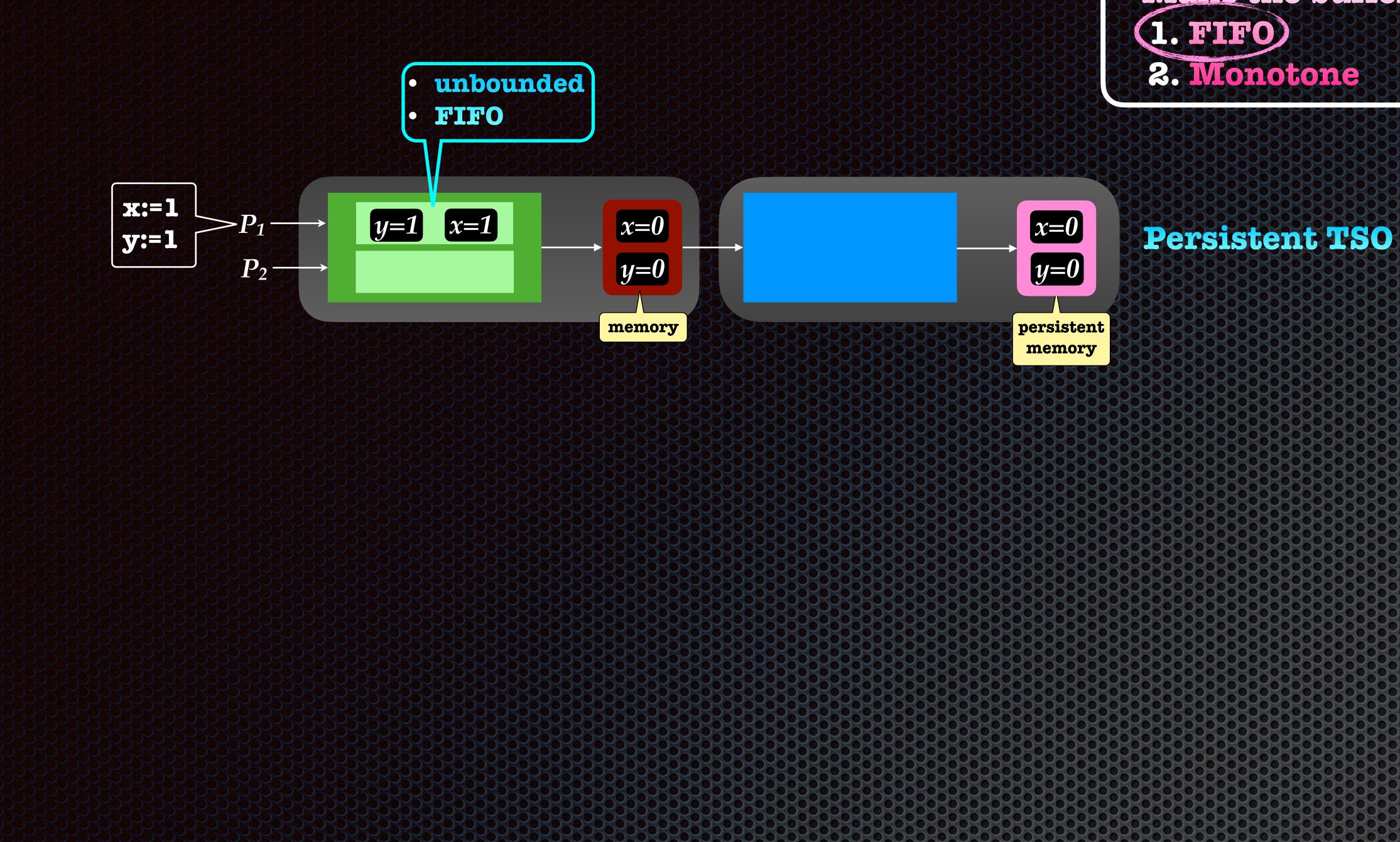




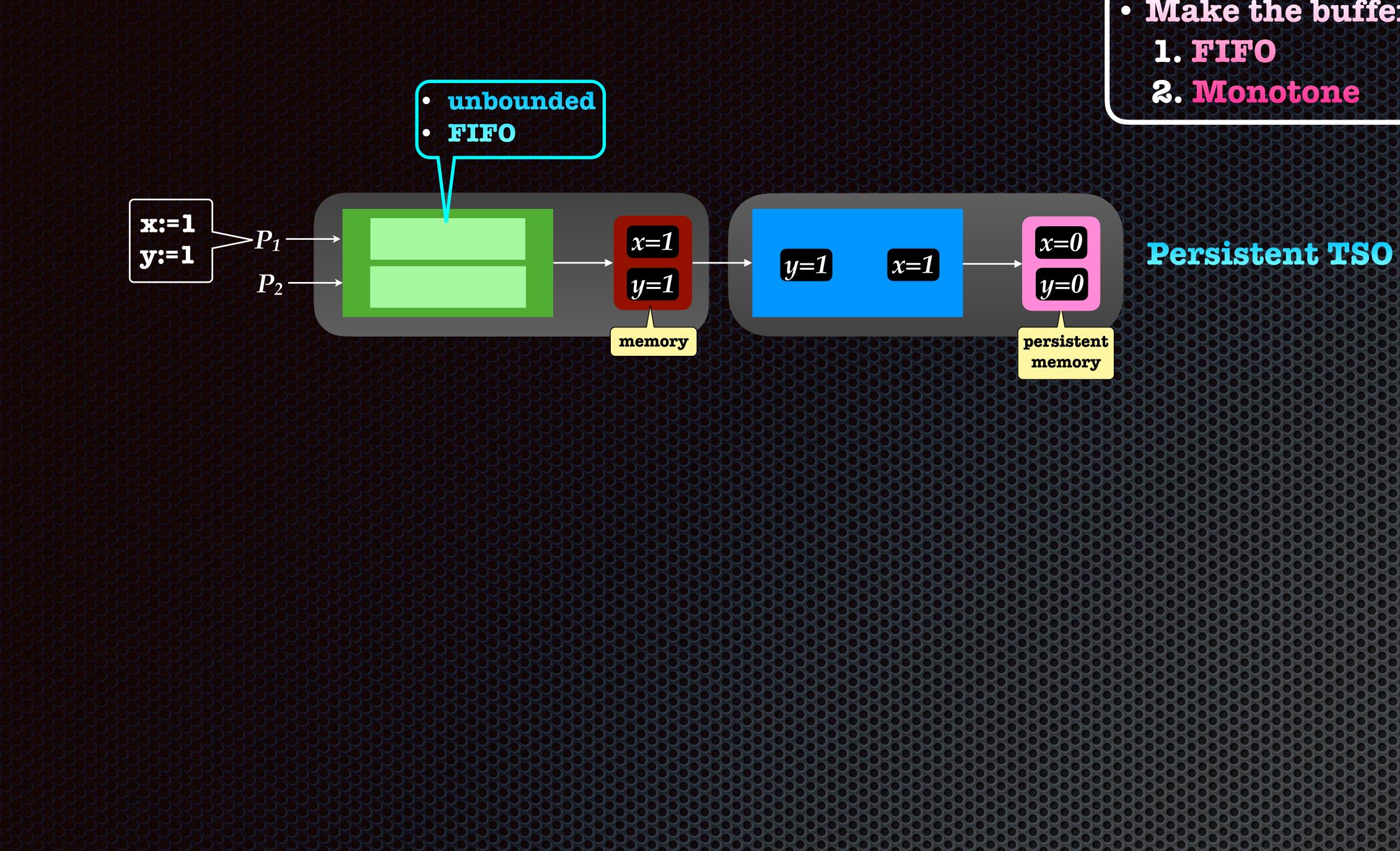




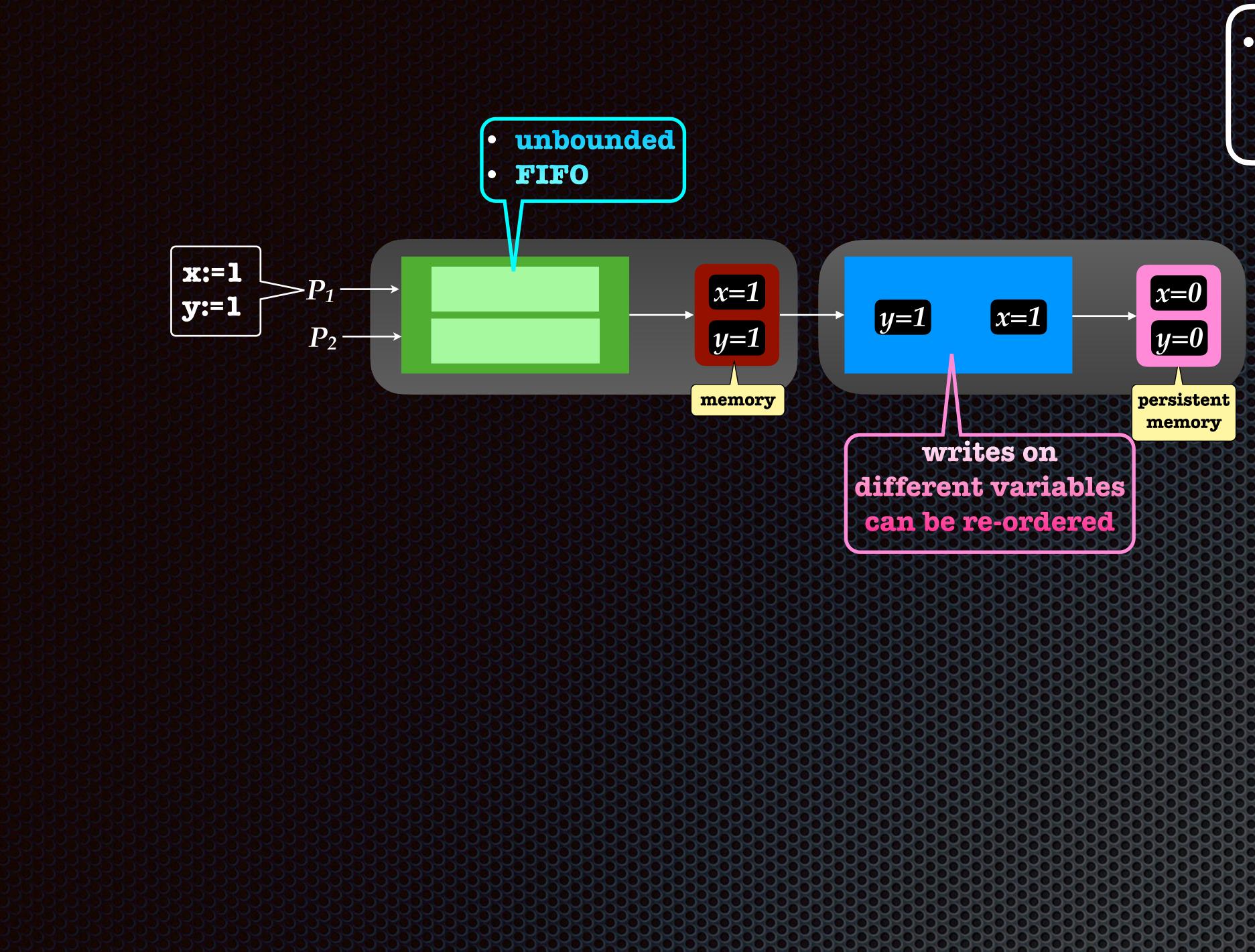








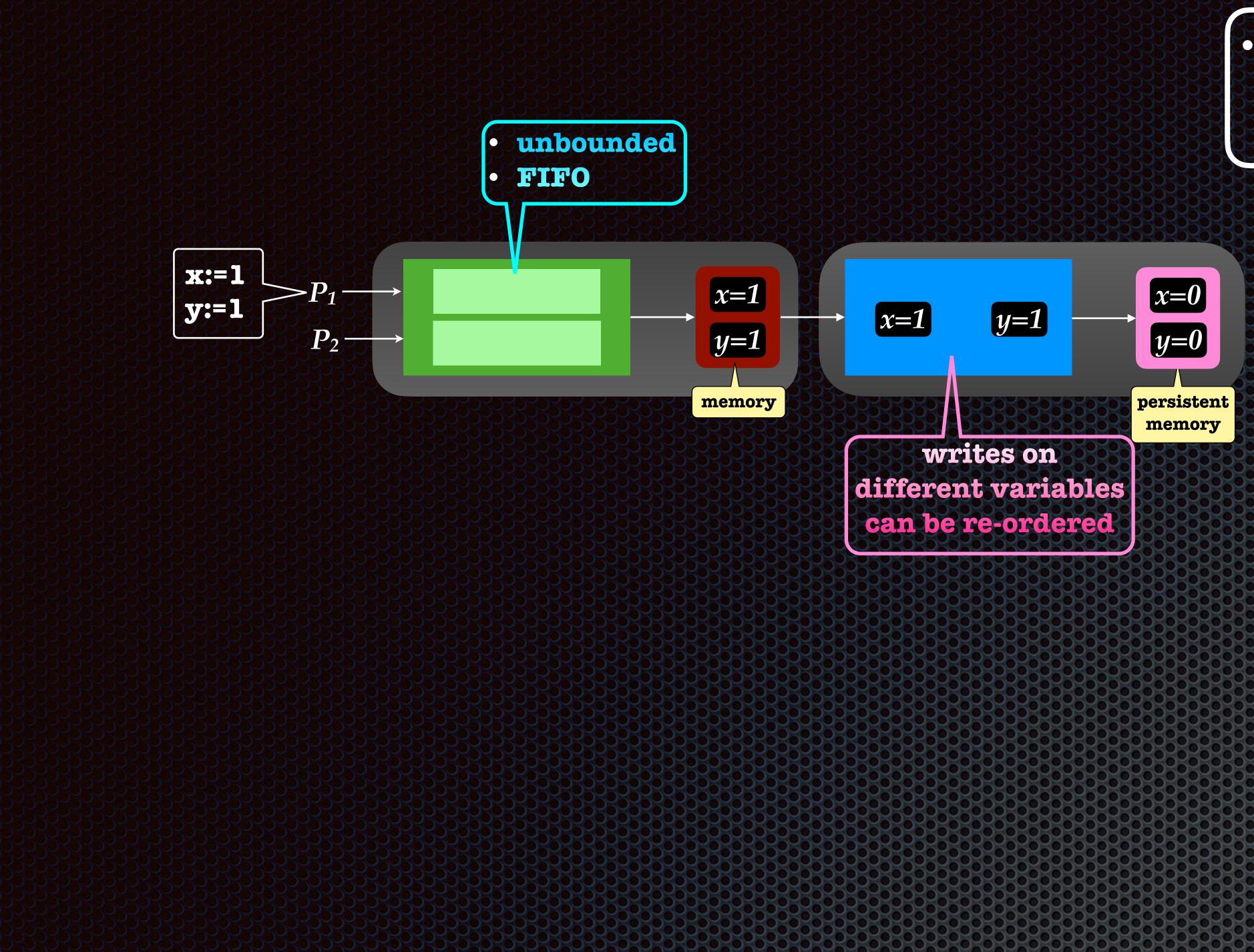




Make the buffers:
1. FIFO
2. Monotone

### **Persistent TSO**

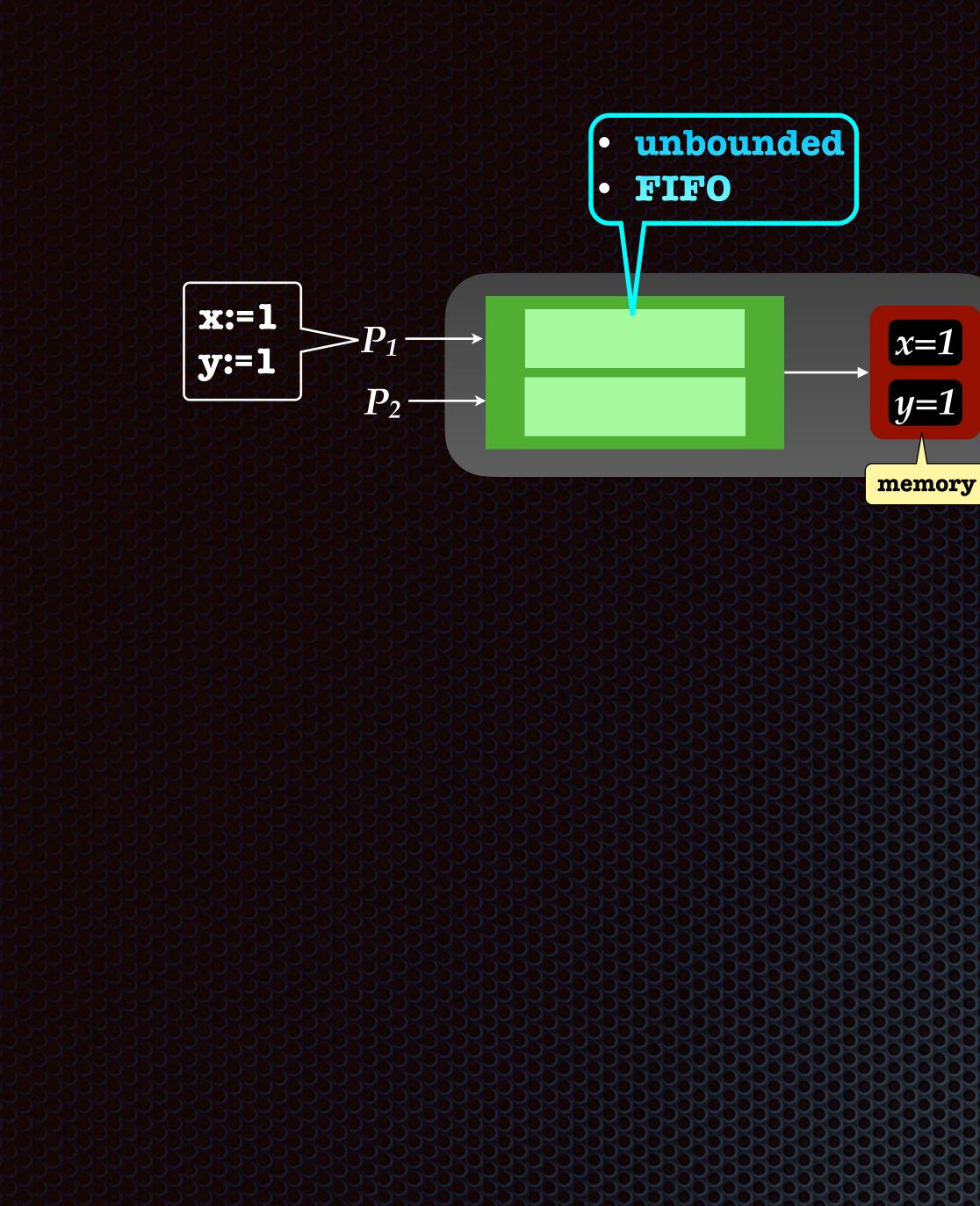




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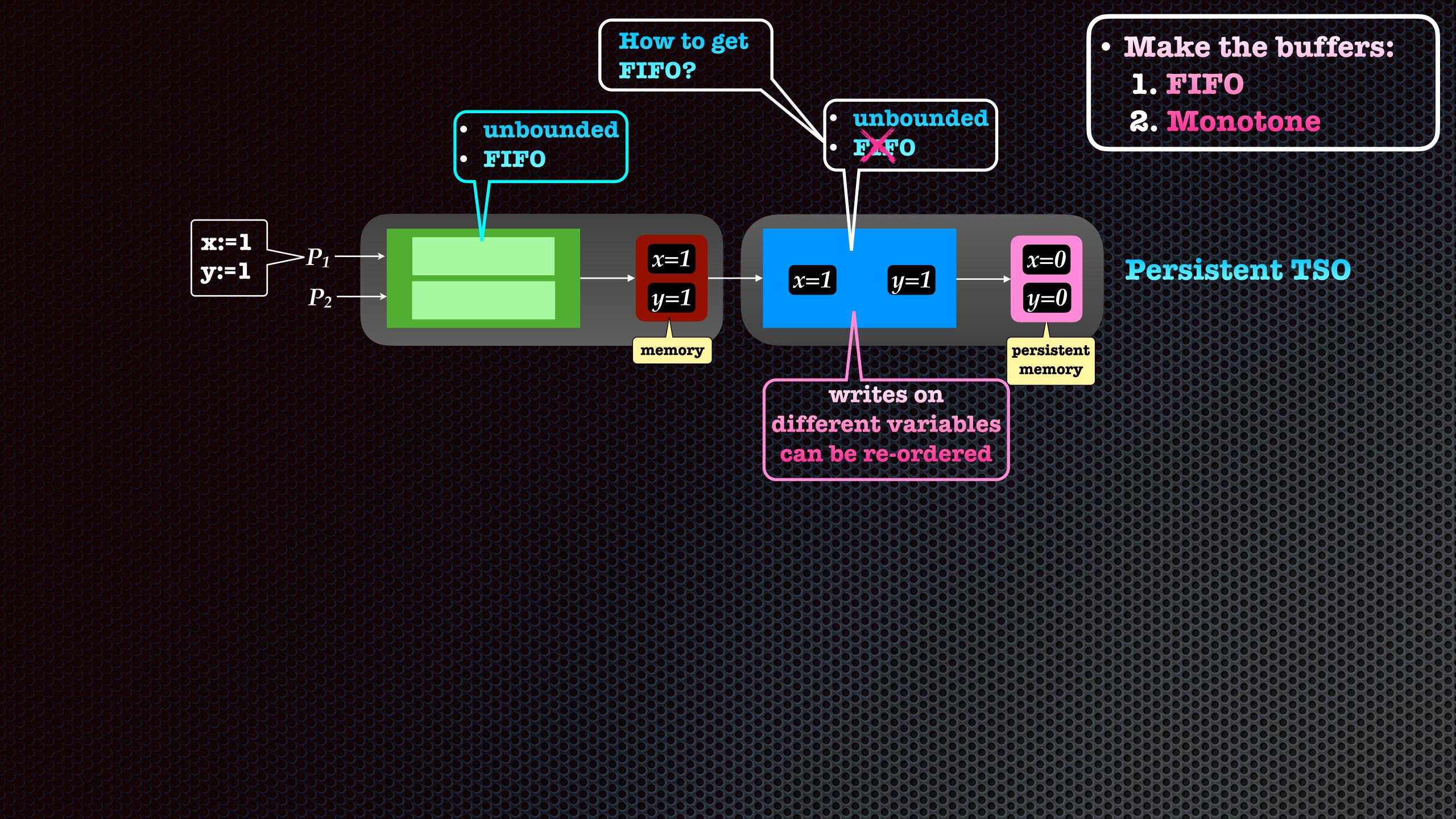
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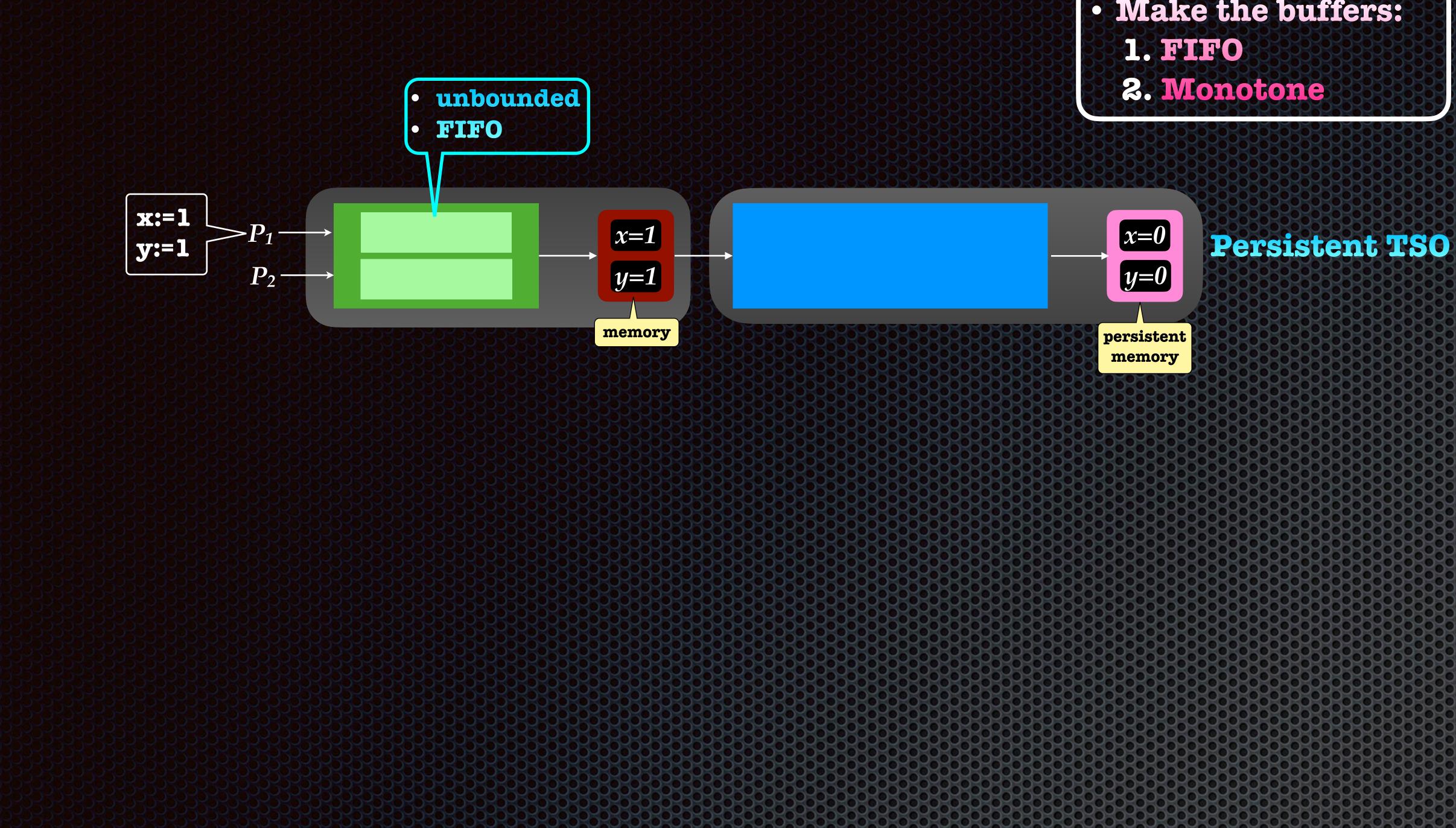




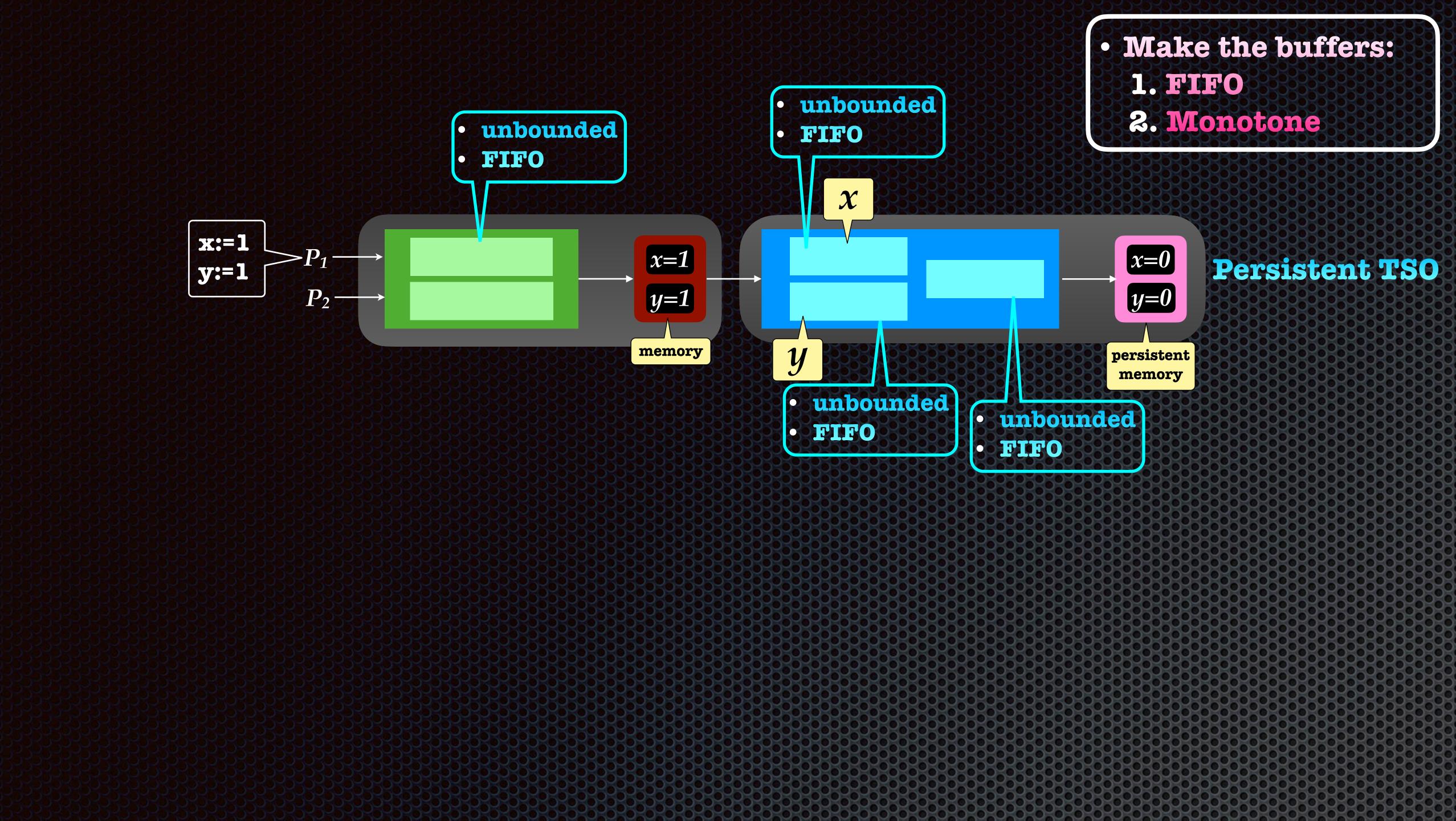
• Make the buffers: 1. FIFO unboundedFFO 2. Monotone x=0 **Persistent TSO** x=1 y=1 *y=0* persistent memory writes on different variables can be re-ordered

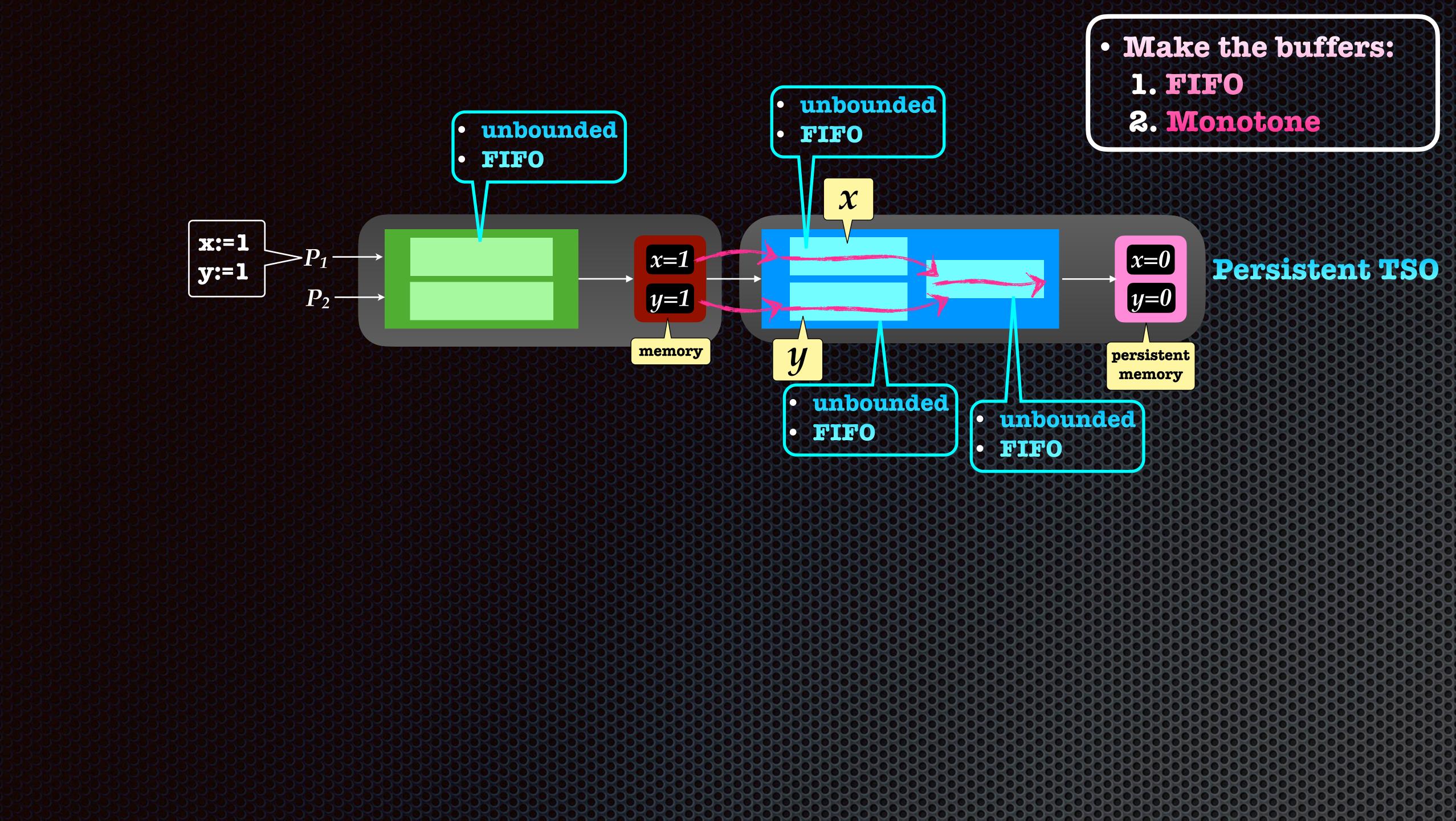


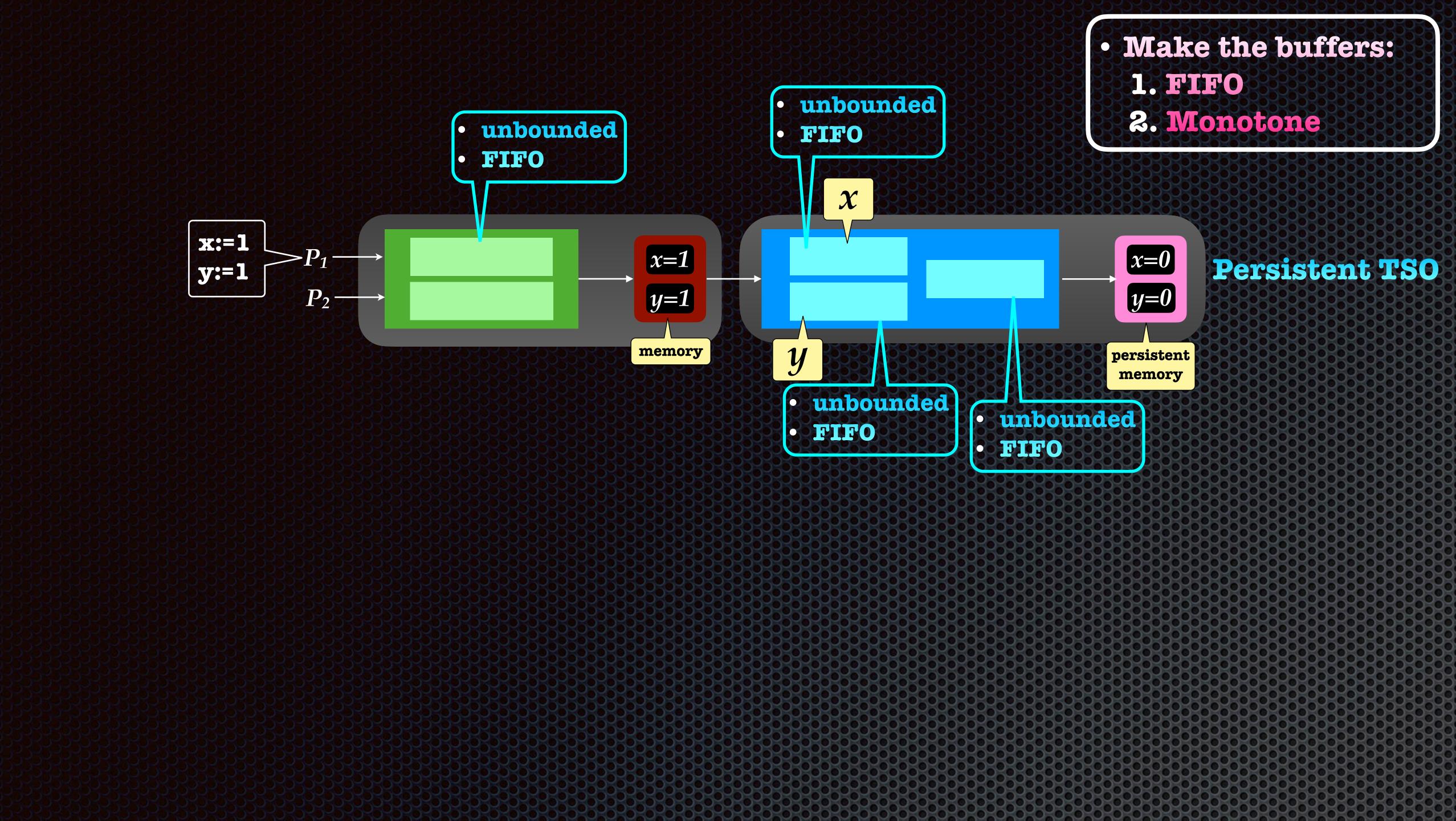


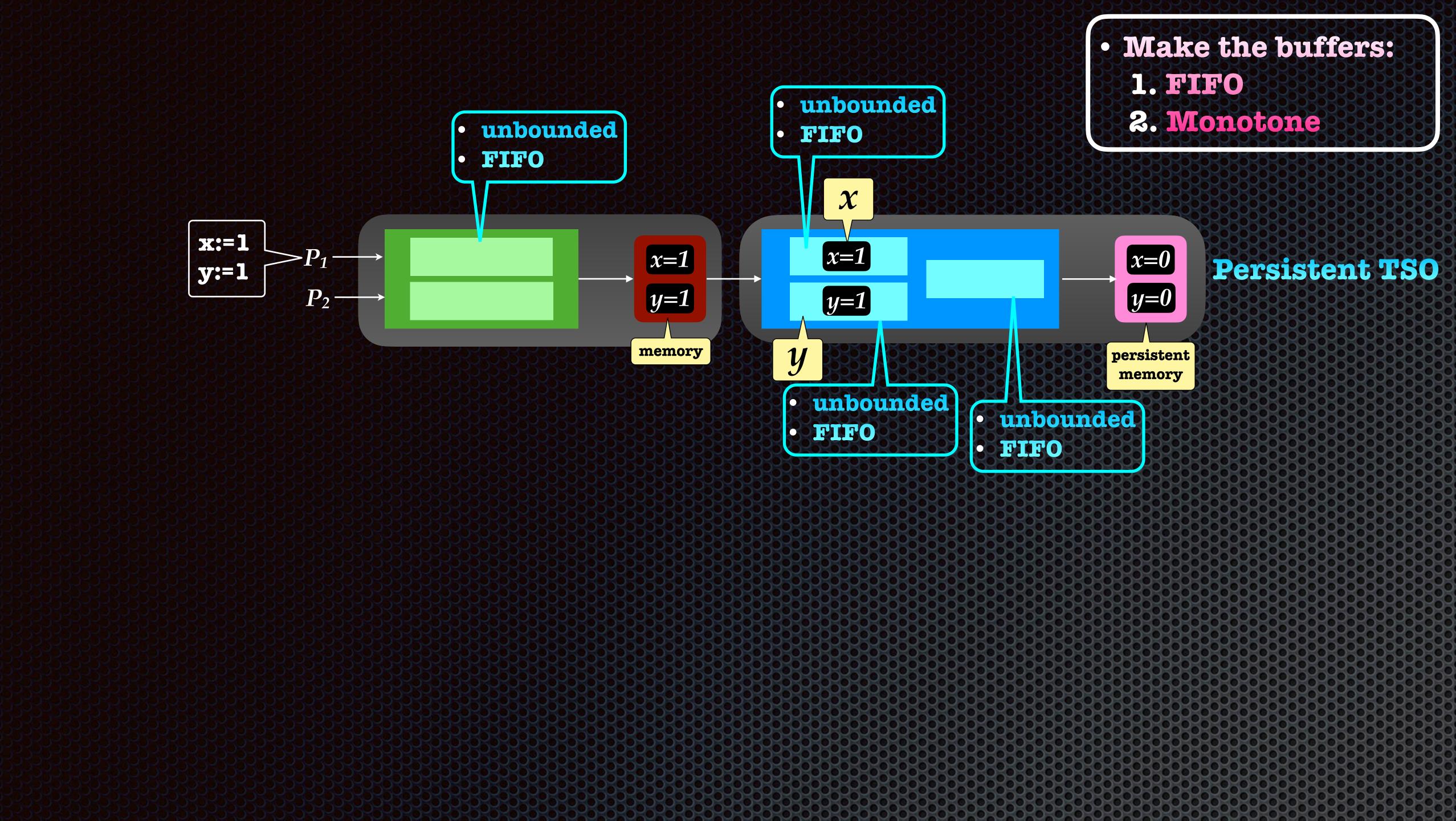


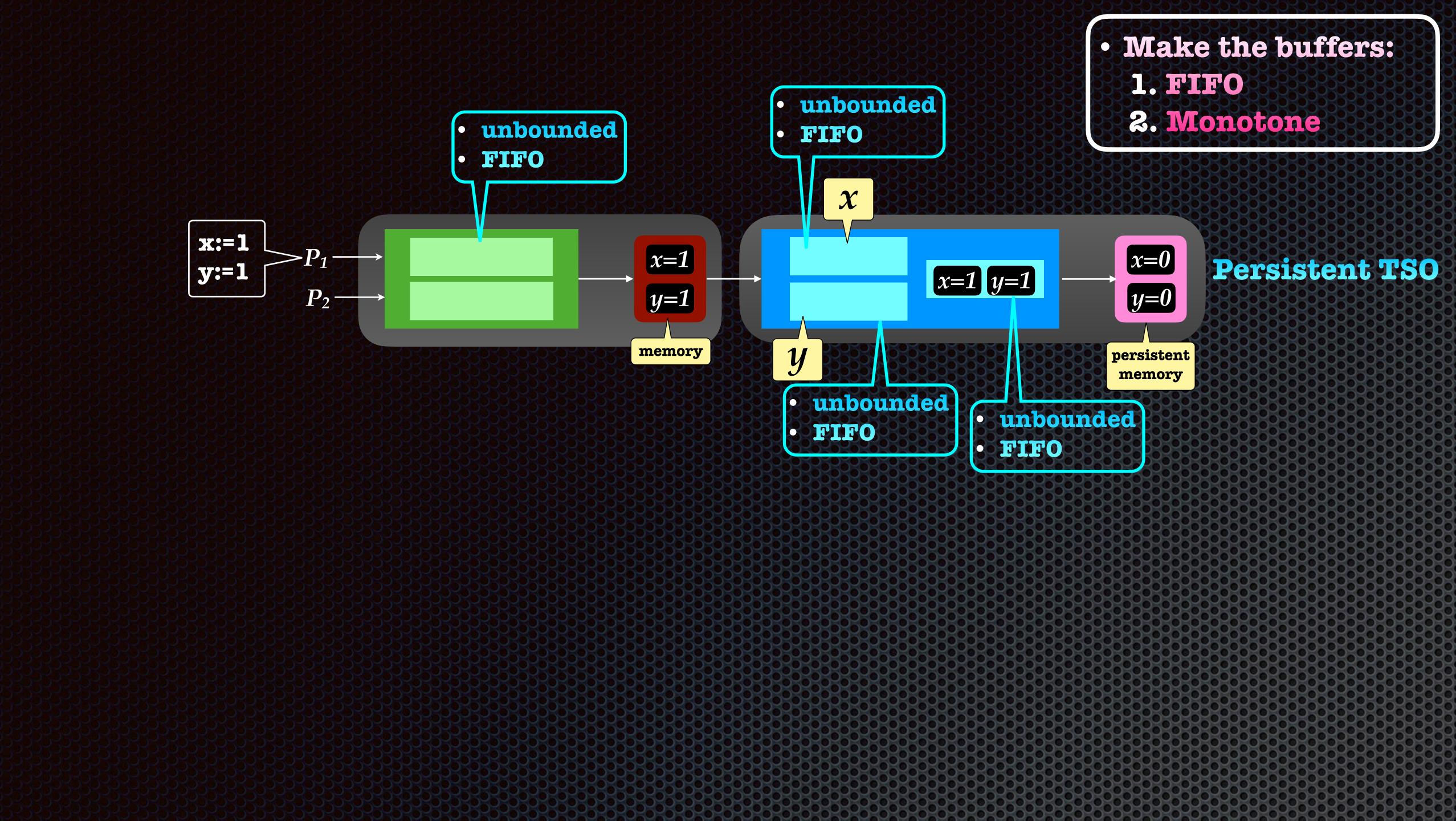


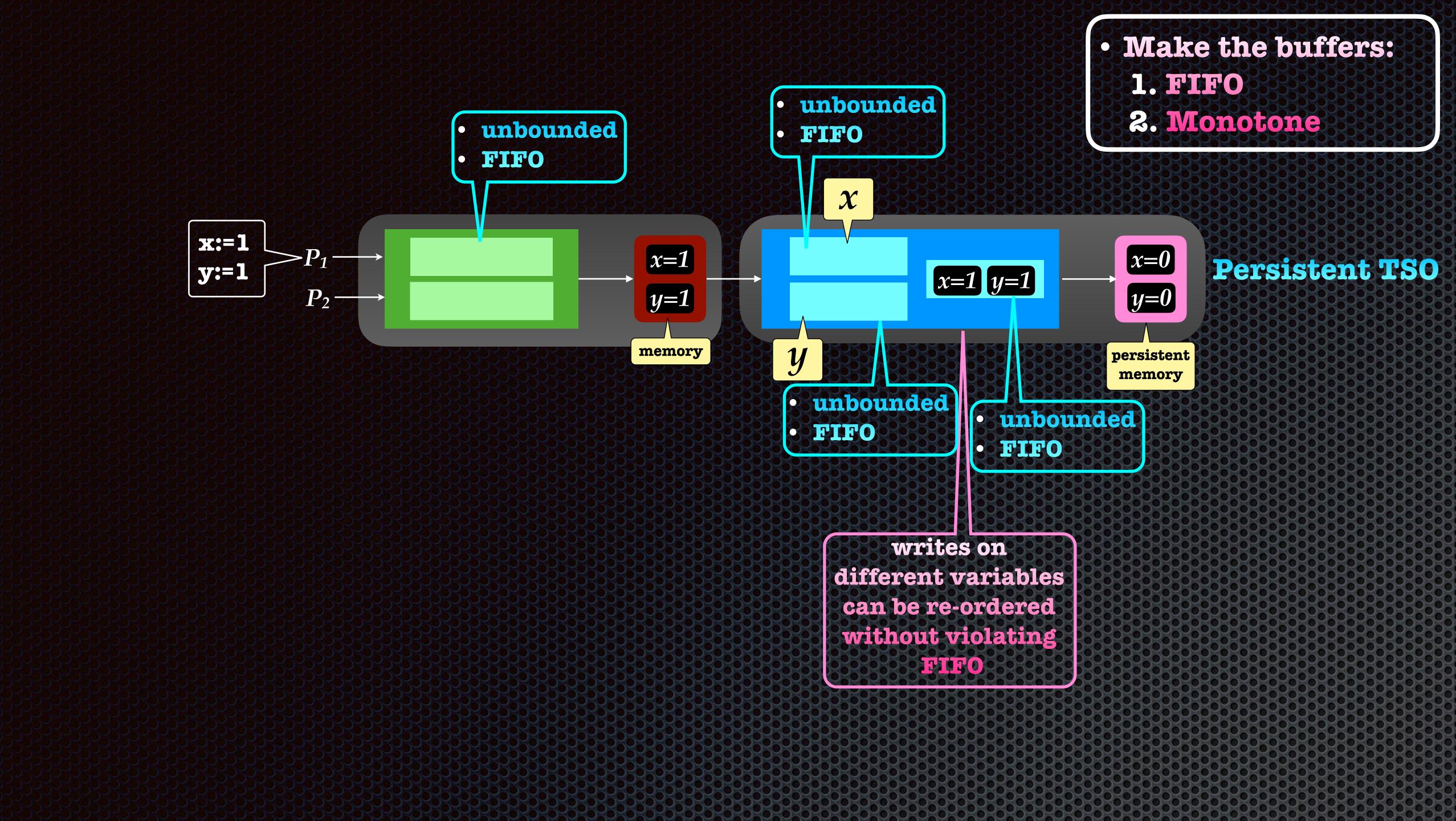


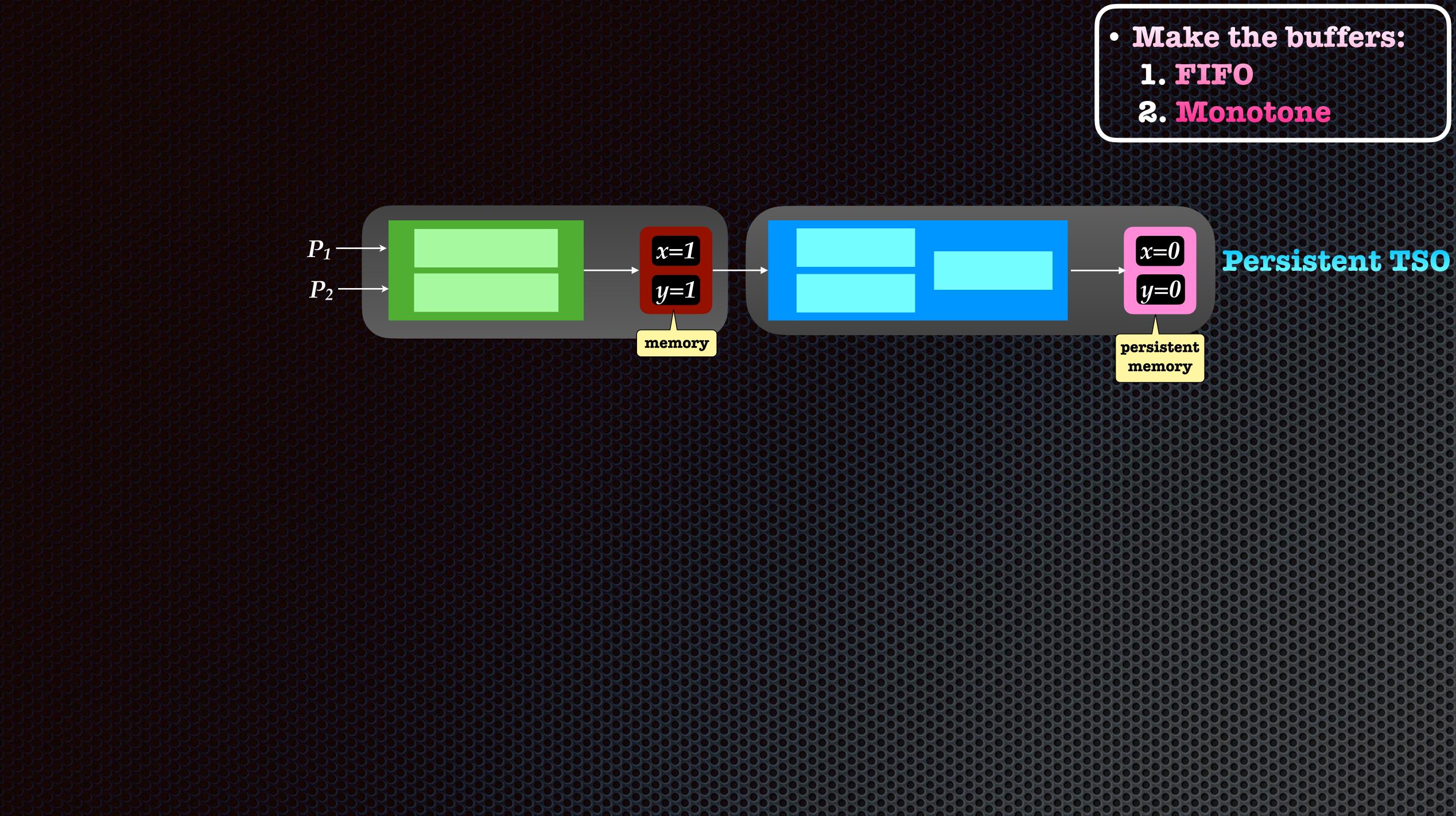






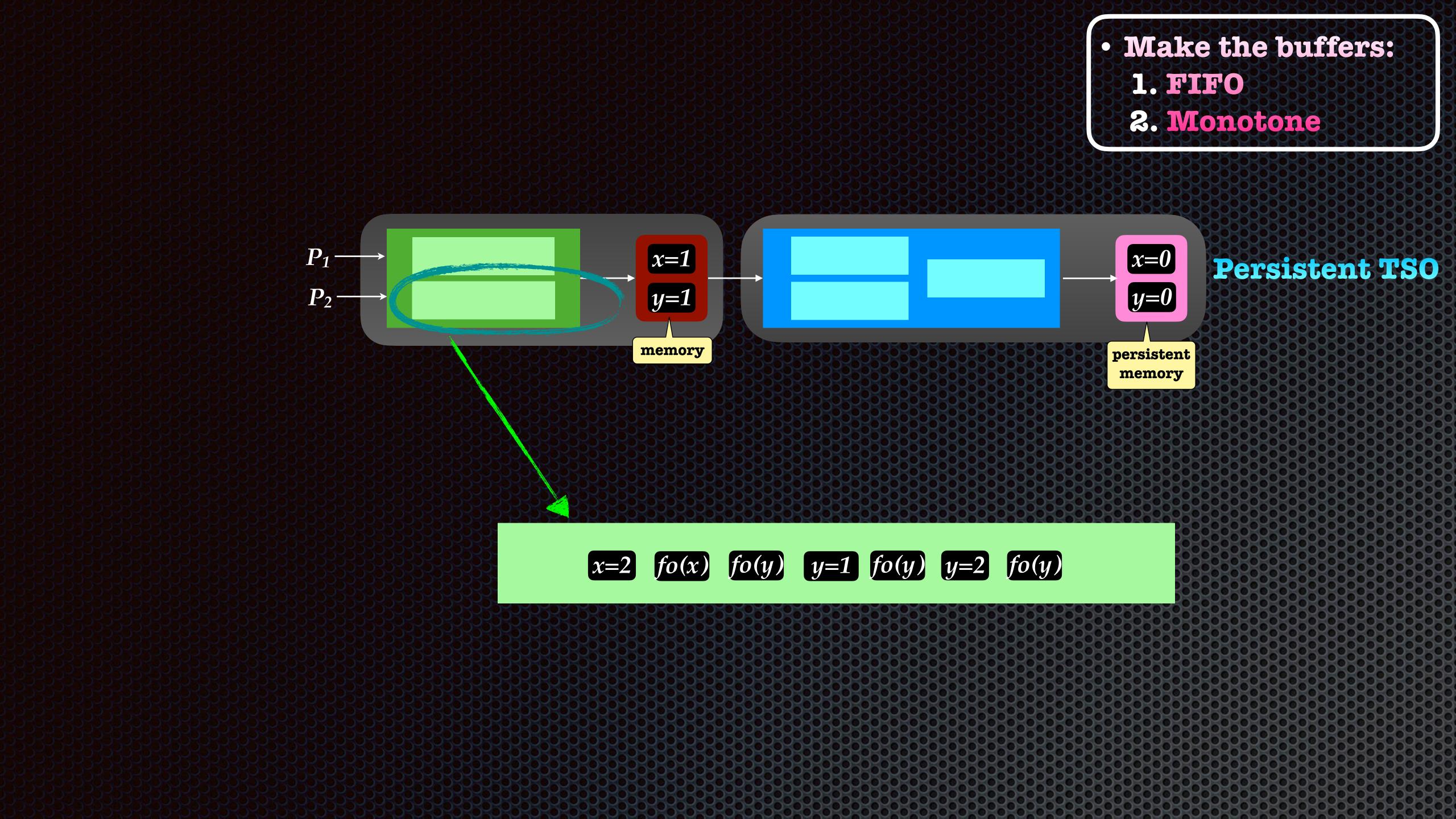


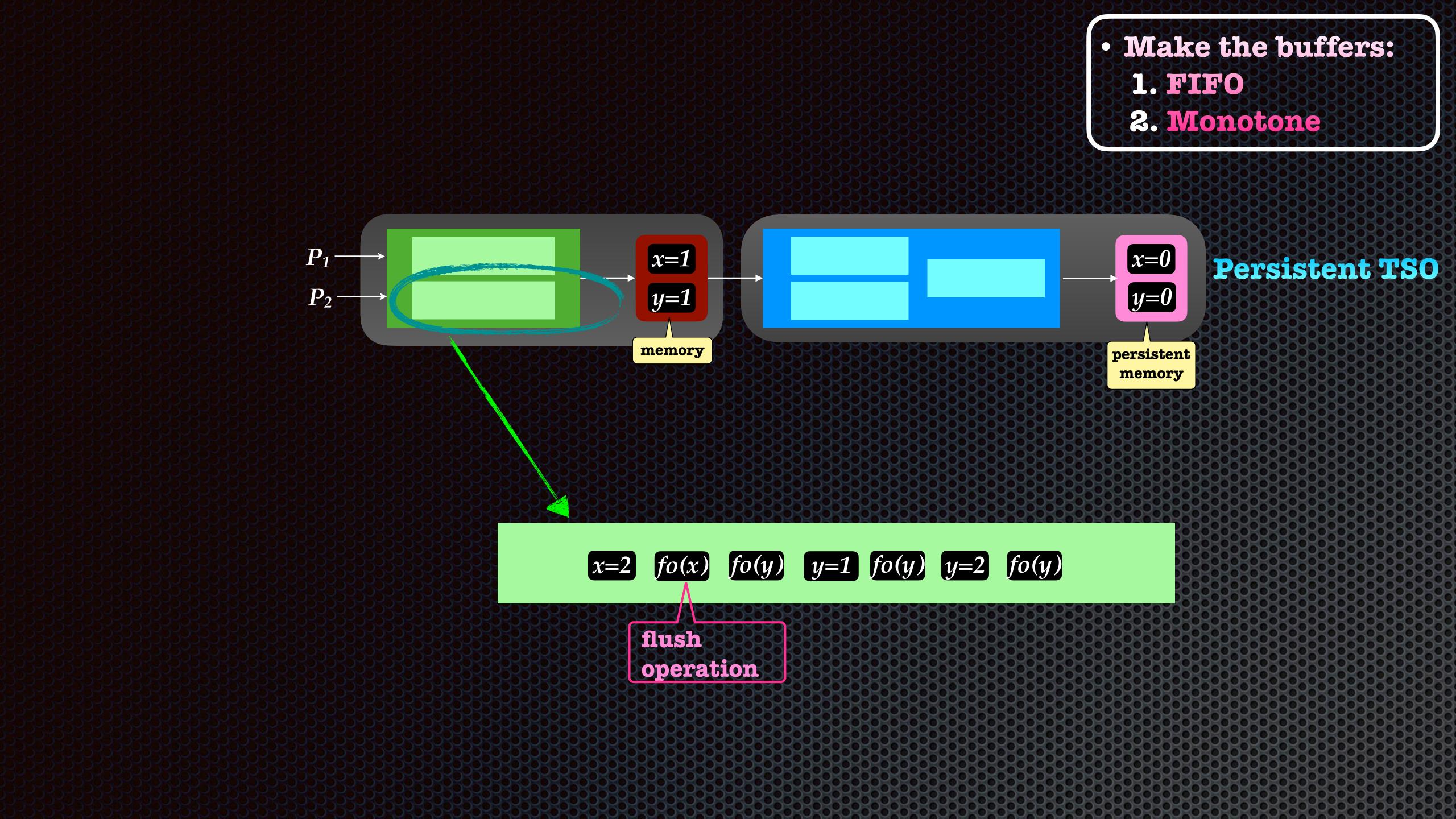


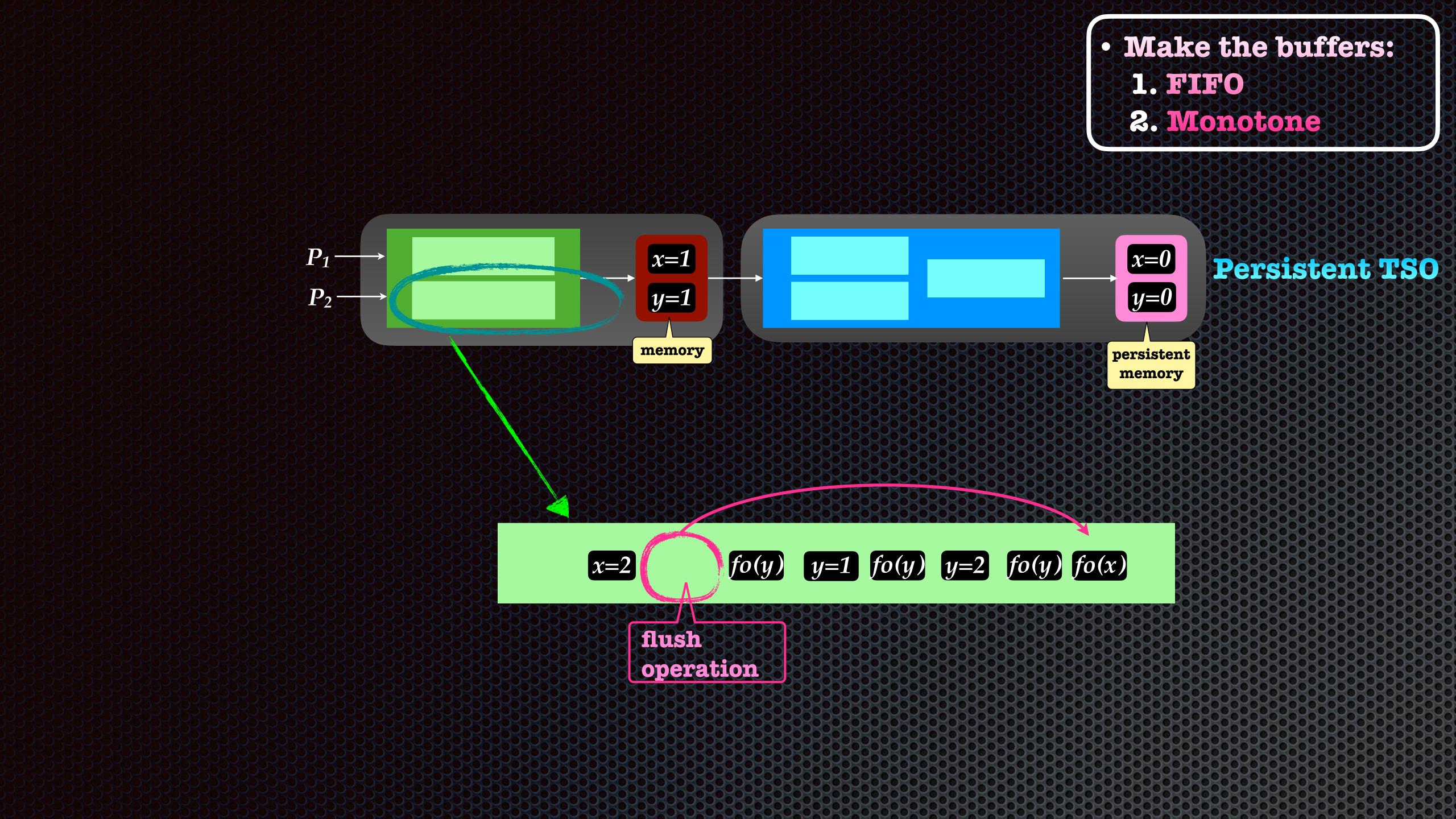


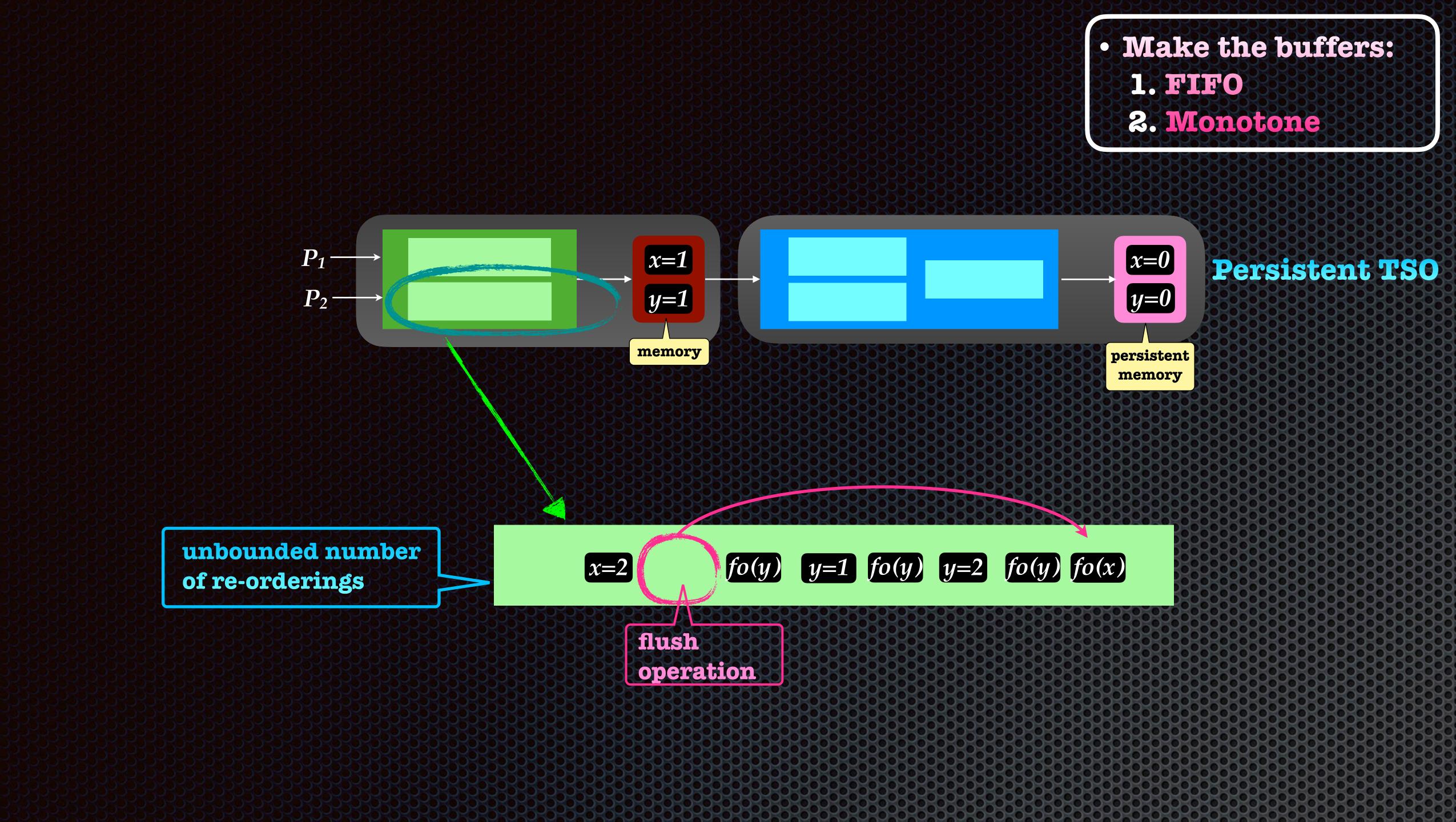


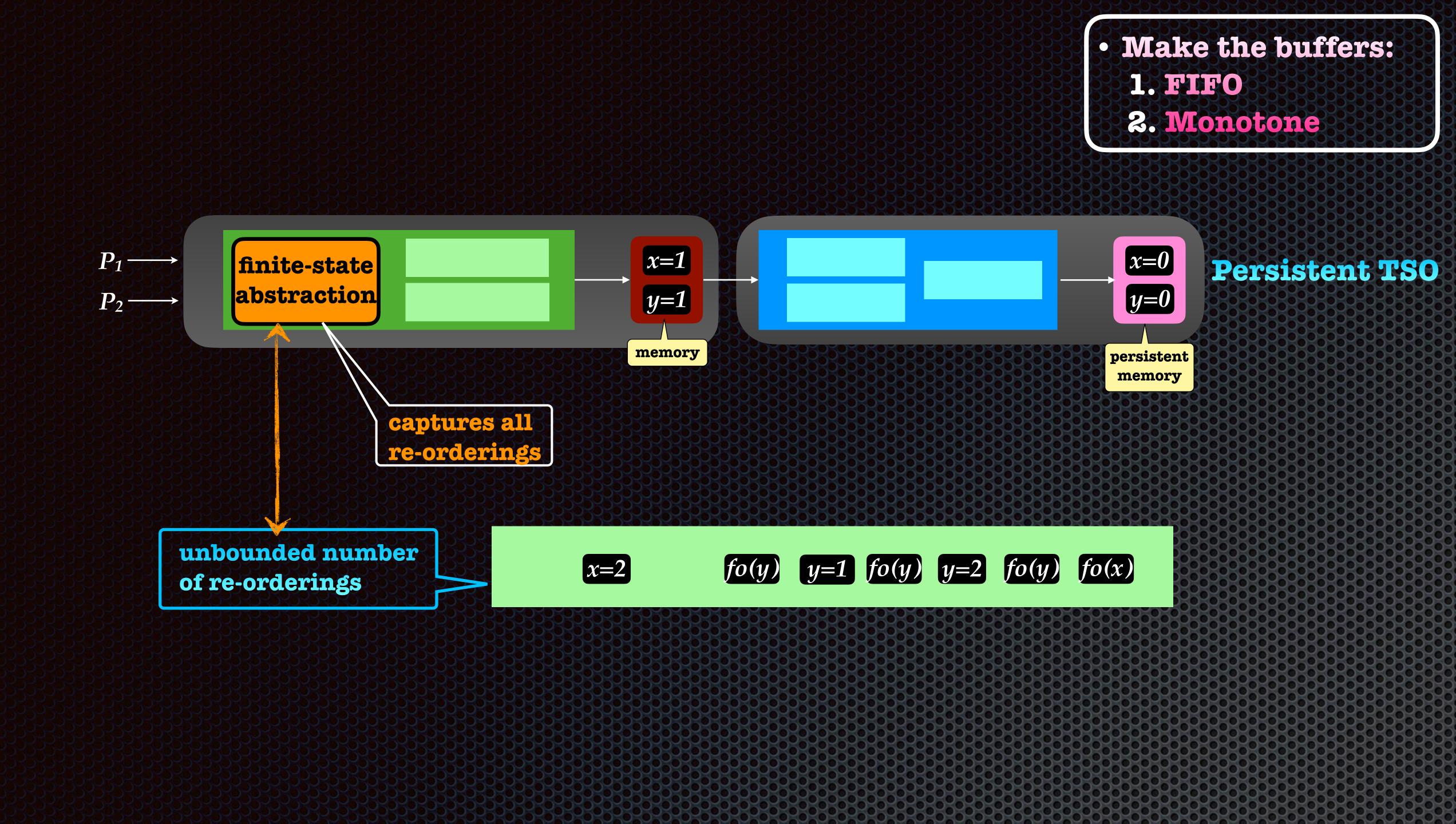


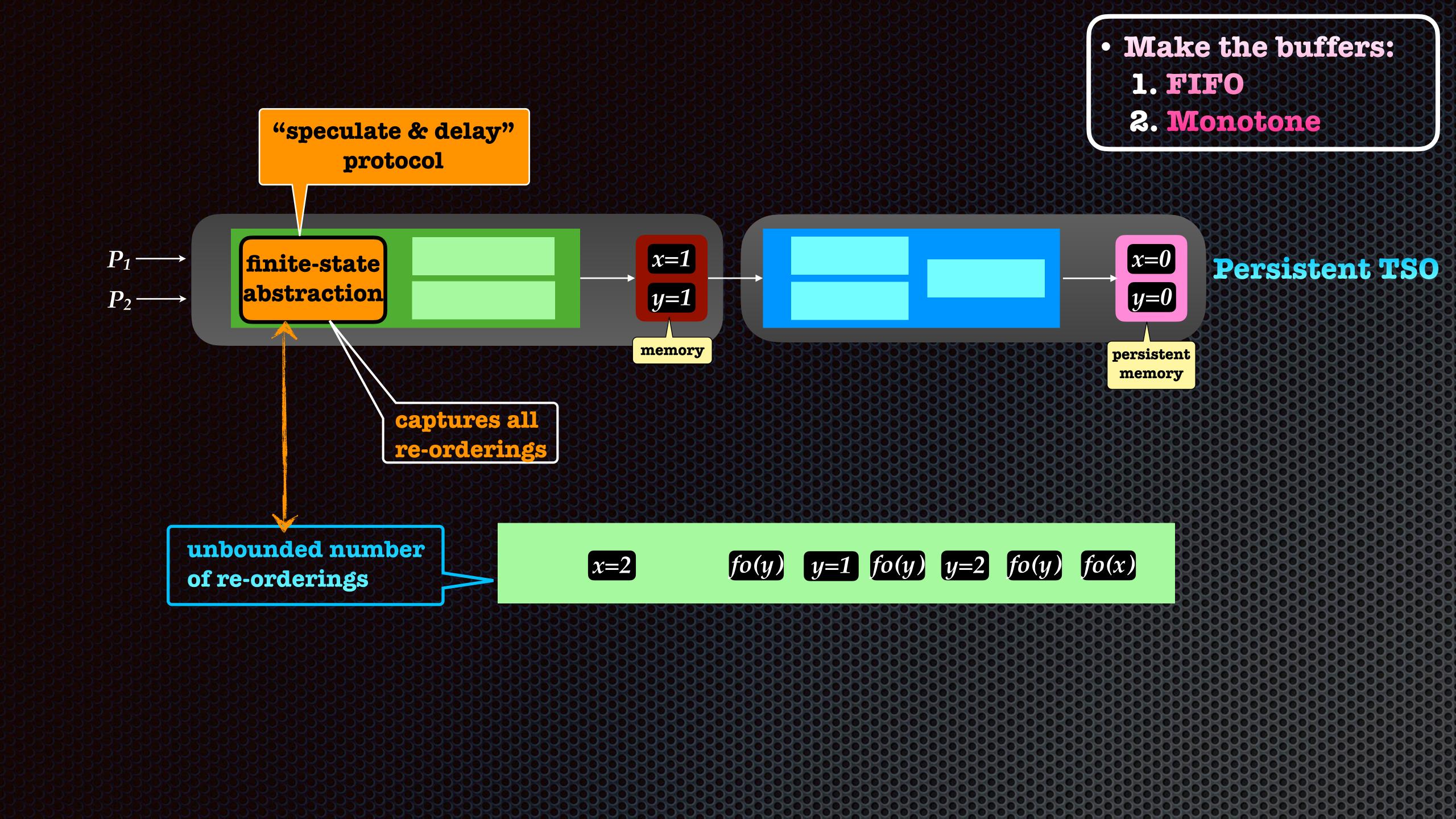


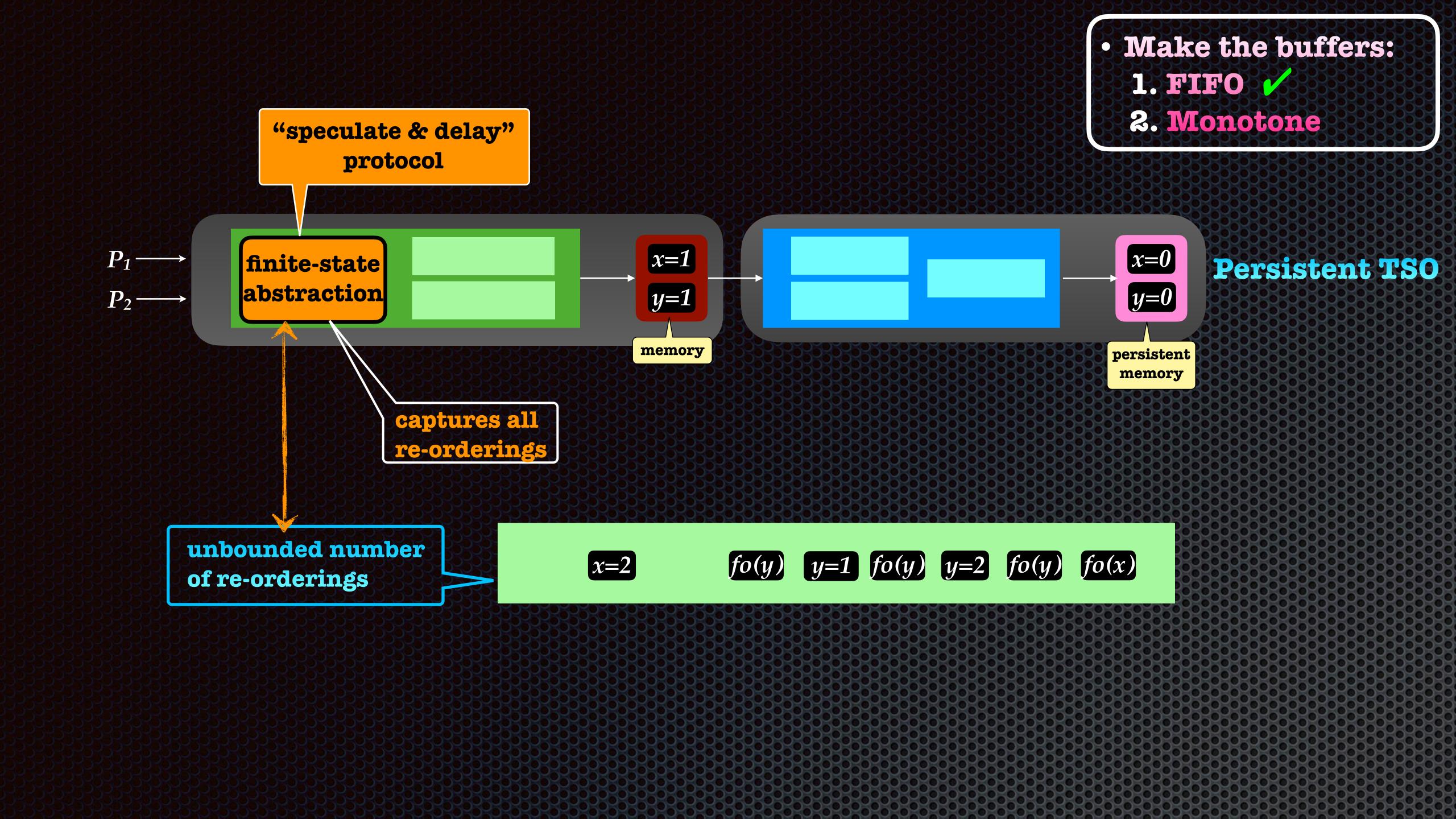


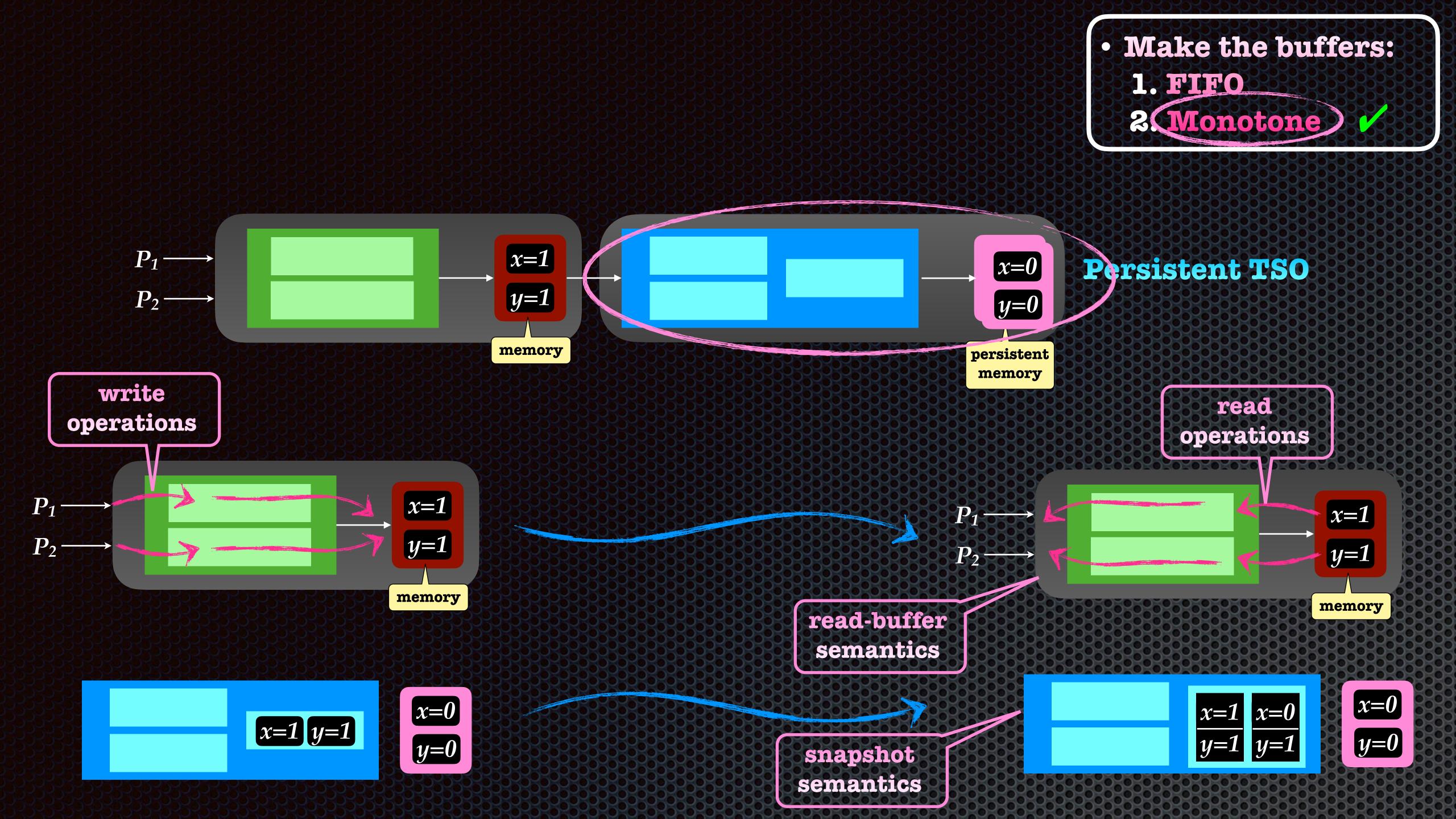






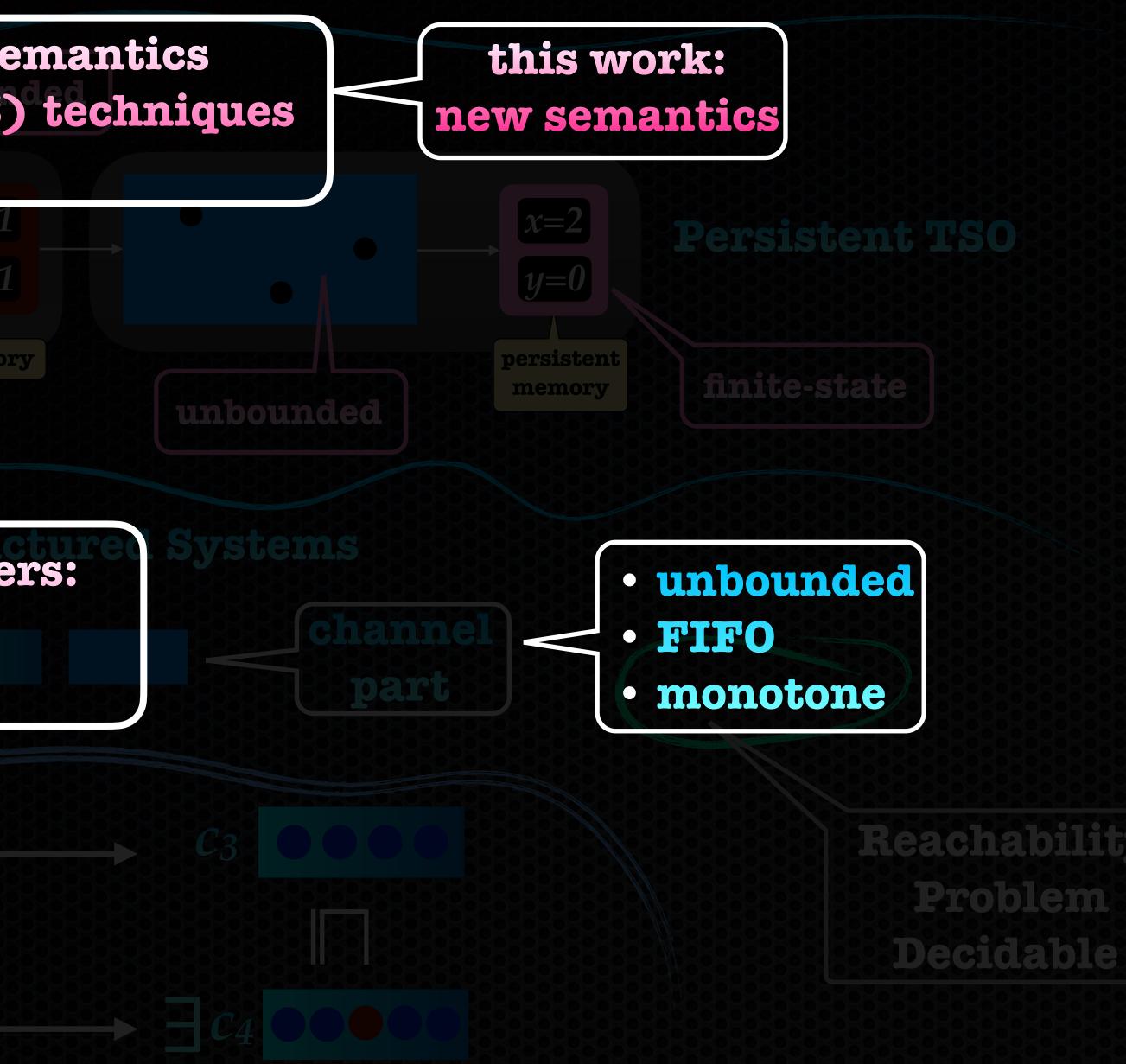






unbounded adapting SC techniques semantics decidability • Equivelant to the Raad et al semantics • Allows applying classical (SC) techniques • "Nice" datastructures process memory • Make the buffers: finite-state 1. FIFO 2. Monotone





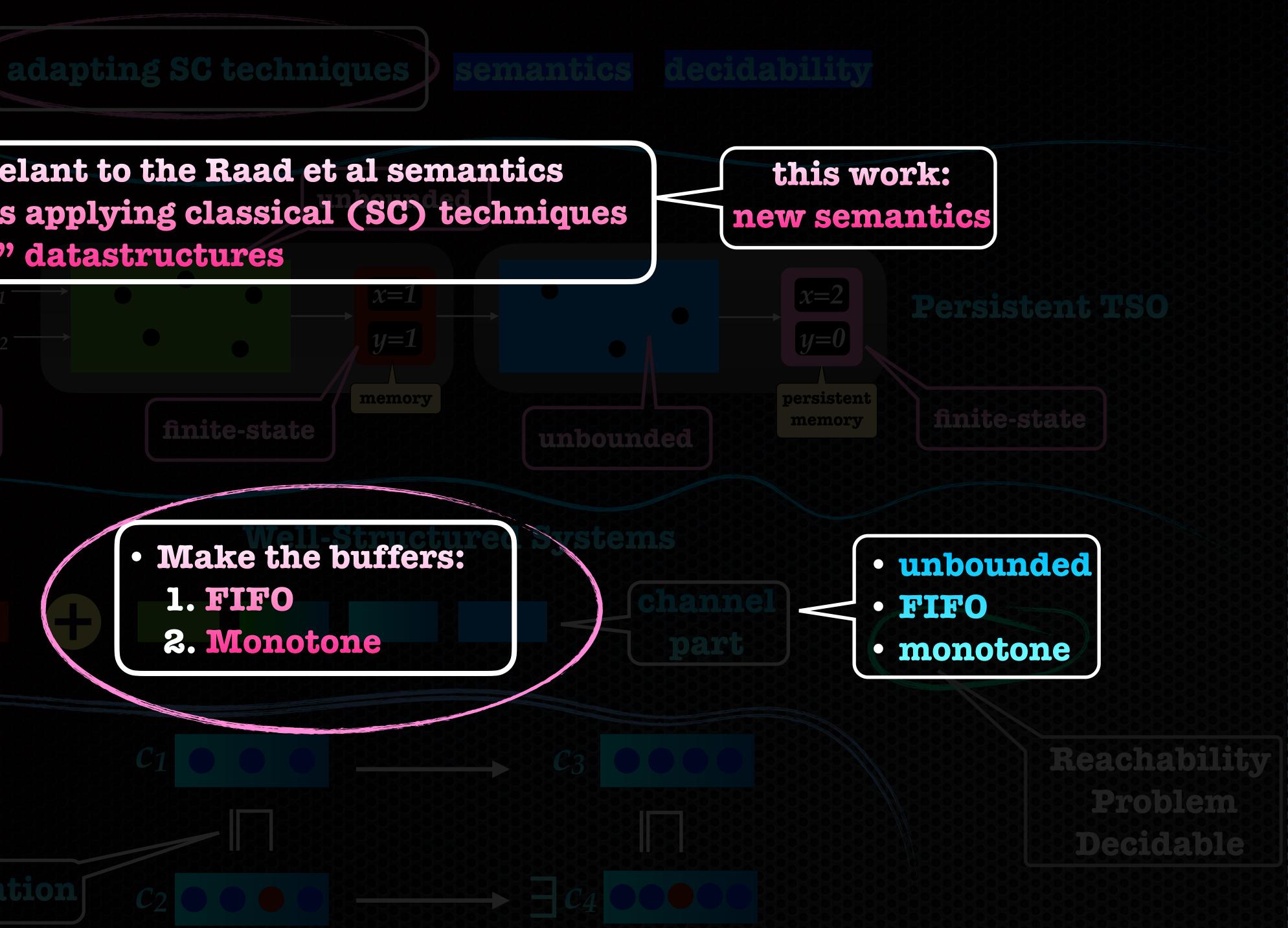


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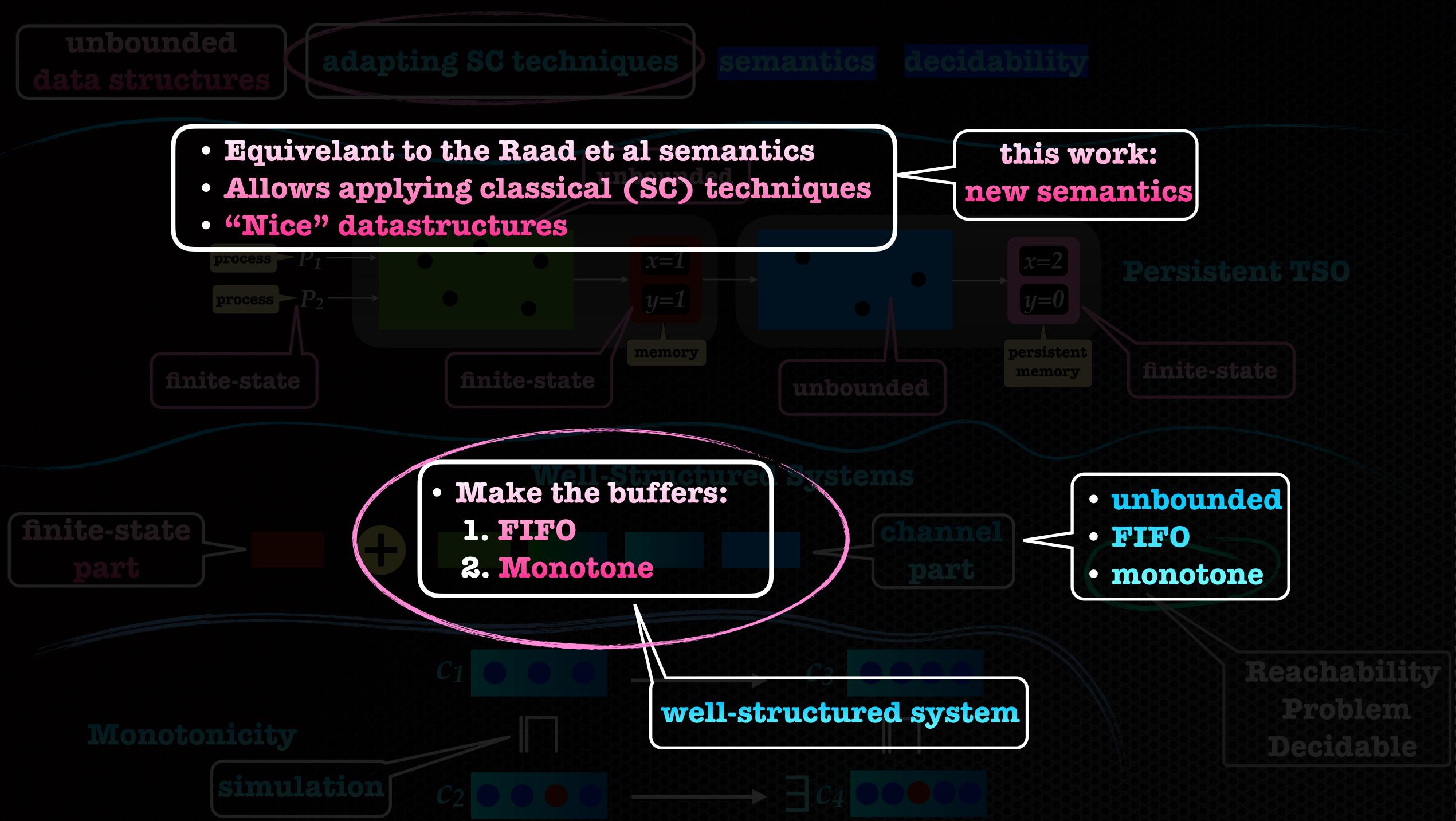
> • Make the buffers: 1. FIFO 2. Monotone

finite-state





unbounded





"solutions require interaction across reach communities"

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Persistency Semantics of the Intel-x86 Architecture

## architecture + programming languages

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architecture + programming languages

this work: programming languages + program verification

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