

Verification of Dynamic Register Automata

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Communication Protocols Analysis

Verification of Dynamic Register Automata



Verification of a class of protocols:

- ▶ **Dynamic creation** of processes
 - ▶ **Unique** ID for each process
- ▶ Finite number of **registers** per process
 - ▶ Used to store the ID of others
- ▶ **Point-to-point** communication
- ▶ **Rendez-vous** communication

Dynamic Register Automata

Verification of Dynamic Register Automata

[Bollig et al. 2010, 2013]



Dynamic Register Automata

Verification of Dynamic Register Automata



Applications

- Leader Election Protocol
- Peer To Peer Protocol
- Ad-Hoc Networks

Dynamic Register Automata

Verification of Dynamic Register Automata



Applications

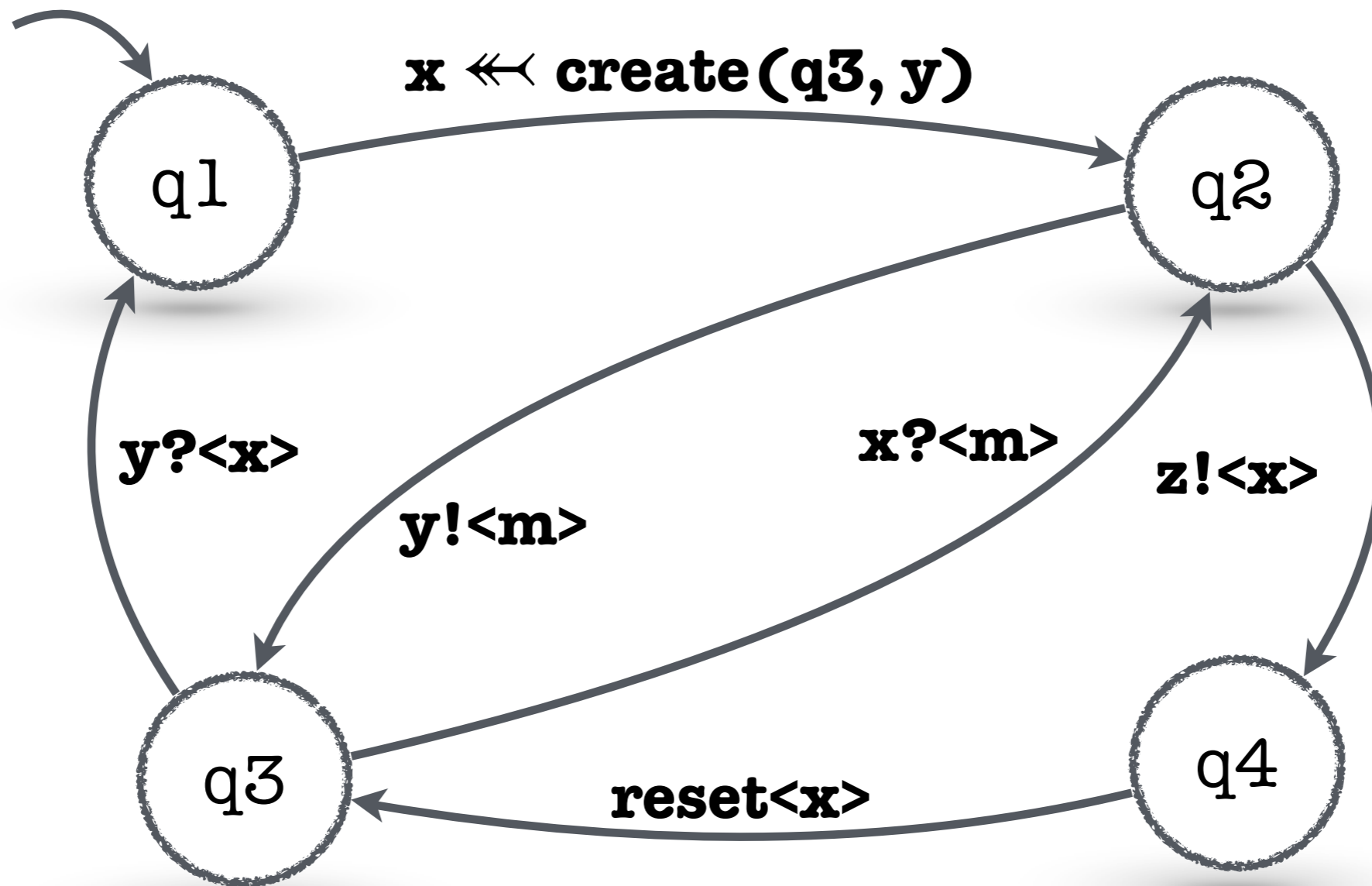
Formal Model

Dynamic Register Automata

Verification of Dynamic Register Automata

Formal Model

Process Model



Dynamic Register Automata

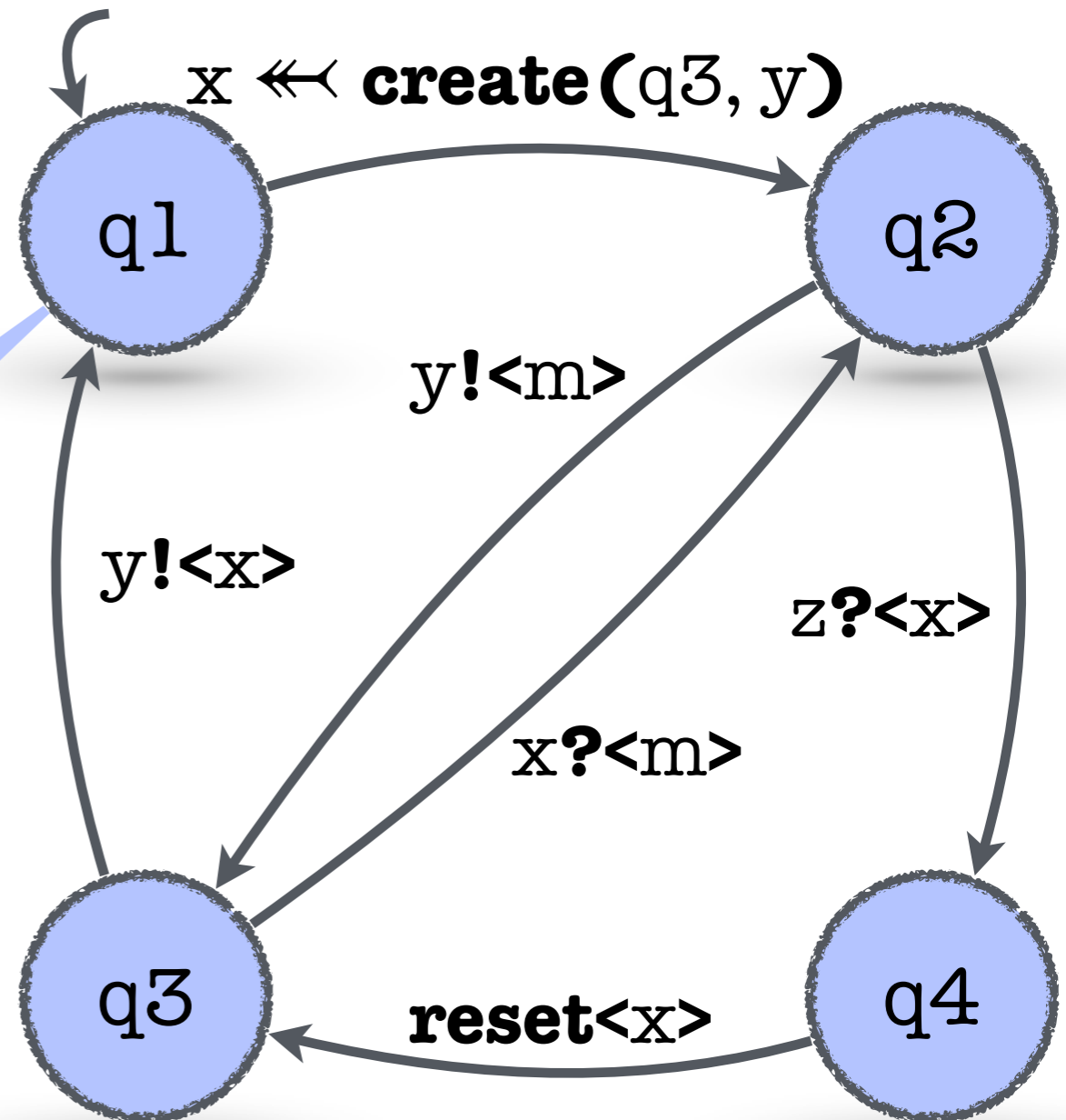
Verification of Dynamic Register Automata



Formal Model

Process Model

Finite number of States



Dynamic Register Automata

Verification of Dynamic Register Automata

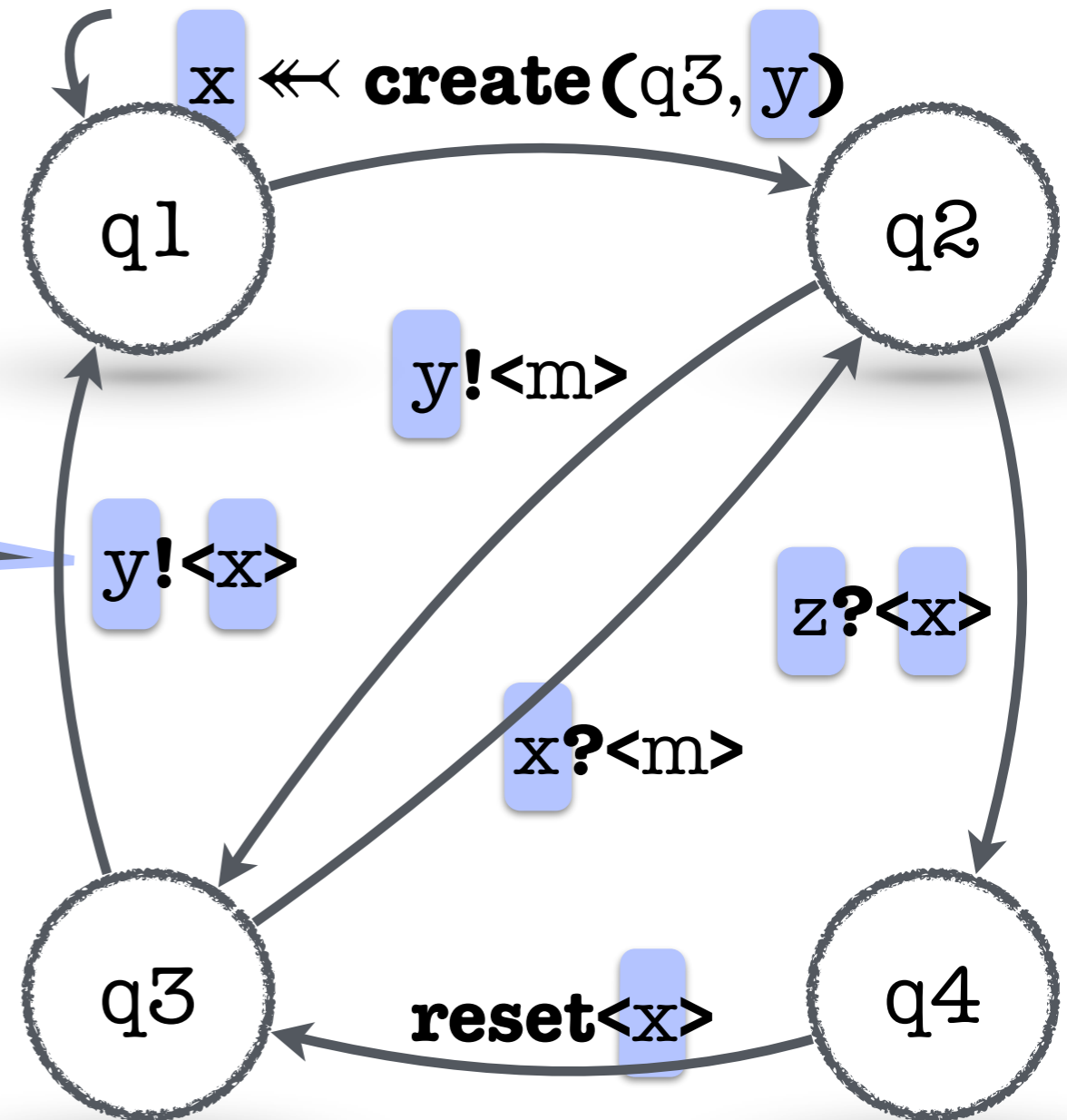


Formal Model

Process Model

Finite number of States

Finite number of Registers



Dynamic Register Automata

Verification of Dynamic Register Automata



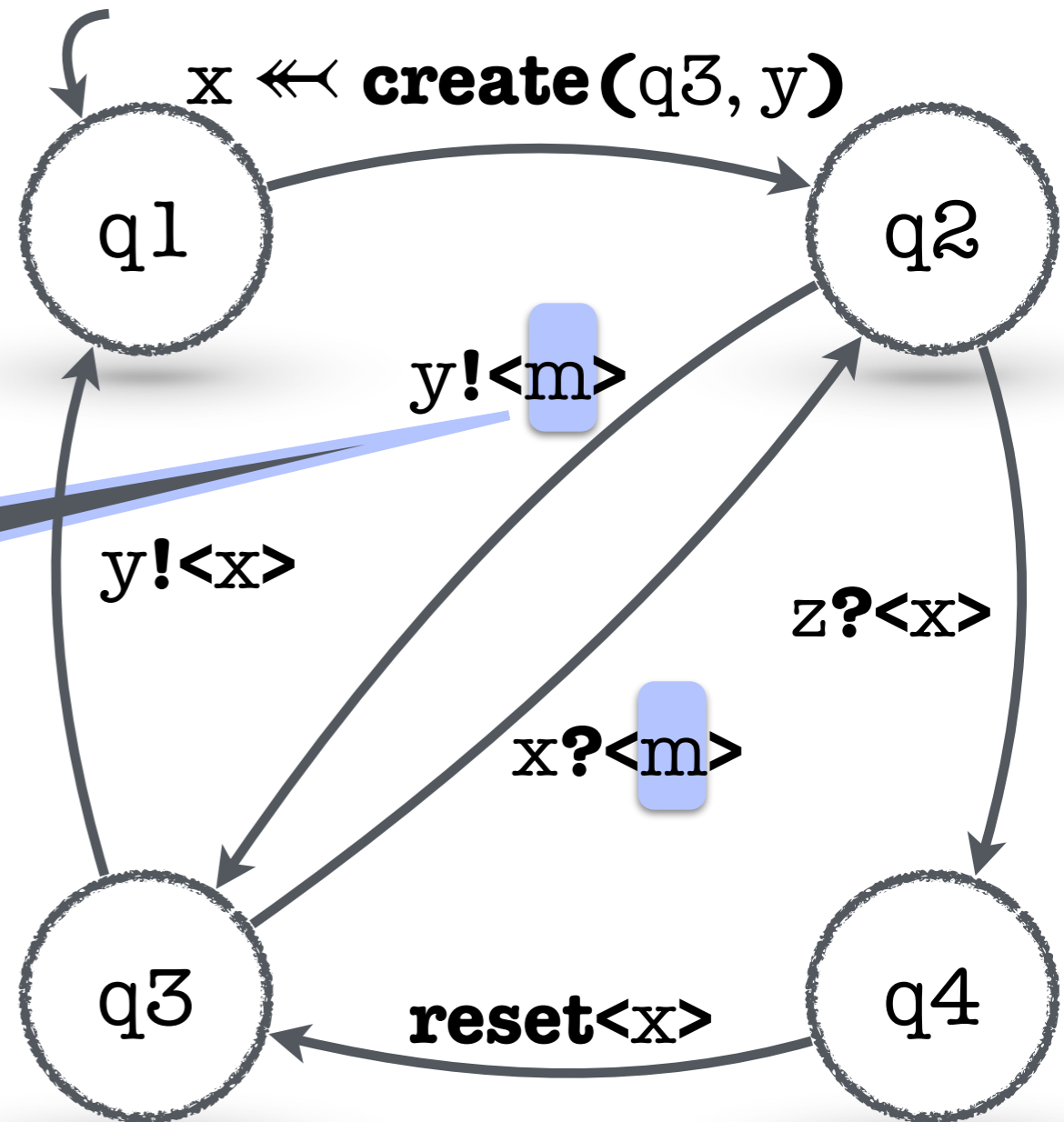
Formal Model

Process Model

Finite number of States

Finite number of Registers

Finite message alphabet



Dynamic Register Automata

Verification of Dynamic Register Automata



Formal Model

Finite number of States

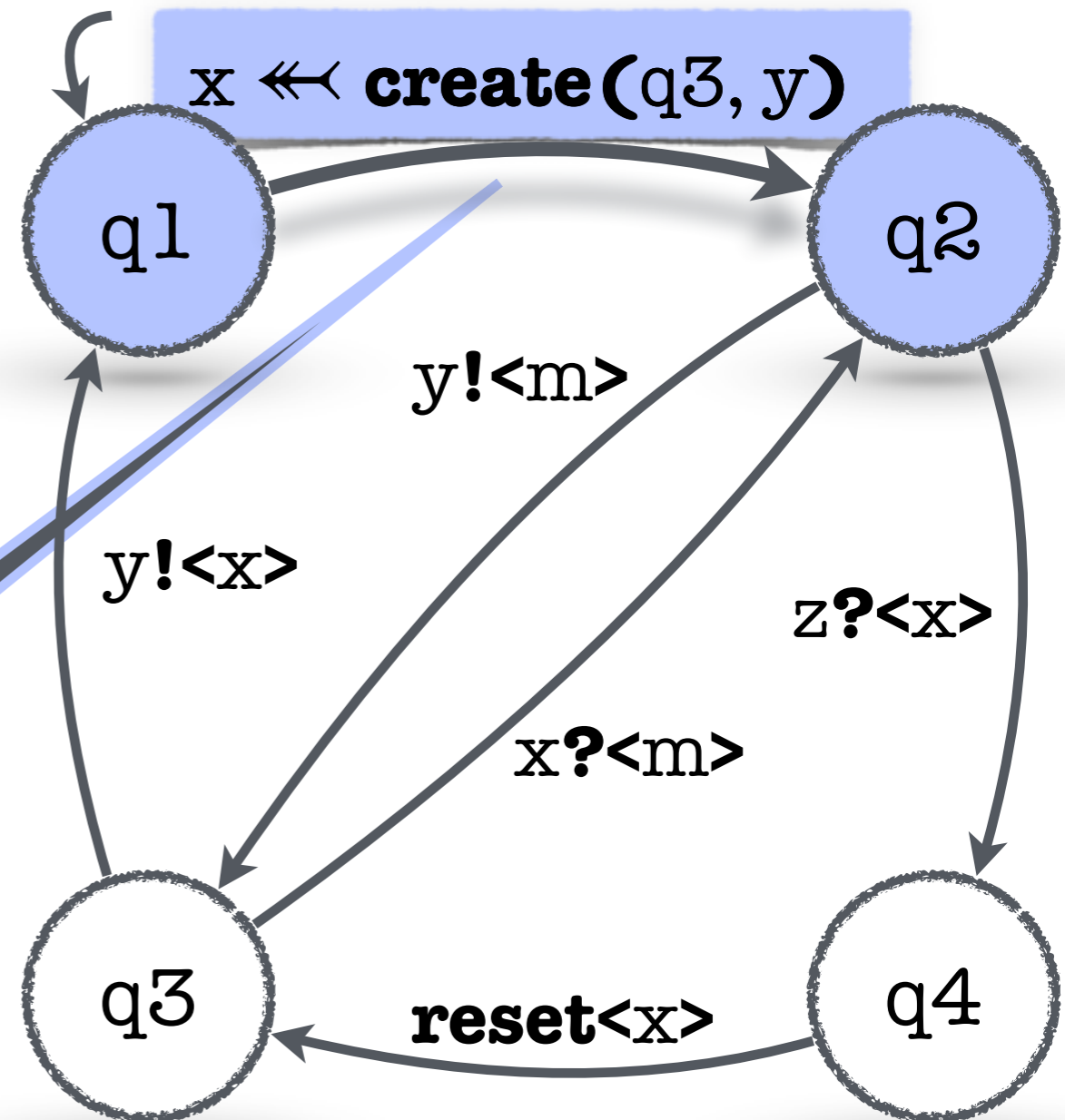
Finite number of Registers

Finite message alphabet

Transitions:

Create Process

Process Model



Dynamic Register Automata

Verification of Dynamic Register Automata



Formal Model

Finite number of States

Finite number of Registers

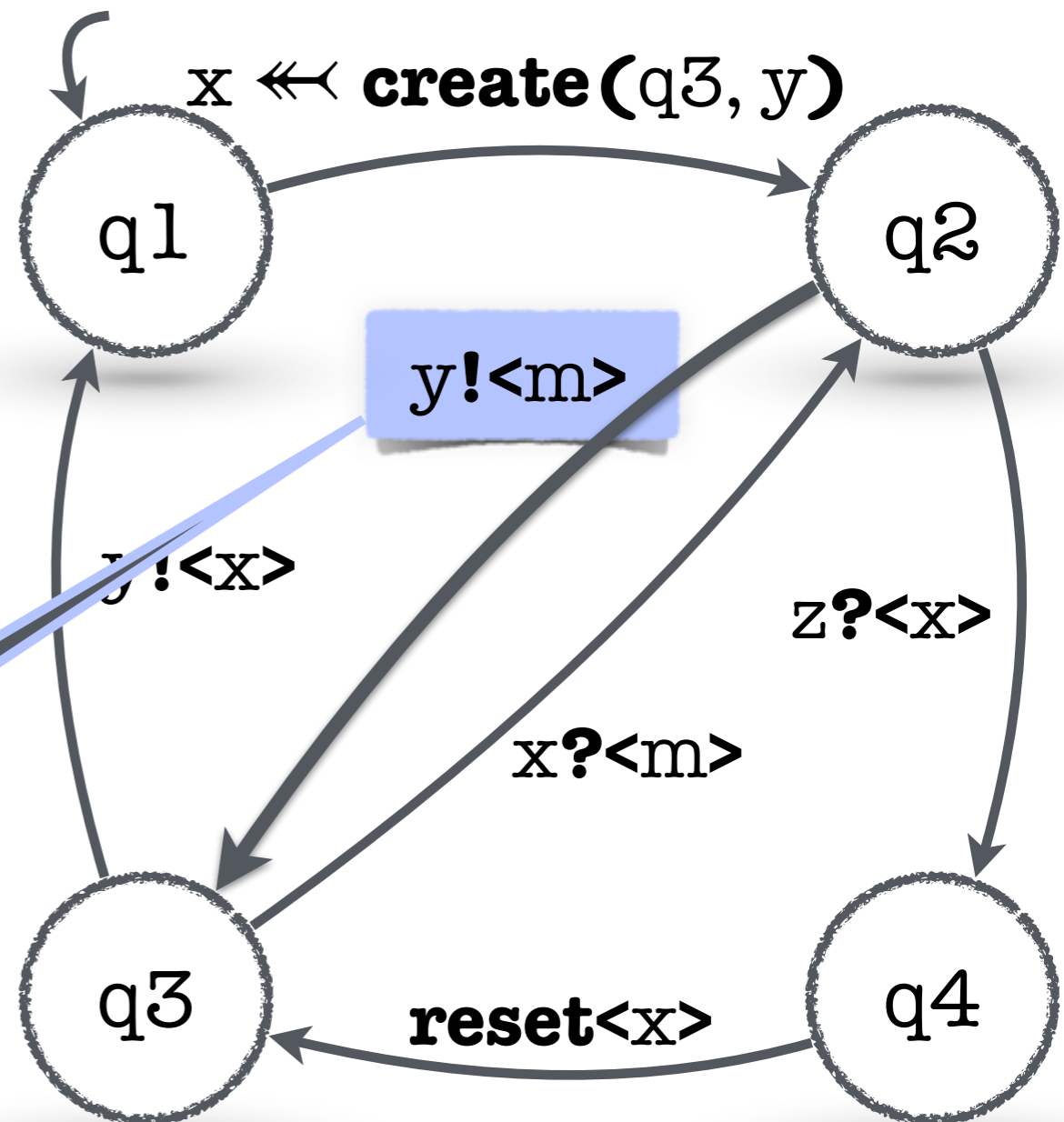
Finite message alphabet

Transitions:

Create Process

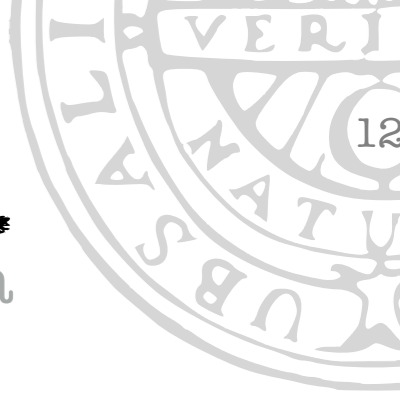
Send Message

Process Model



Dynamic Register Automata

Verification of Dynamic Register Automata



Formal Model

Finite number of States

Finite number of Registers

Finite message alphabet

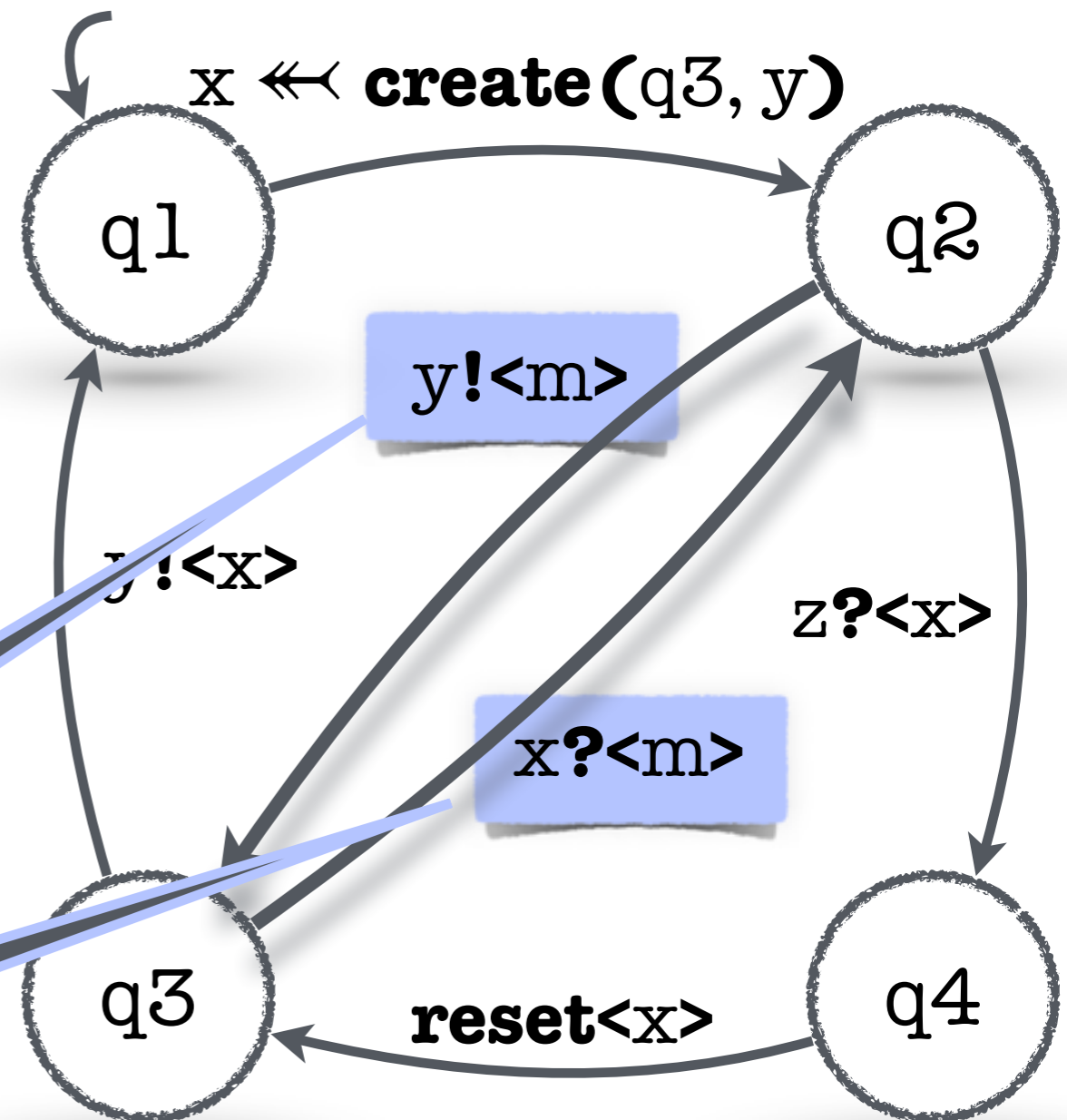
Transitions:

Create Process

Send Message

Receive Message

Process Model



Dynamic Register Automata

Verification of Dynamic Register Automata



Formal Model

Finite number of States

Finite number of Registers

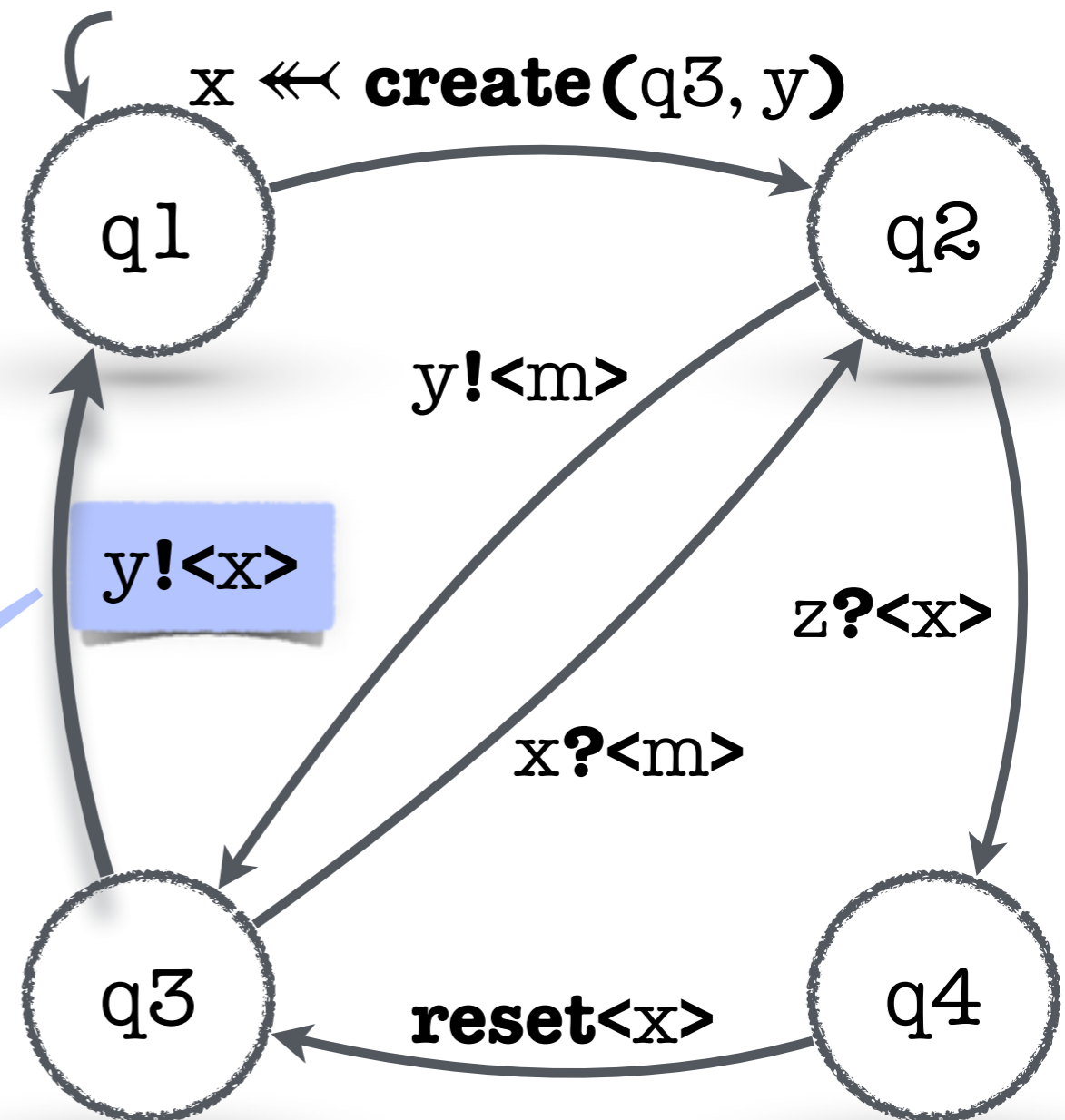
Finite message alphabet

Transitions:

Create Process

Send ID

Process Model



Dynamic Register Automata

Verification of Dynamic Register Automata



Formal Model

Finite number of States

Finite number of Registers

Finite message alphabet

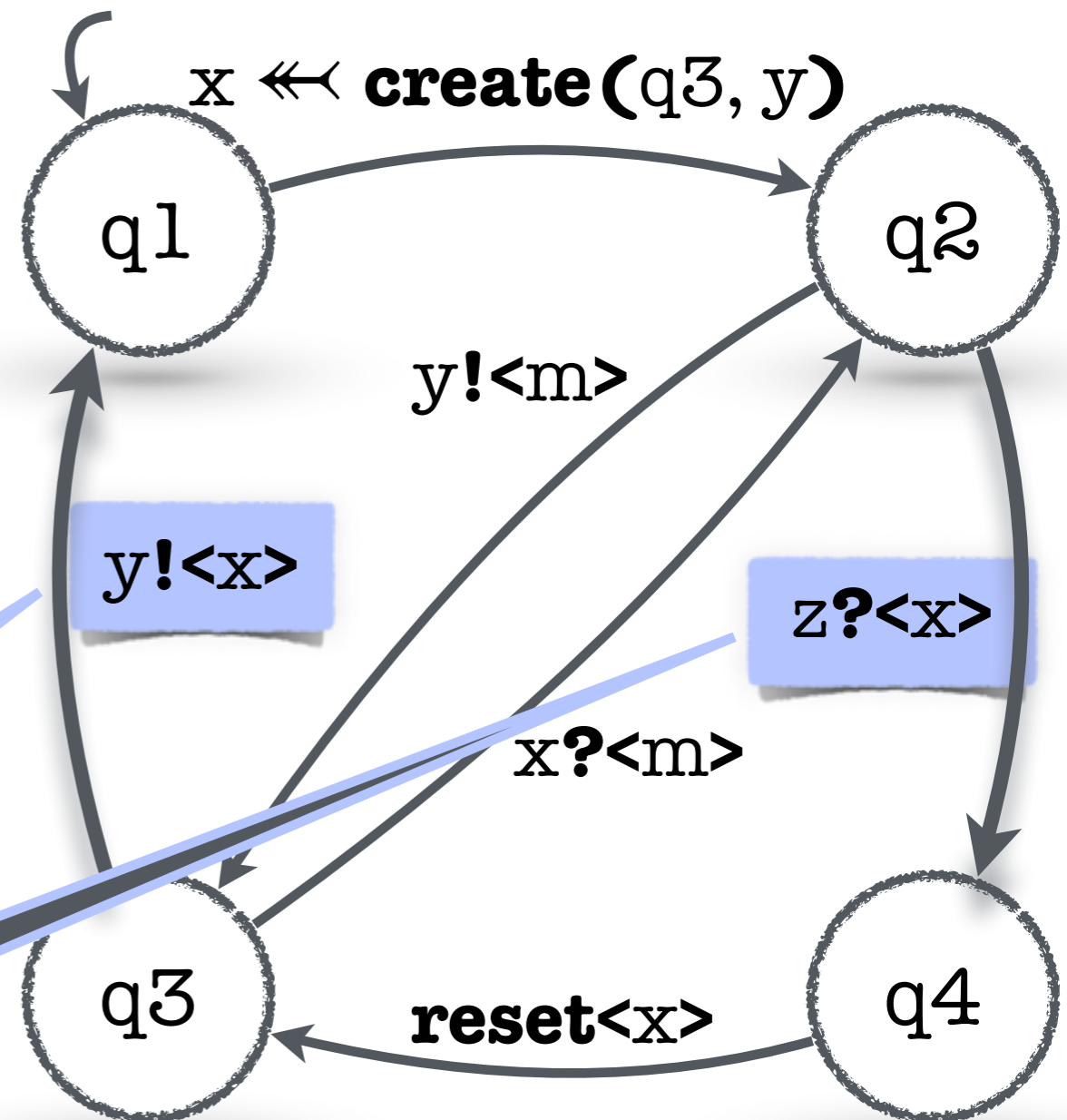
Transitions:

Create Process

Send ID

Receive ID

Process Model



Dynamic Register Automata

Verification of Dynamic Register Automata



Formal Model

Finite number of States

Finite number of Registers

Finite message alphabet

Transitions:

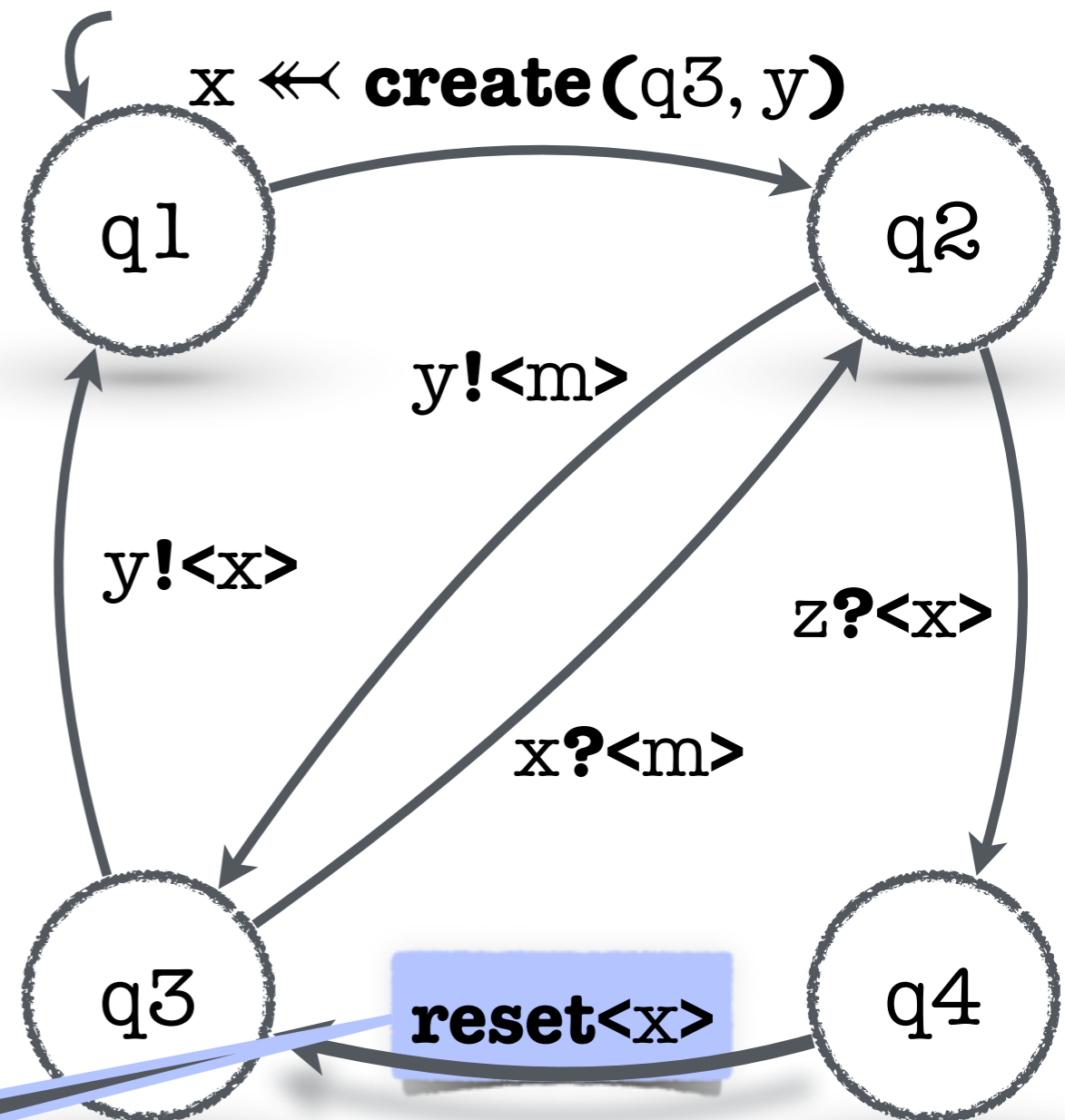
Create Process

Send Msg / ID

Receive Msg / ID

Register Reset

Process Model



Dynamic Register Automata

Verification of Dynamic Register Automata



Formal Model

Finite number of States

Finite number of Registers

Finite message alphabet

Transitions:

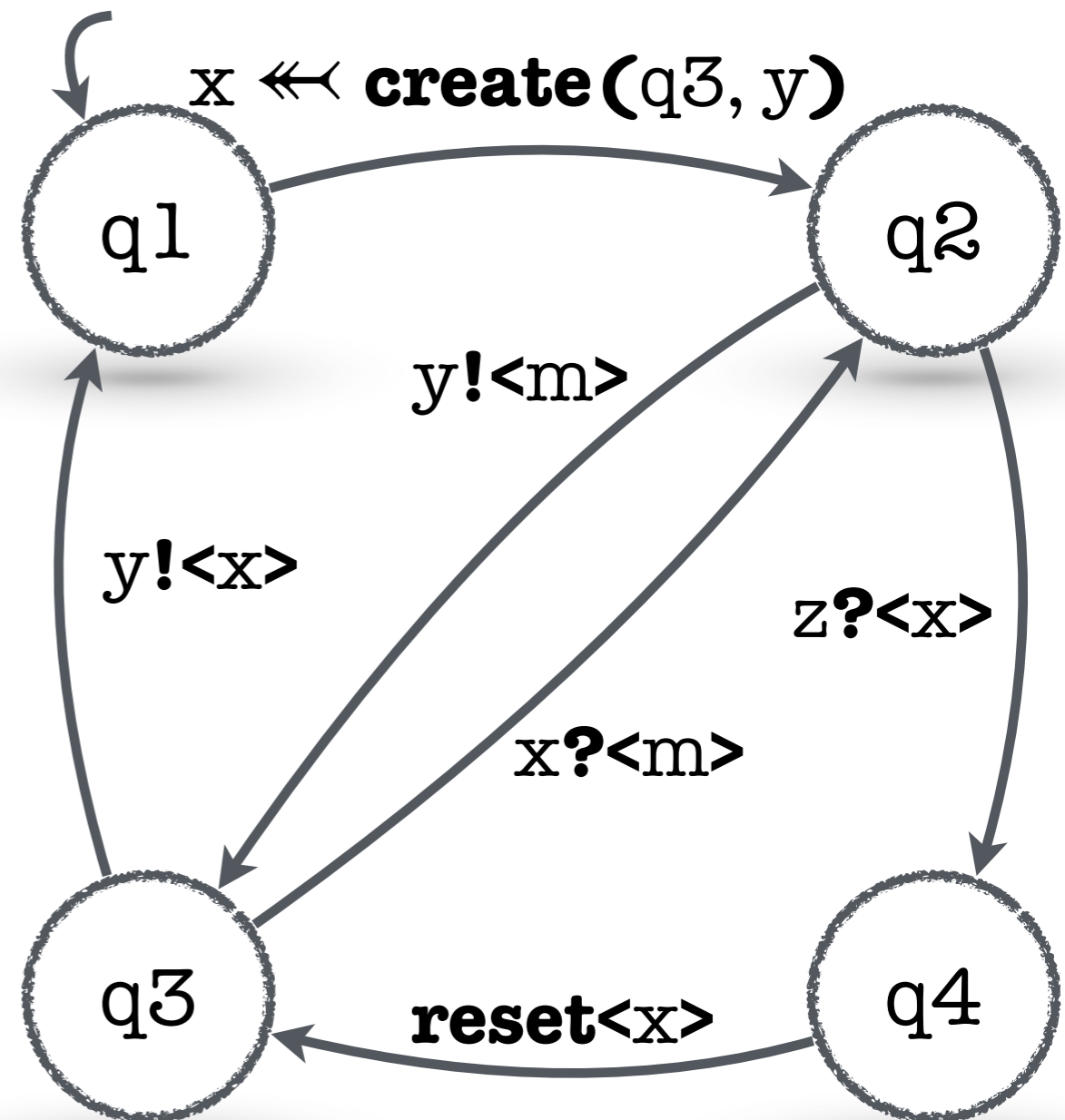
Create Process

Send Msg / ID

Receive Msg / ID

Register Reset

Process Model

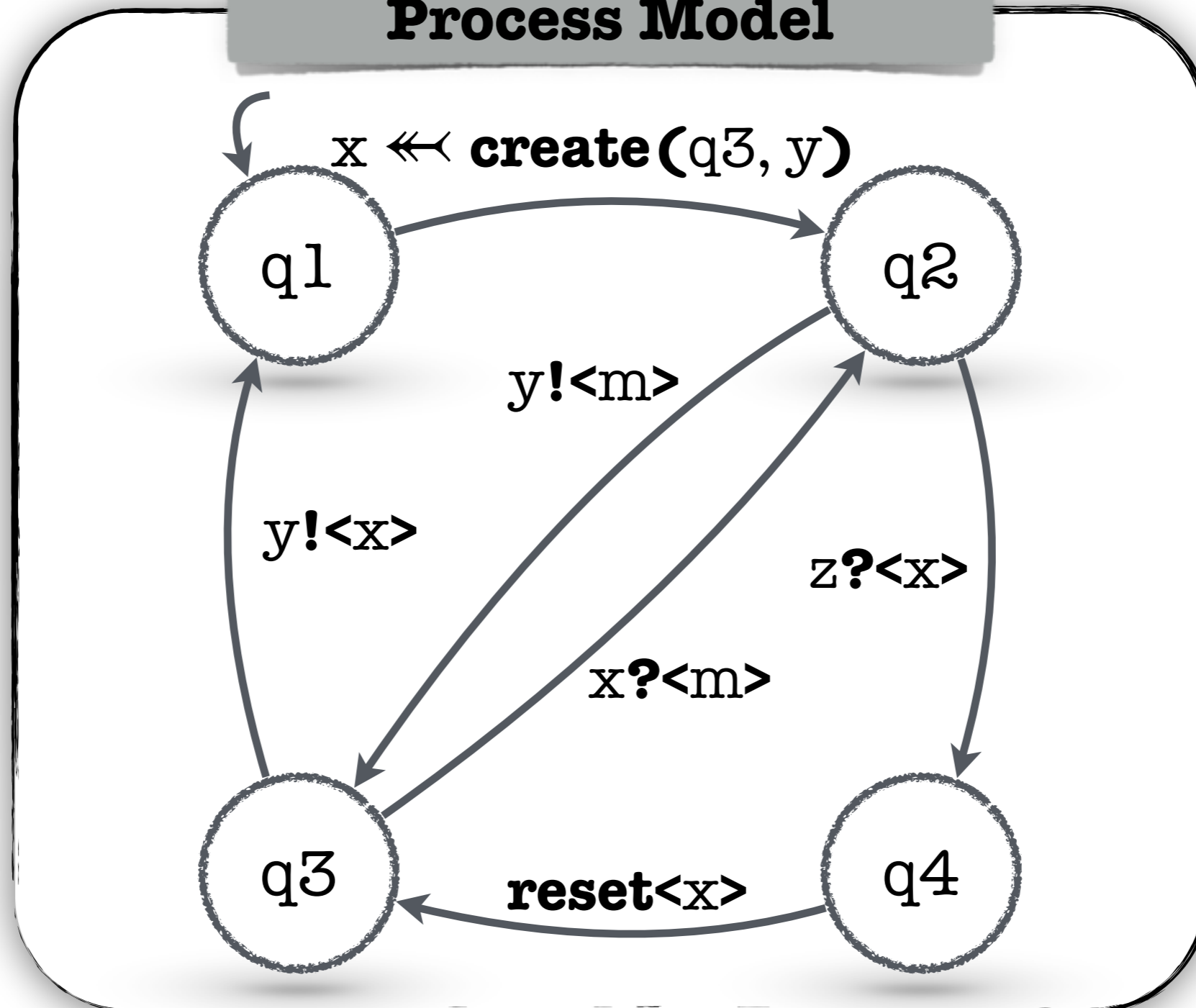


Dynamic Register Automata

Verification of Dynamic Register Automata

Formal Model

Process Model



Dynamic Register Automata

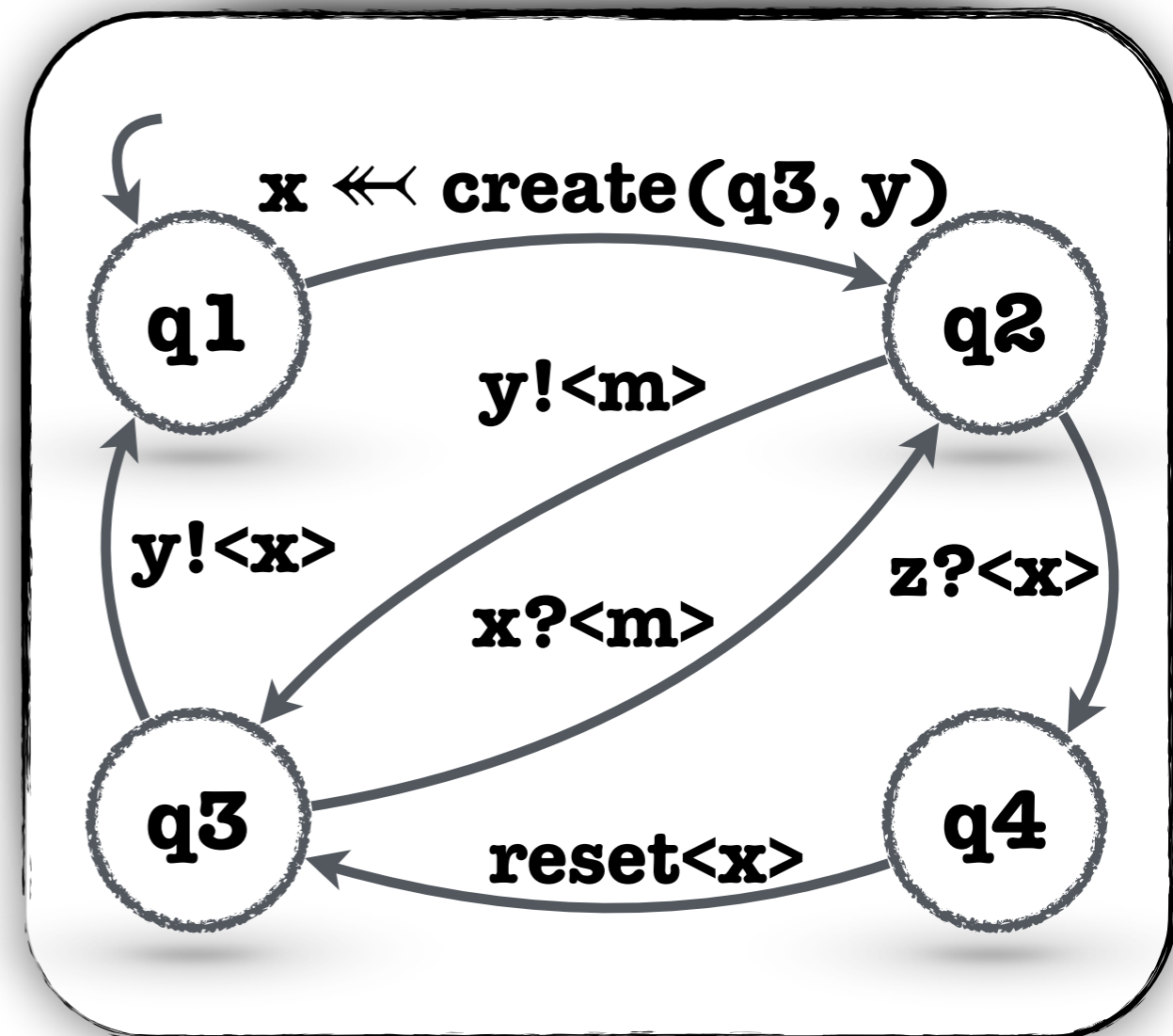
Verification of Dynamic Register Automata



Formal Model

Process Model

Finite State System



Dynamic Register Automata

Verification of Dynamic Register Automata



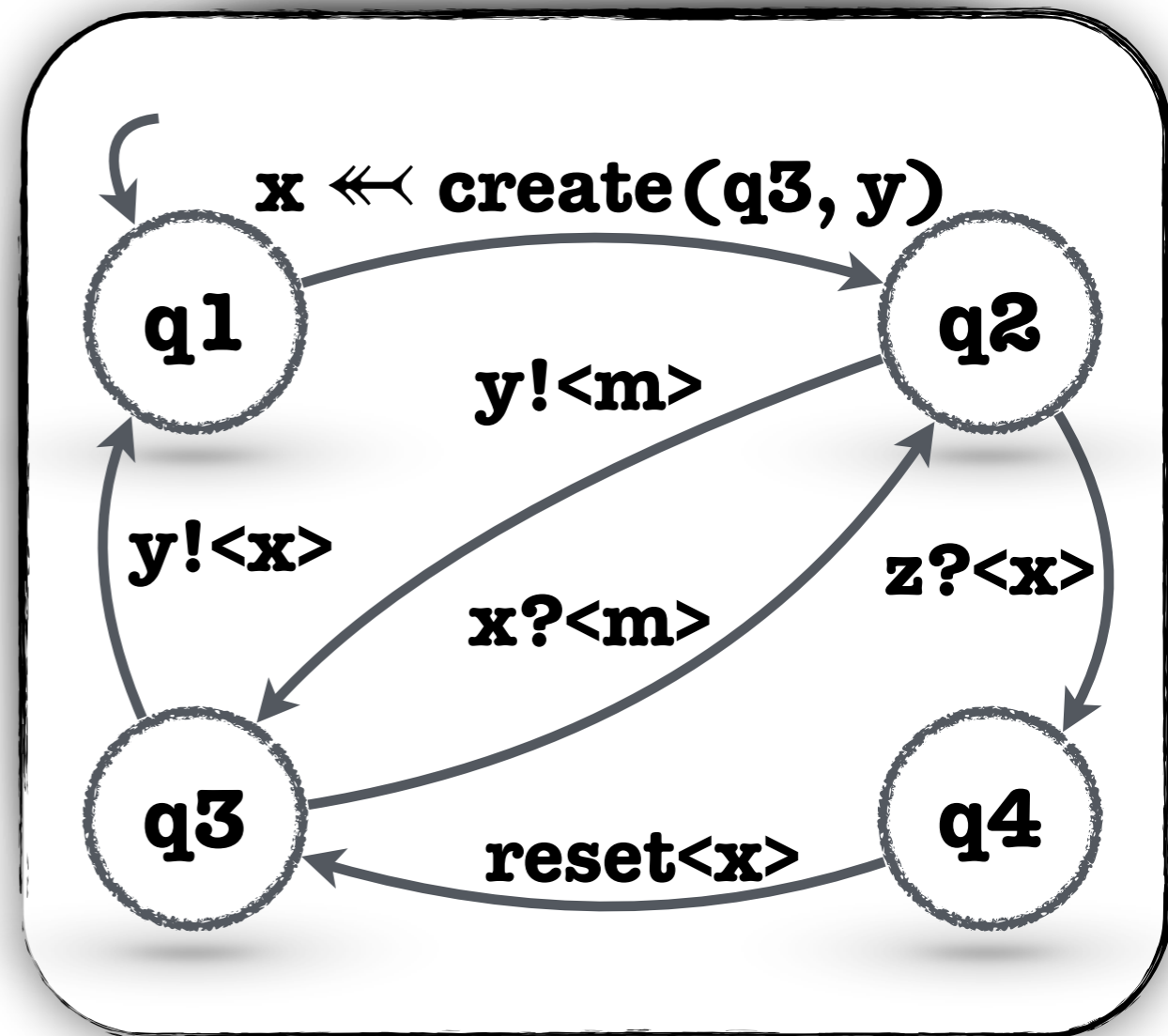
Formal Model

Configuration

Network of Processes

Process Model

Finite State System



Dynamic Register Automata

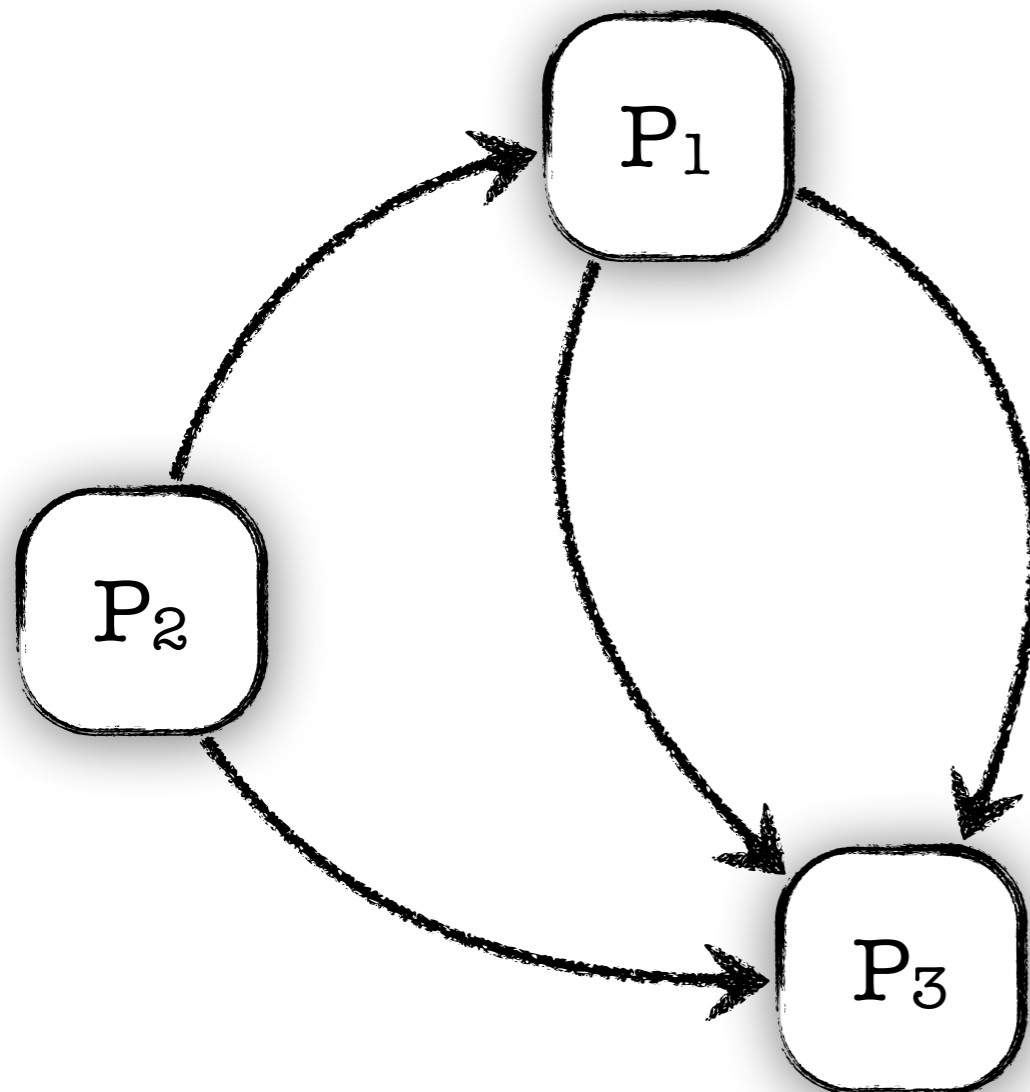


Verification of Dynamic Register Automata

Formal Model

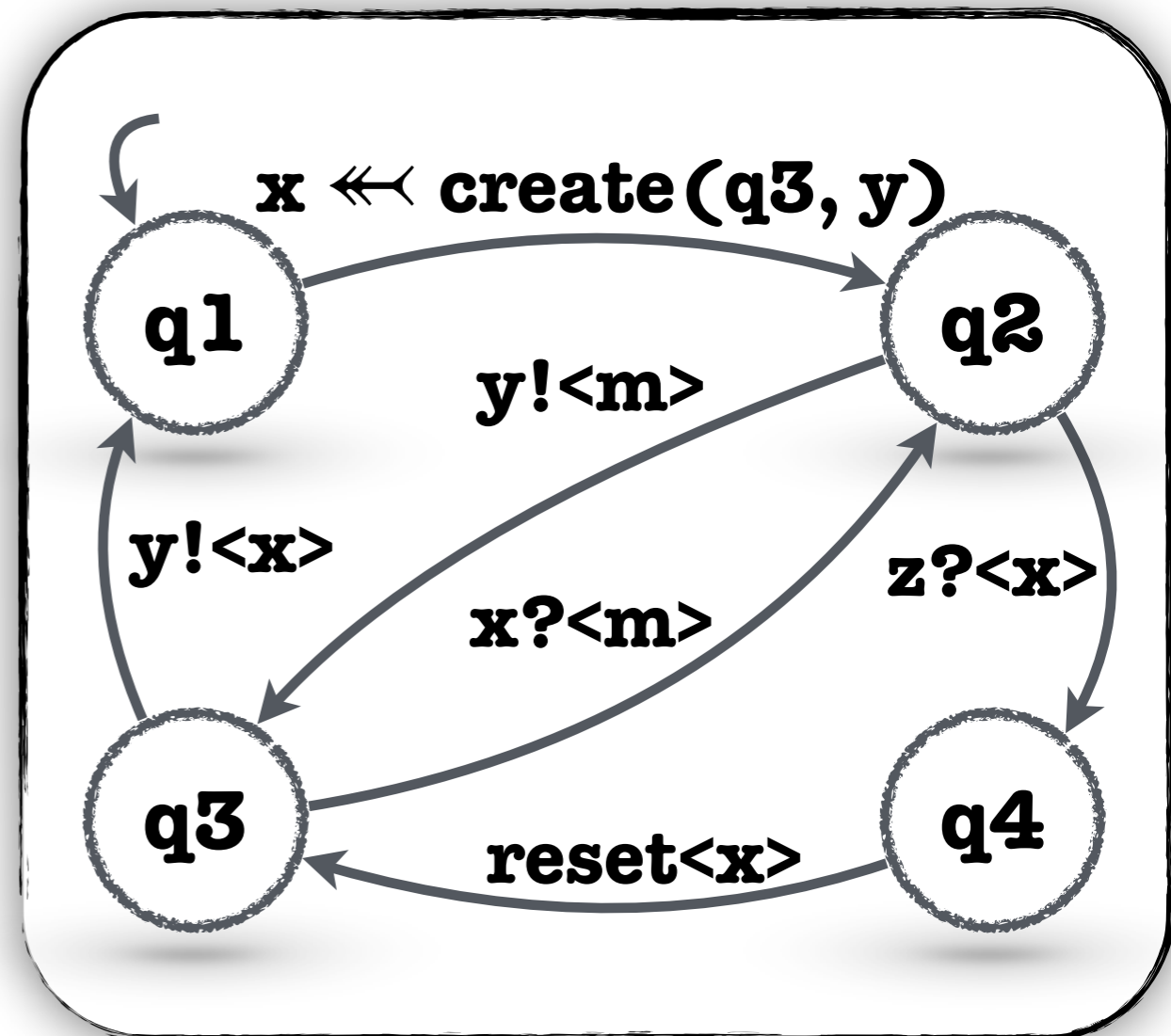
Configuration

Network of Processes

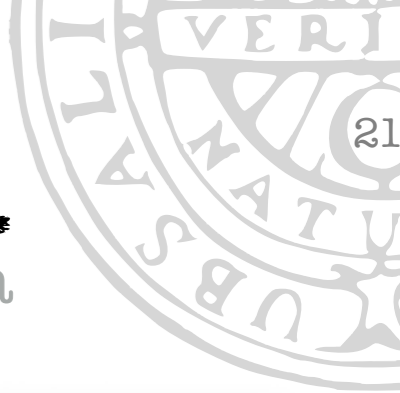


Process Model

Finite State System



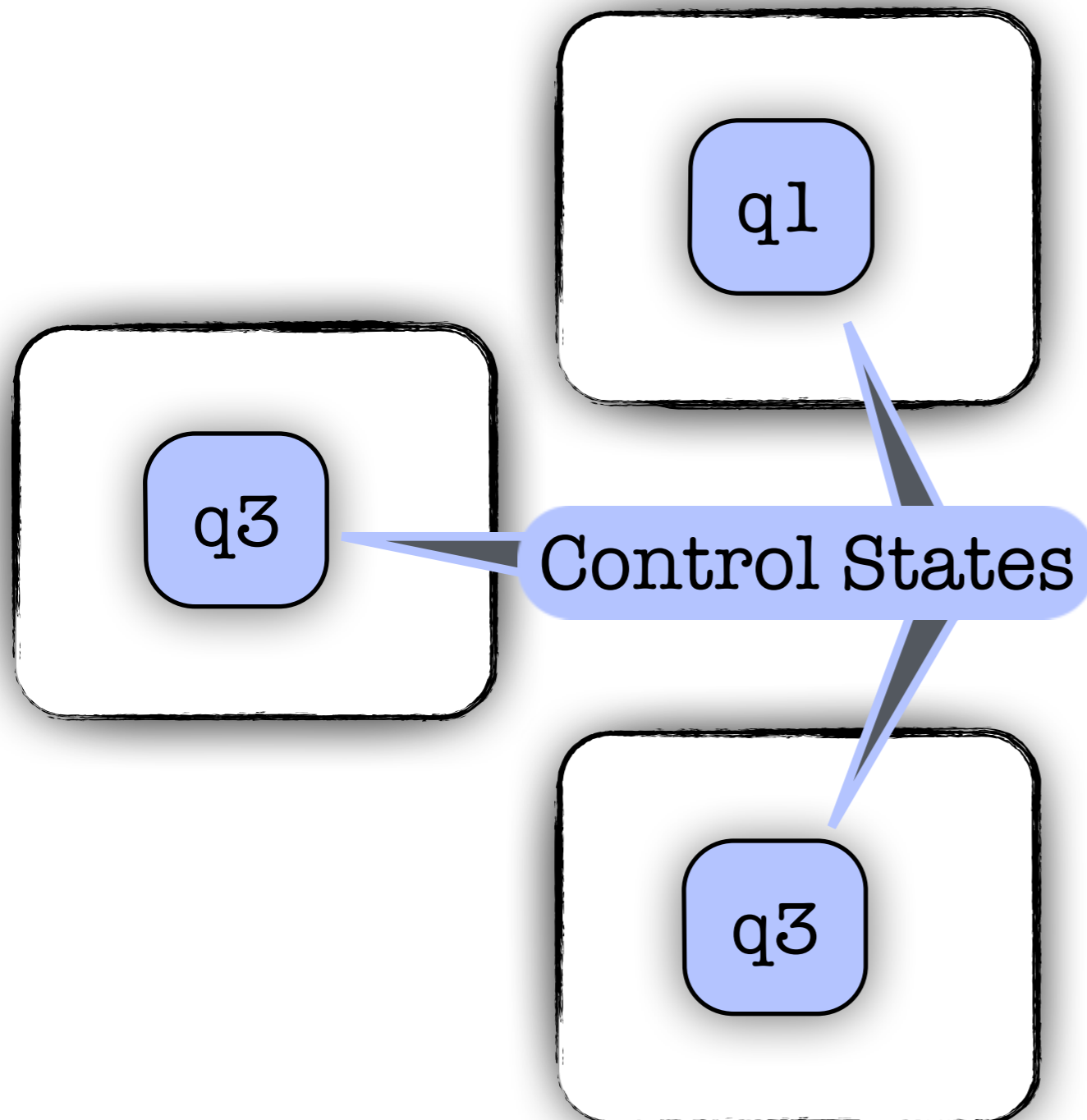
Dynamic Register Automata



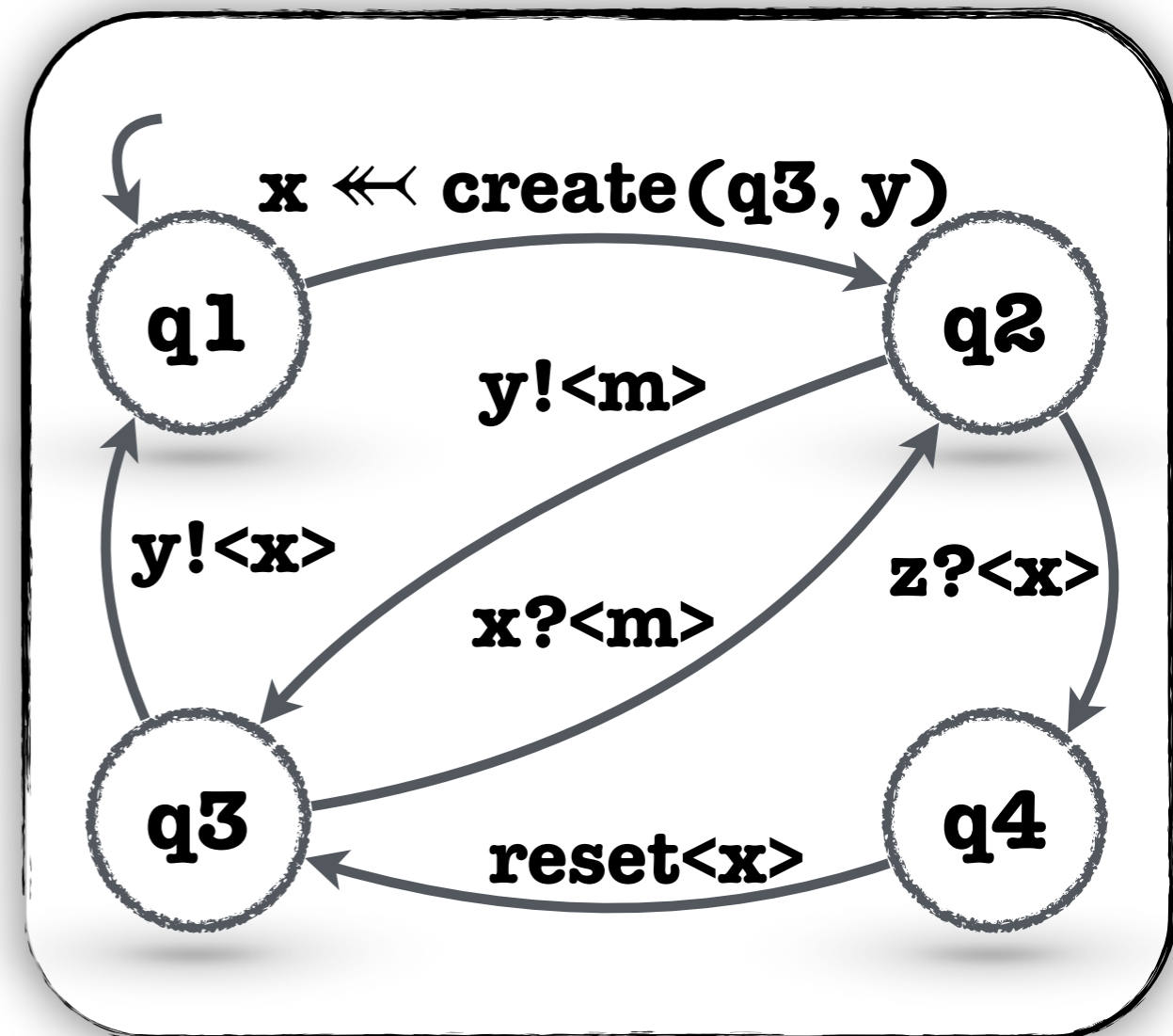
Verification of Dynamic Register Automata

Formal Model

Configuration



Process Model



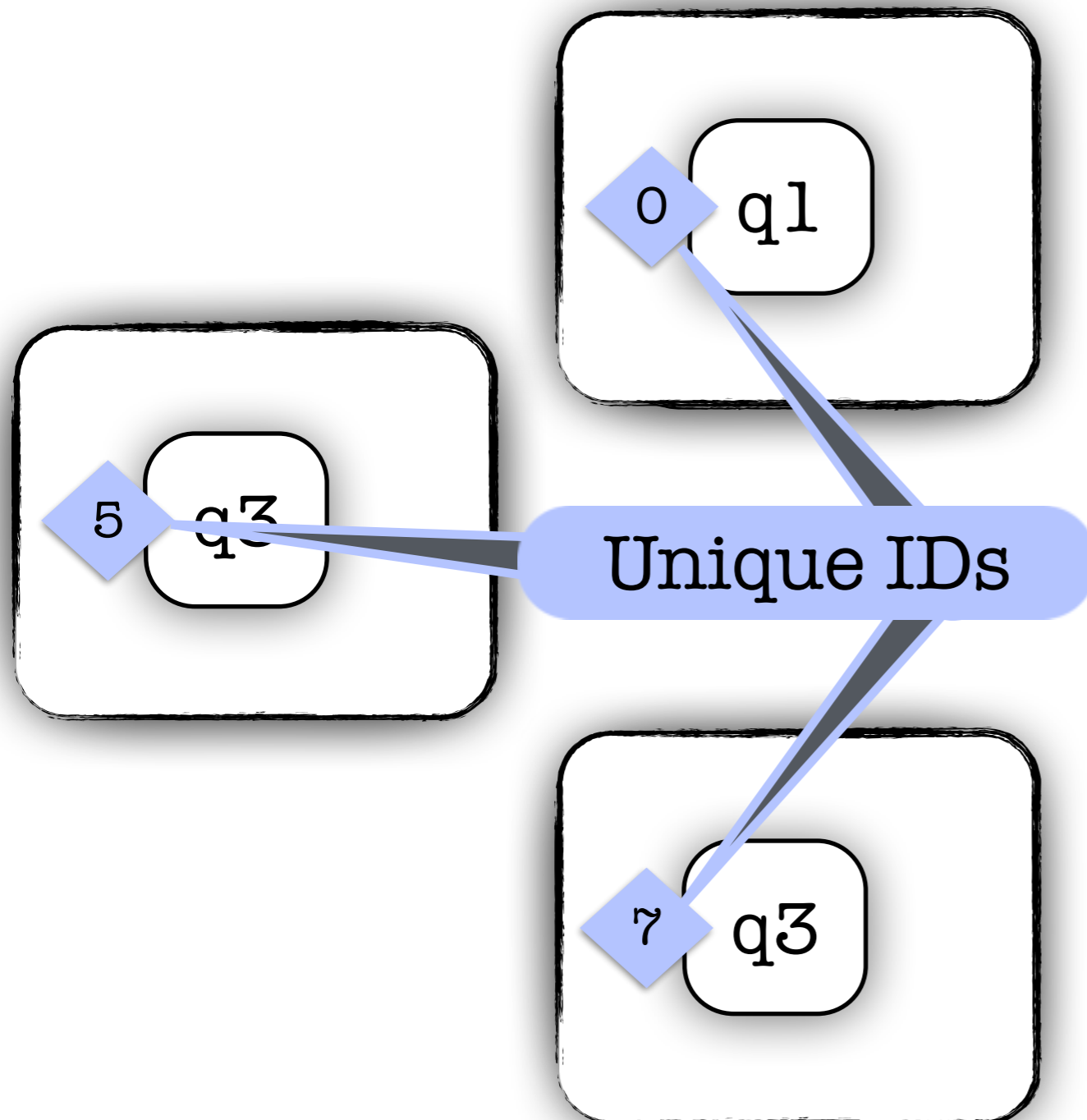
Dynamic Register Automata



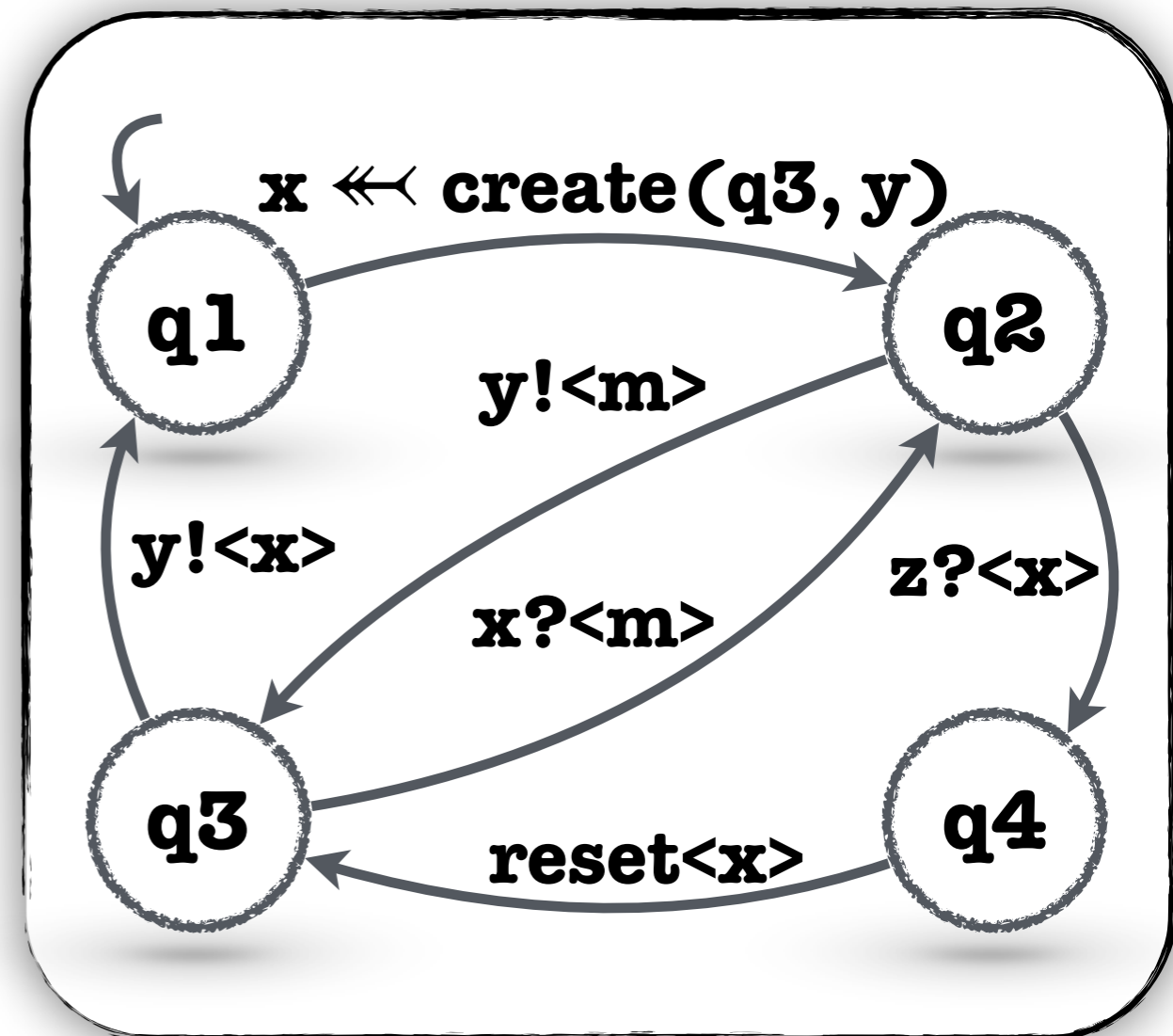
Verification of Dynamic Register Automata

Formal Model

Configuration



Process Model



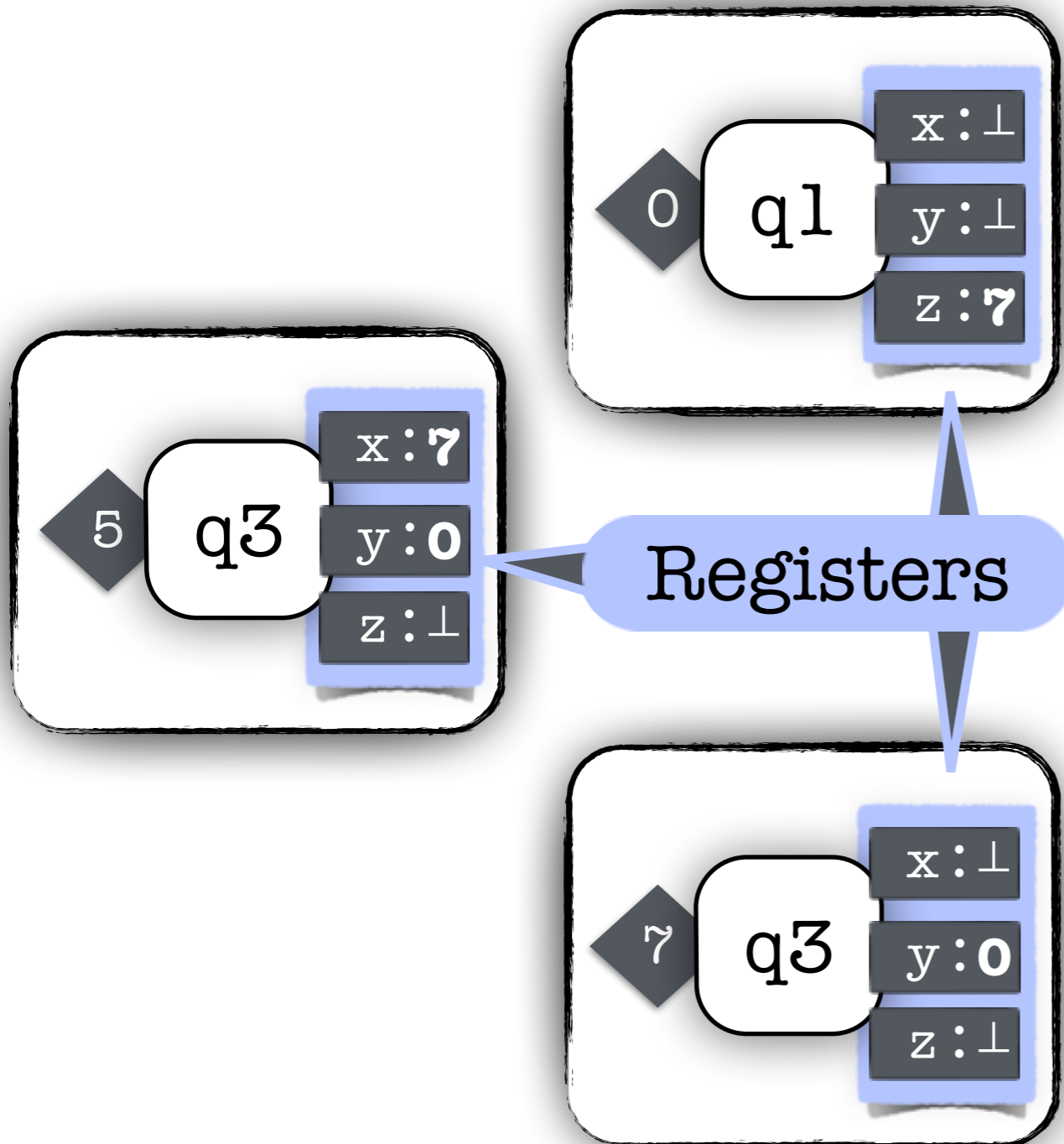
Dynamic Register Automata



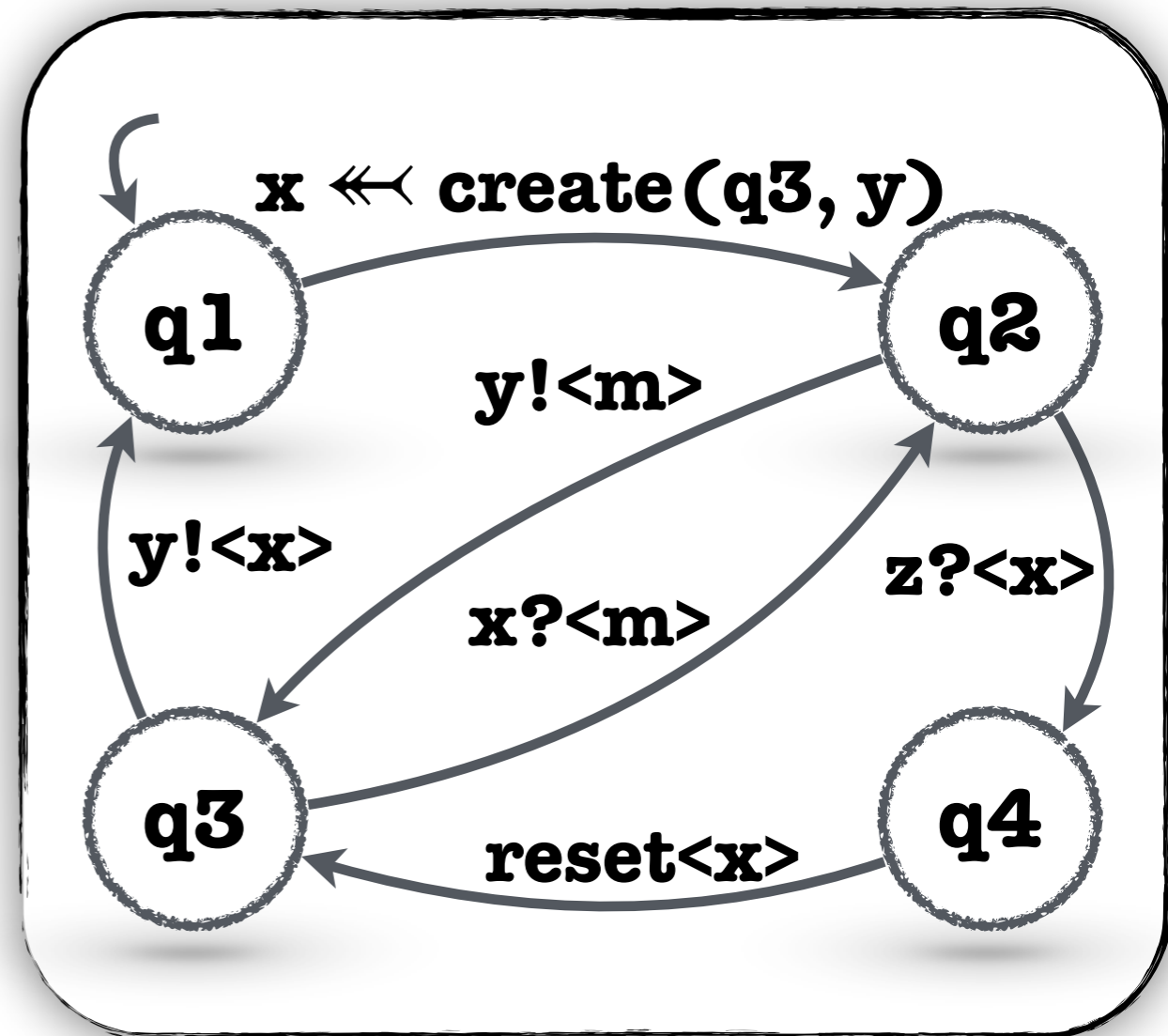
Verification of Dynamic Register Automata

Formal Model

Configuration



Process Model



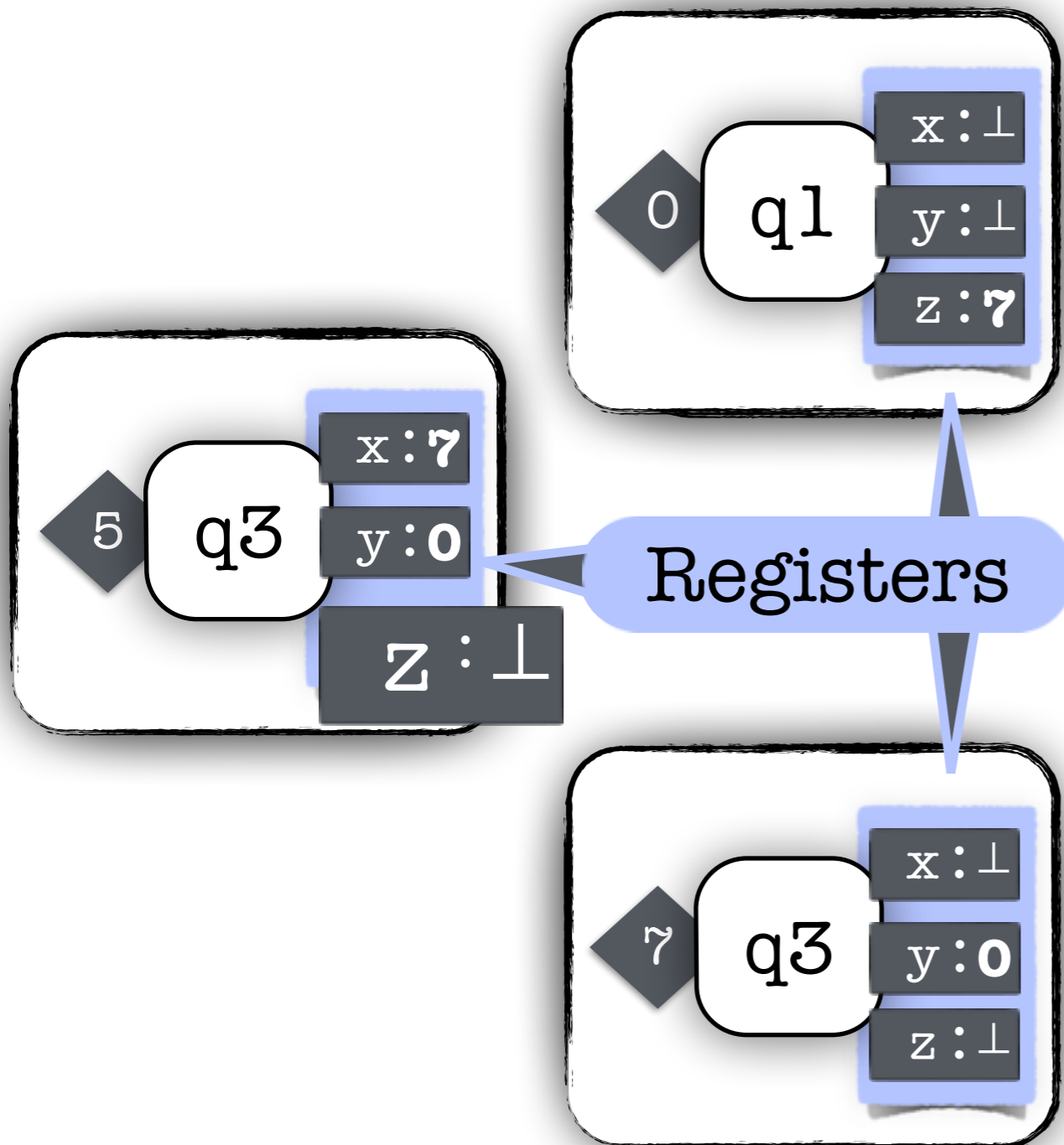
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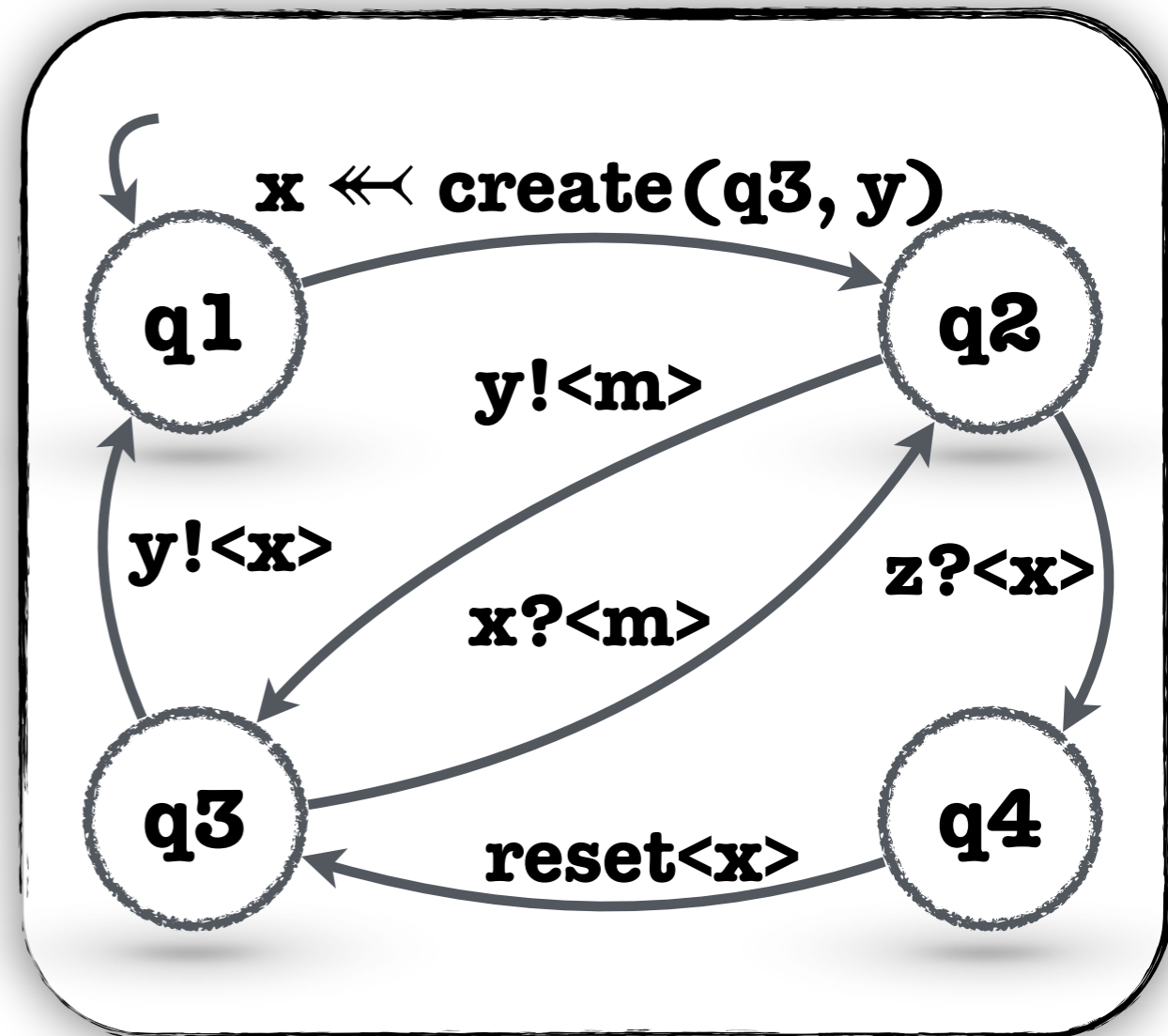
Verification of Dynamic Register Automata

Formal Model

Configuration



Process Model



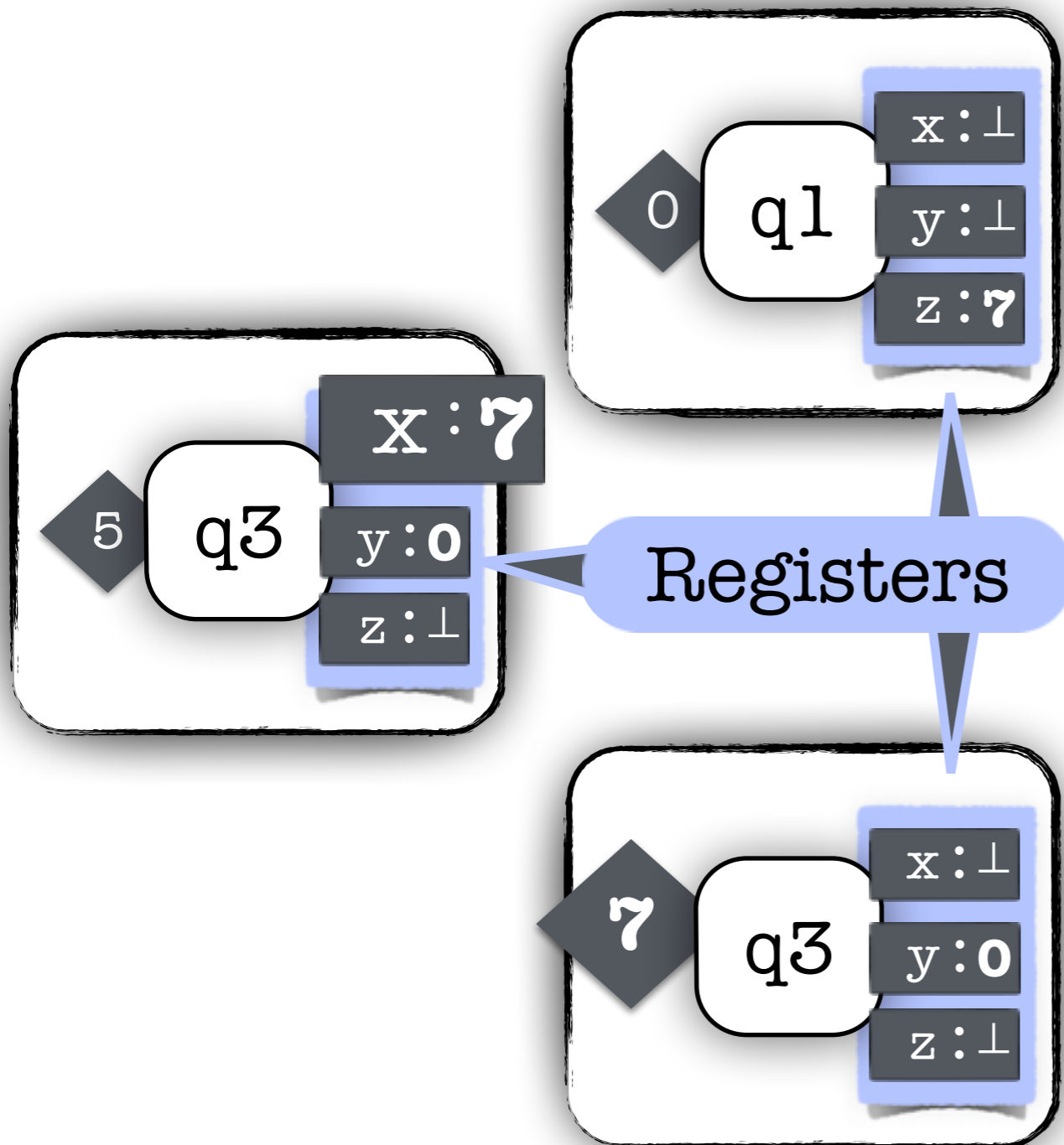
Dynamic Register Automata



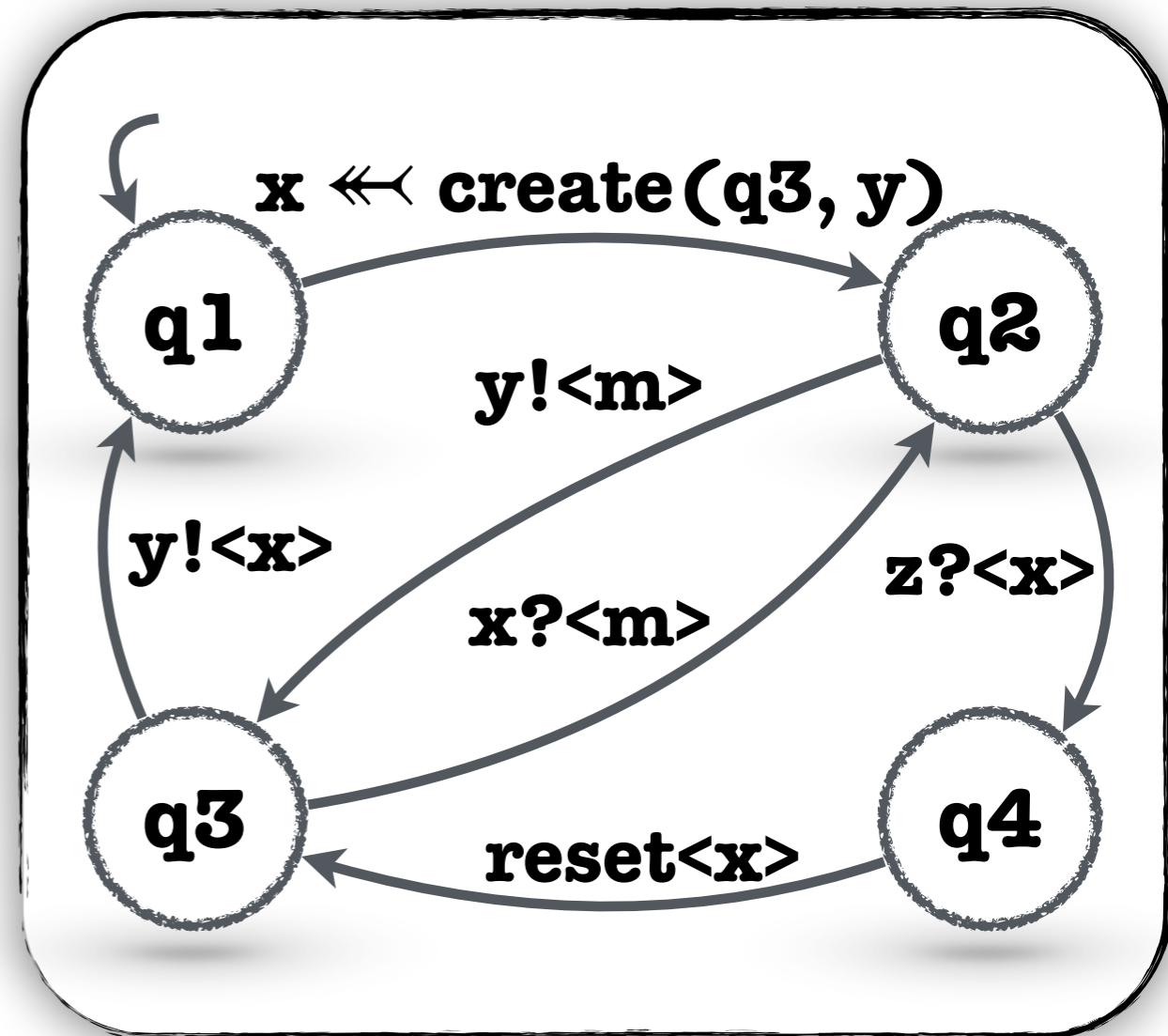
Formal Model

Verification of Dynamic Register Automata

Configuration



Process Model



Dynamic Register Automata

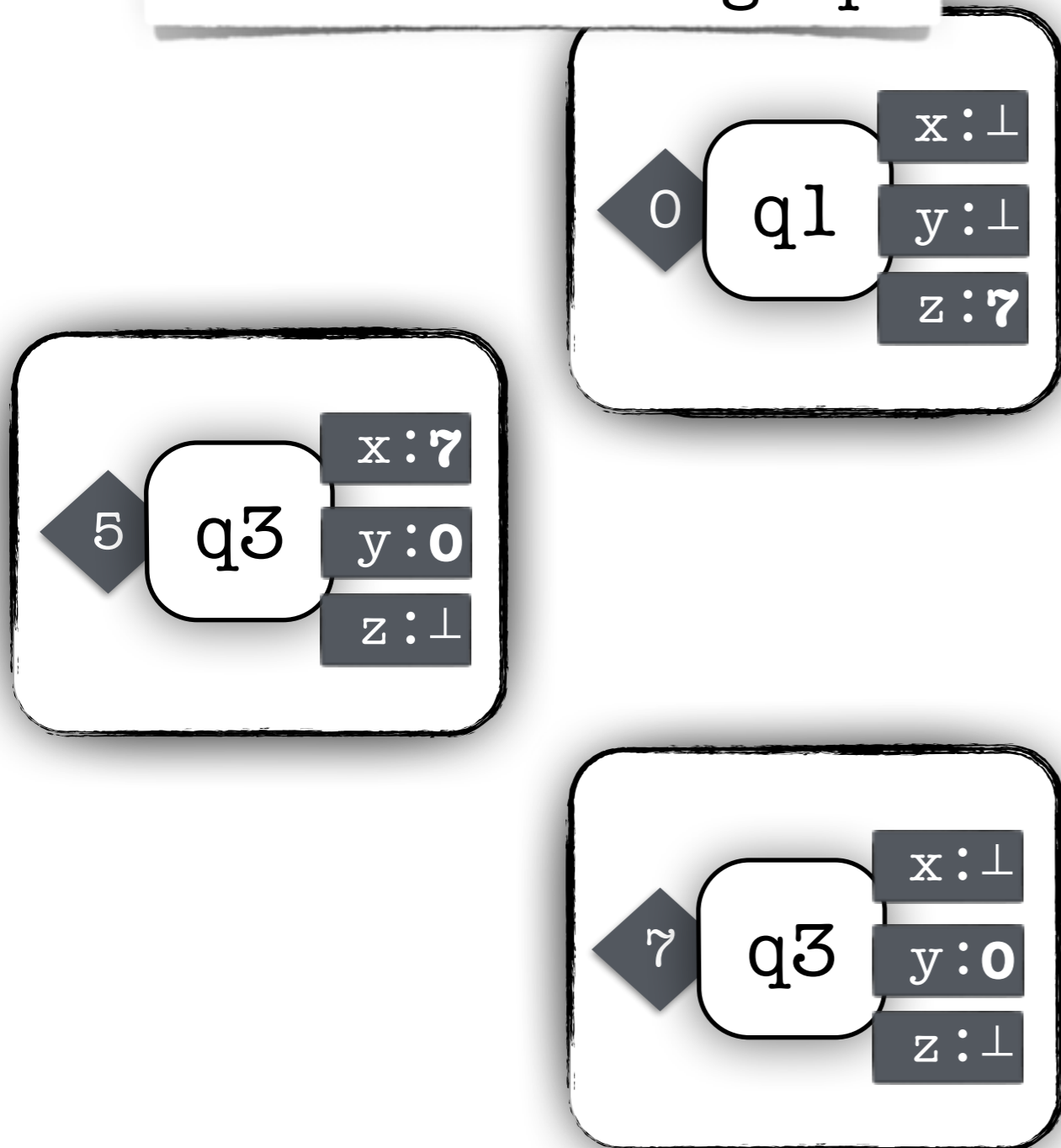


Formal Model

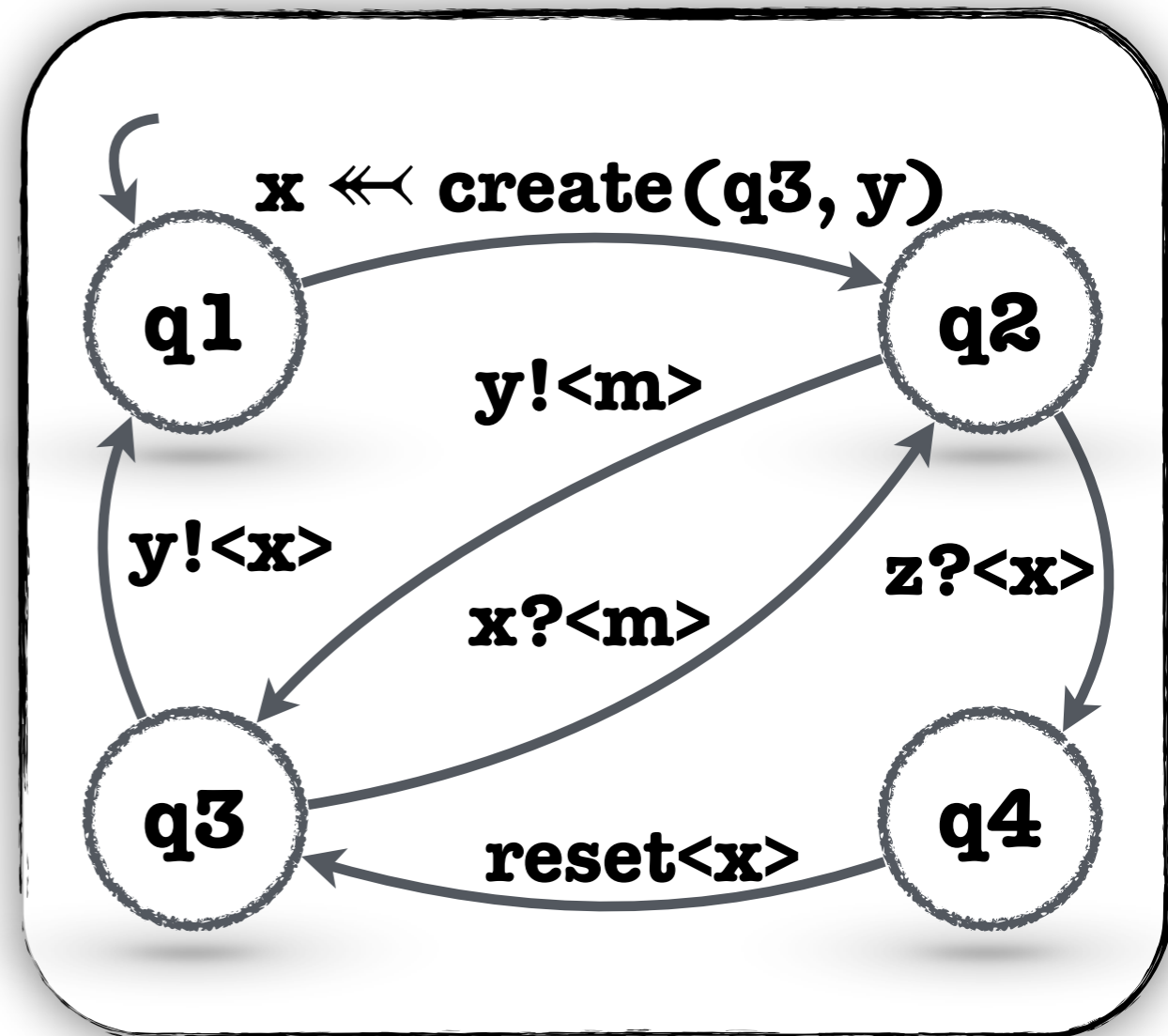
Verification of Dynamic Register Automata

Configuration

Communication graph



Process Model



Dynamic Register Automata

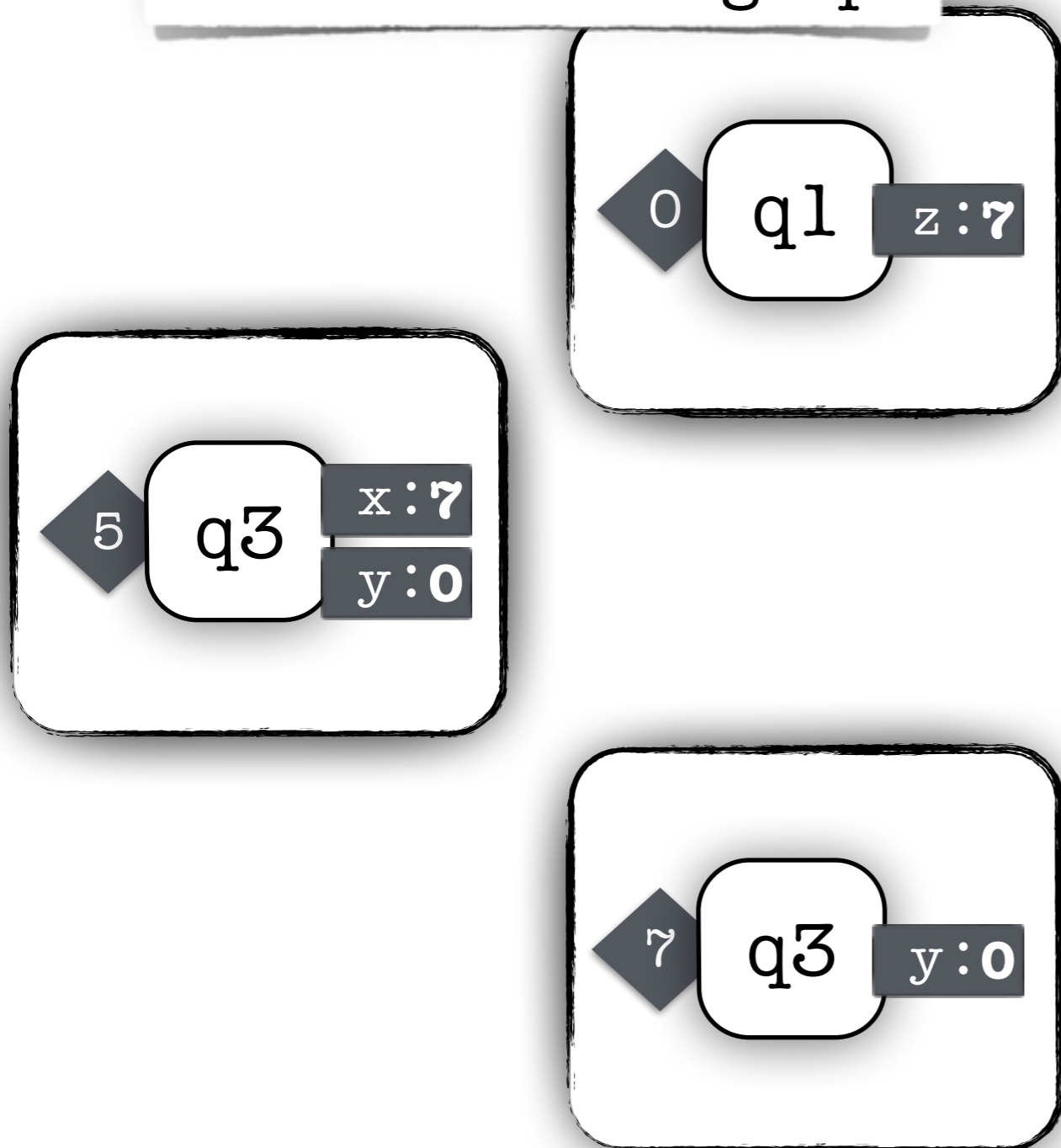


Formal Model

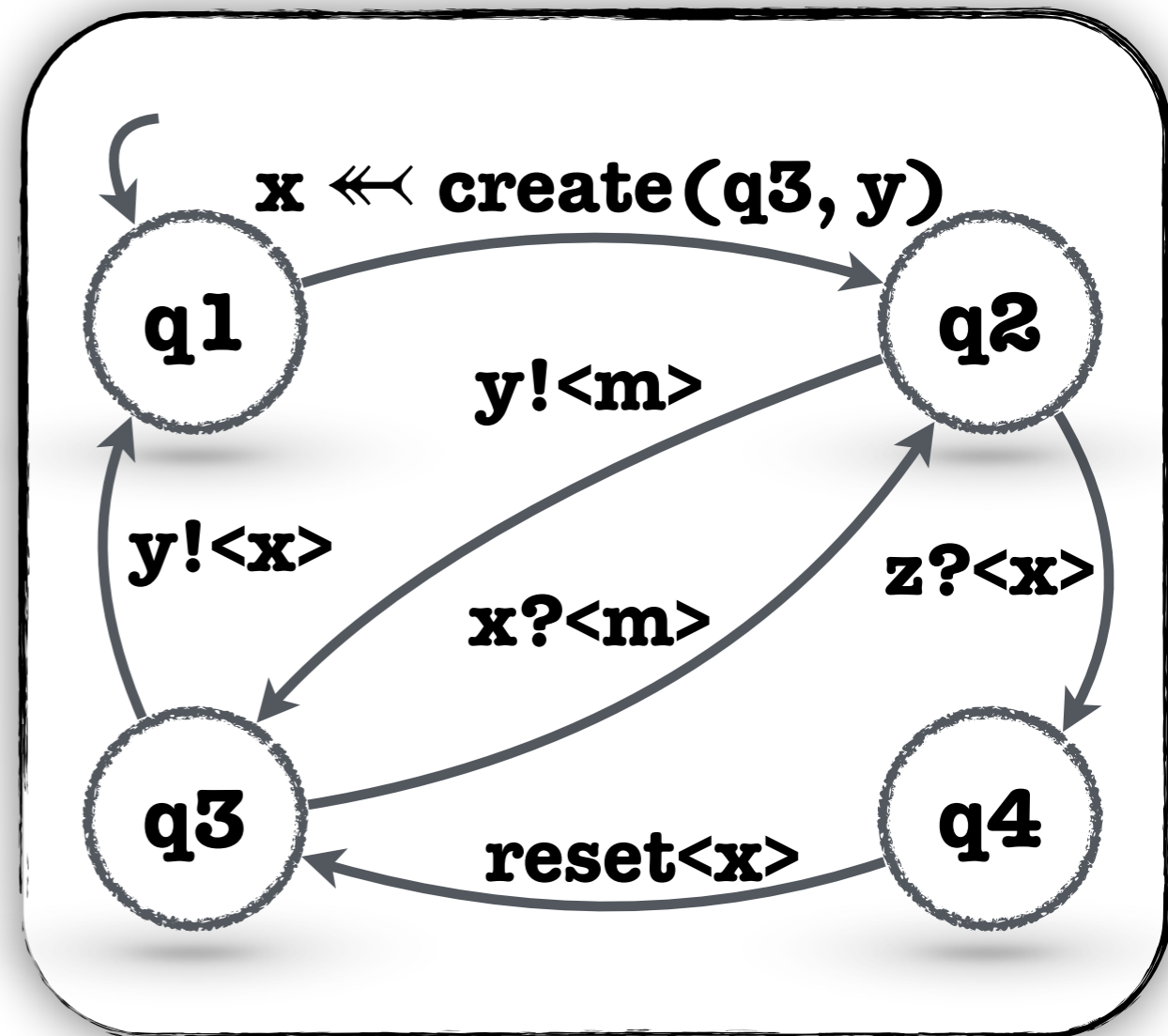
Verification of Dynamic Register Automata

Configuration

Communication graph



Process Model



Dynamic Register Automata

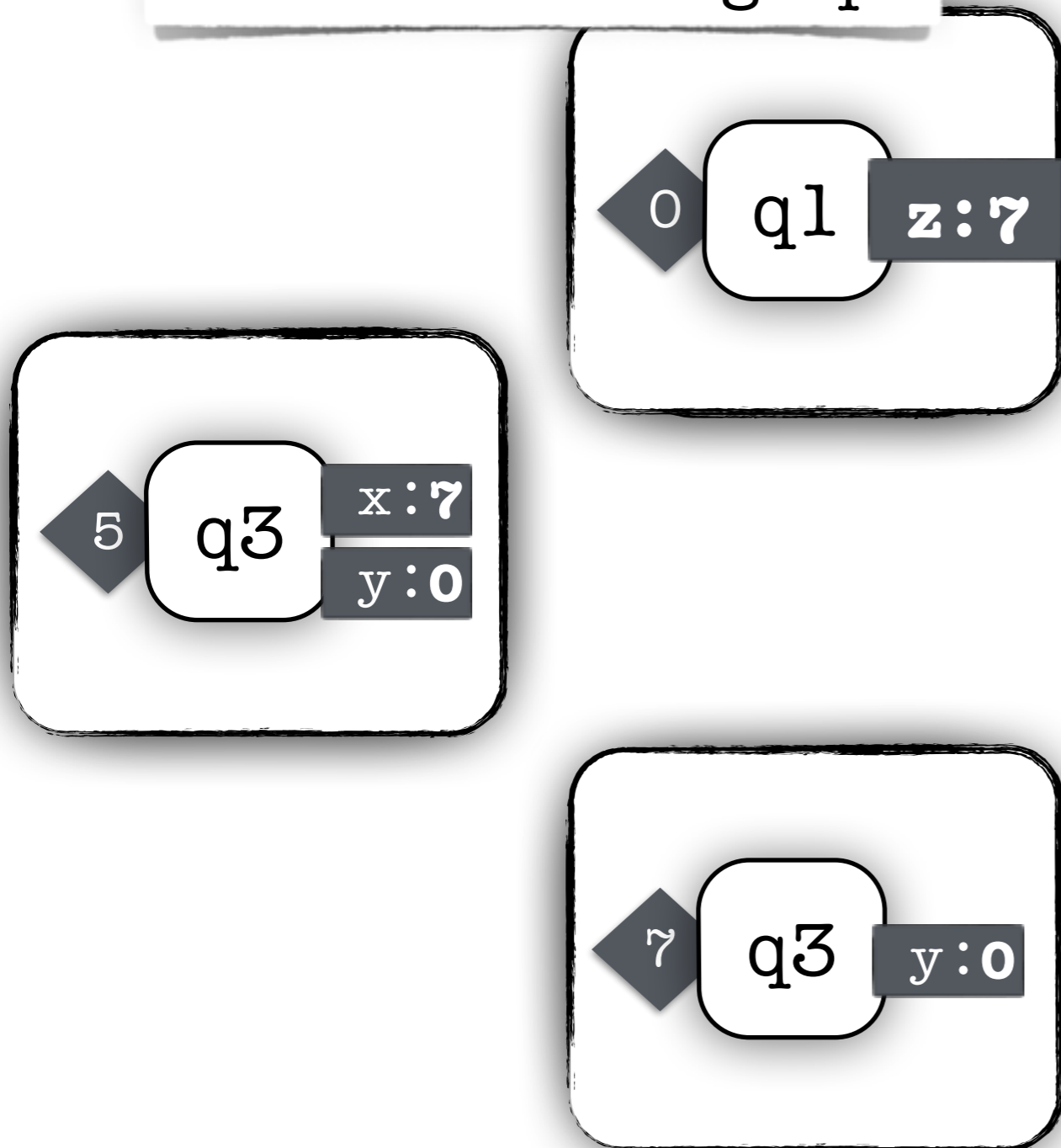


Verification of Dynamic Register Automata

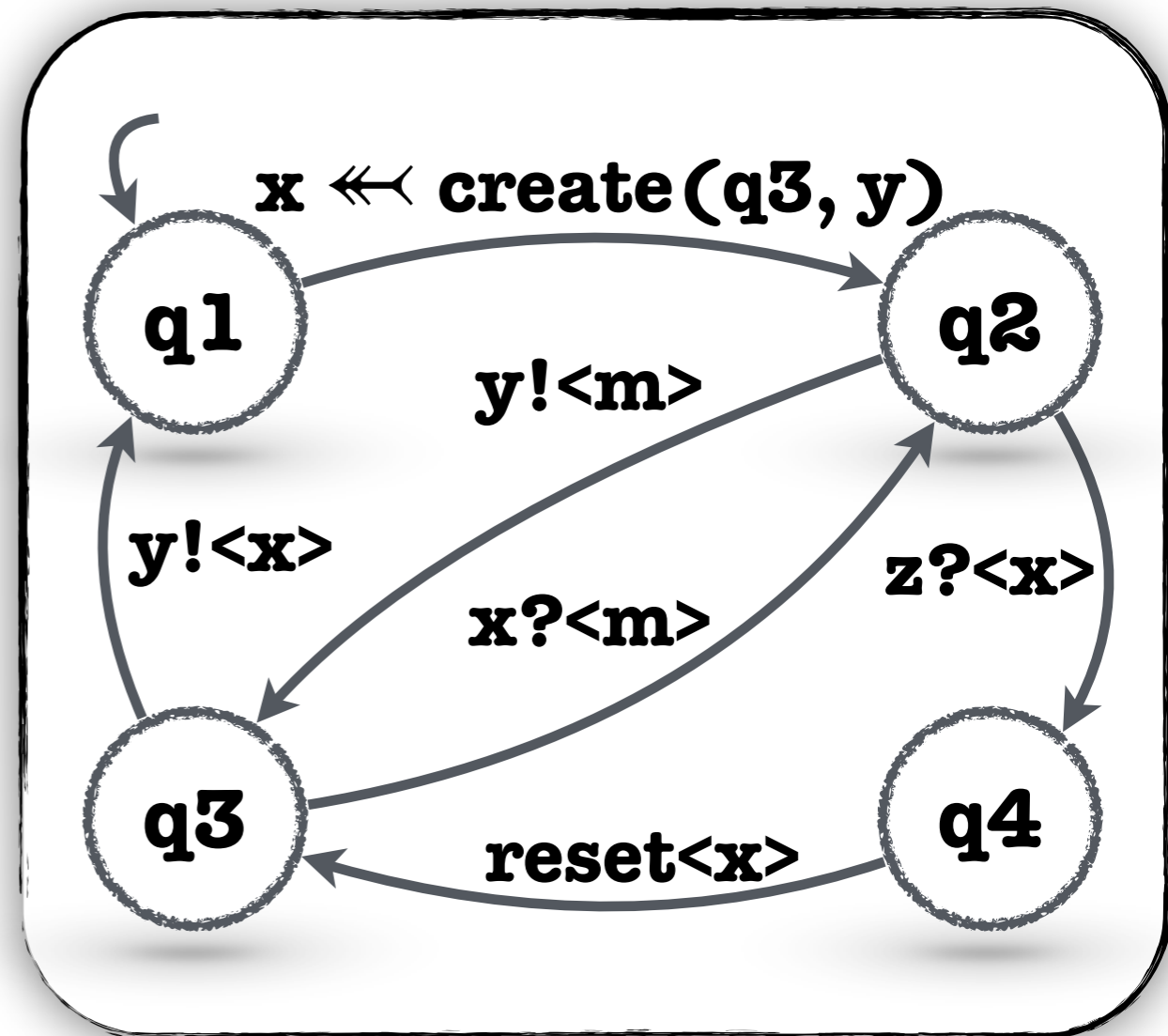
Formal Model

Configuration

Communication graph



Process Model



Dynamic Register Automata

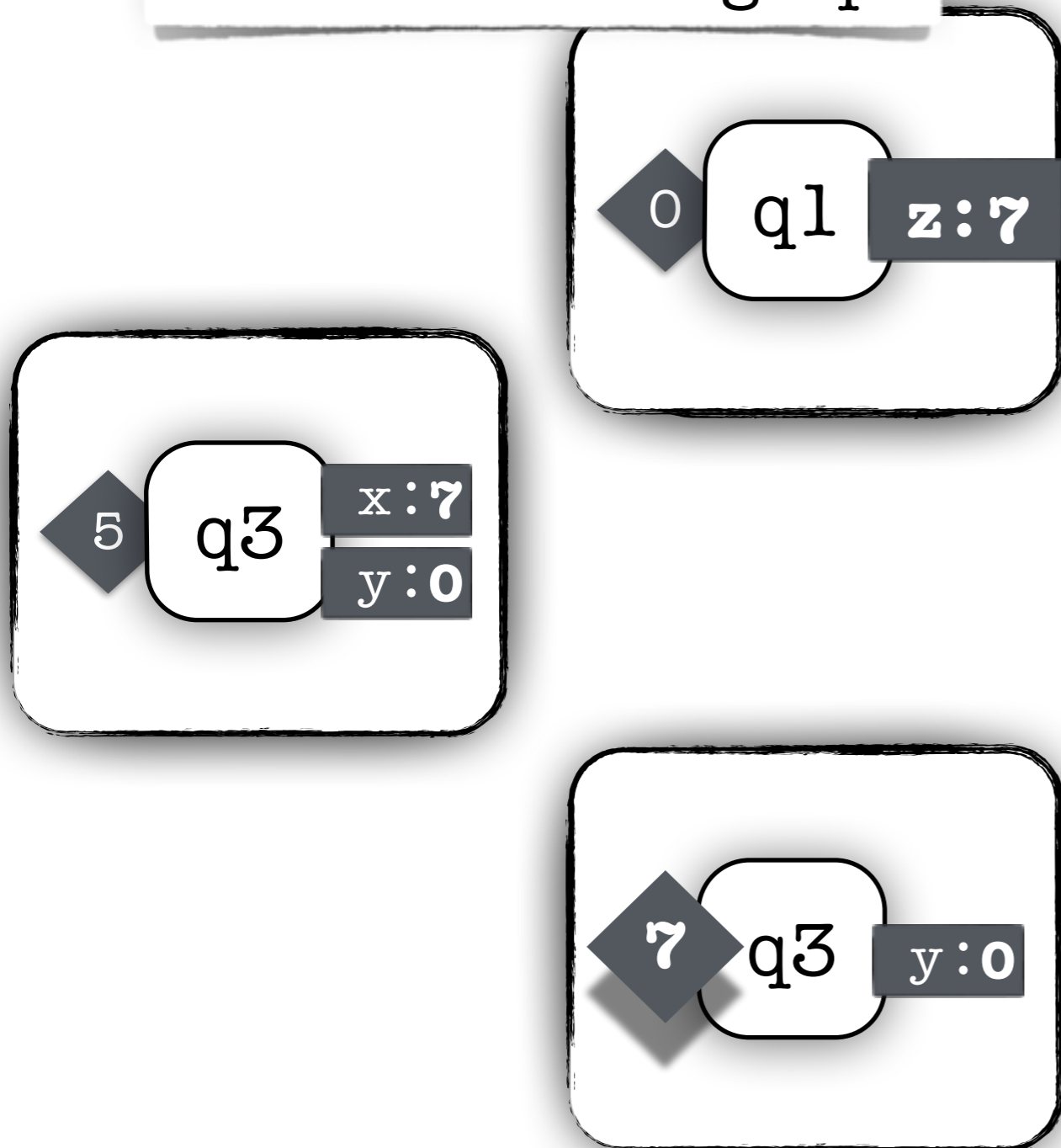


Verification of Dynamic Register Automata

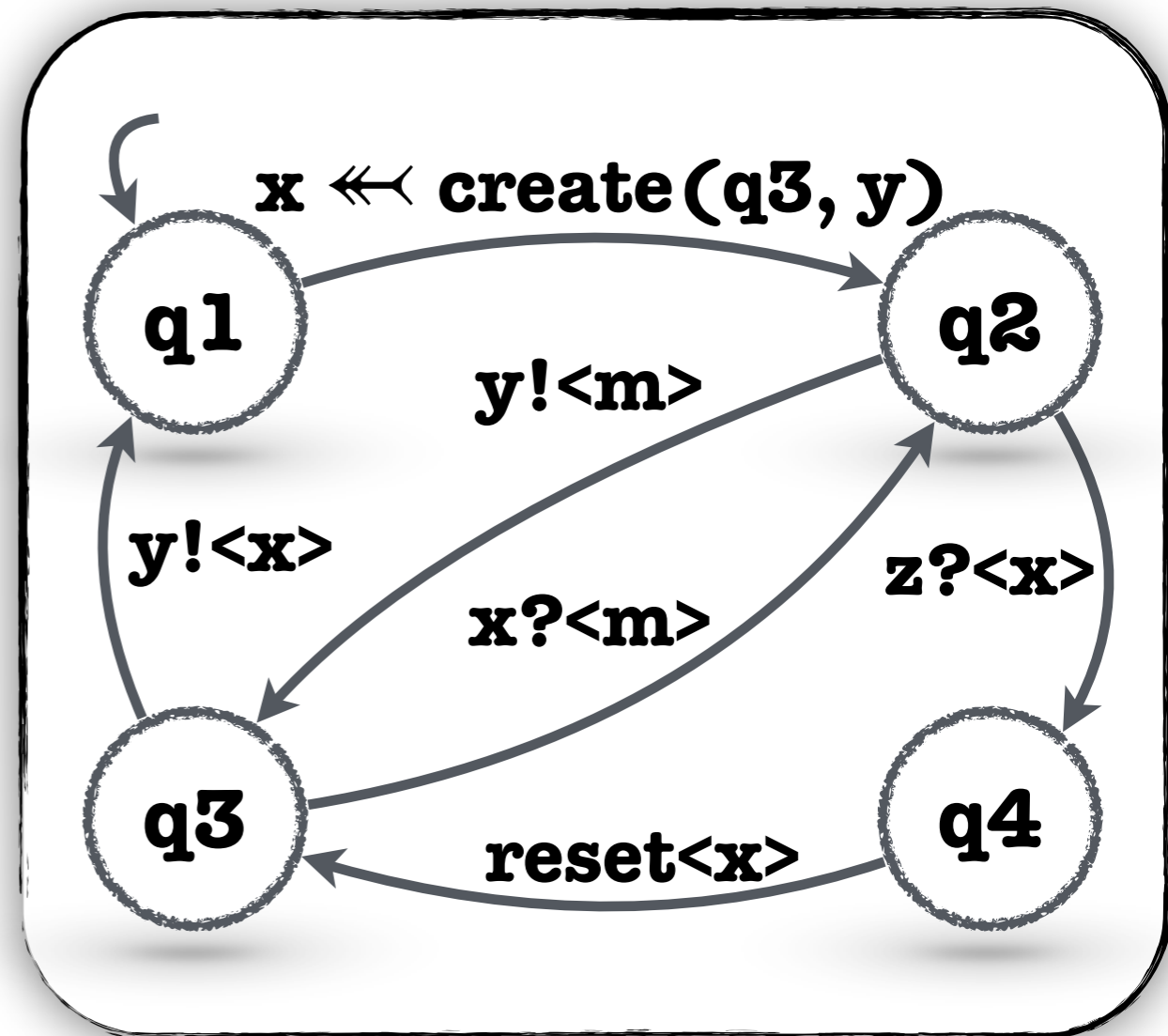
Formal Model

Configuration

Communication graph



Process Model



Dynamic Register Automata

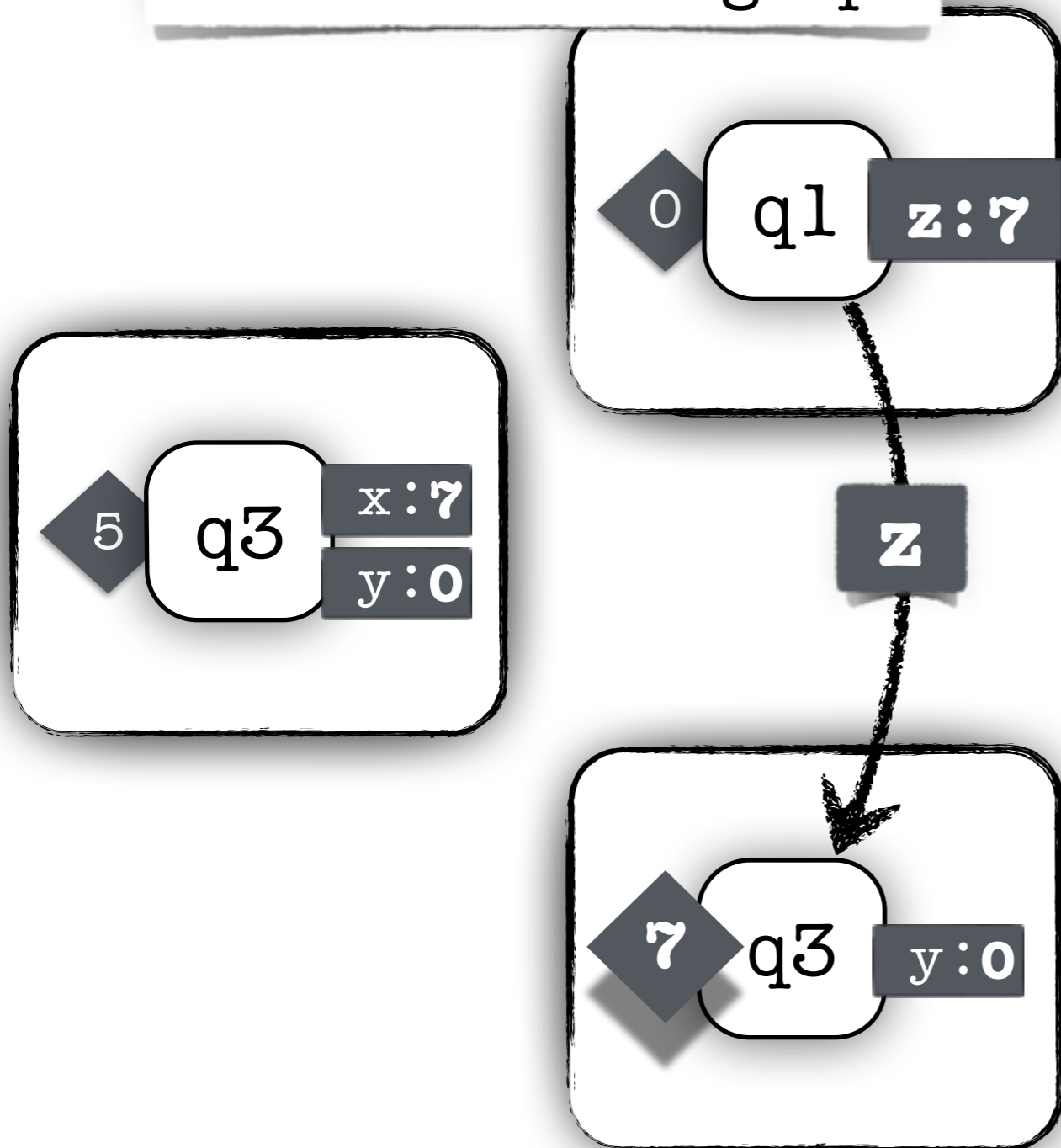


Formal Model

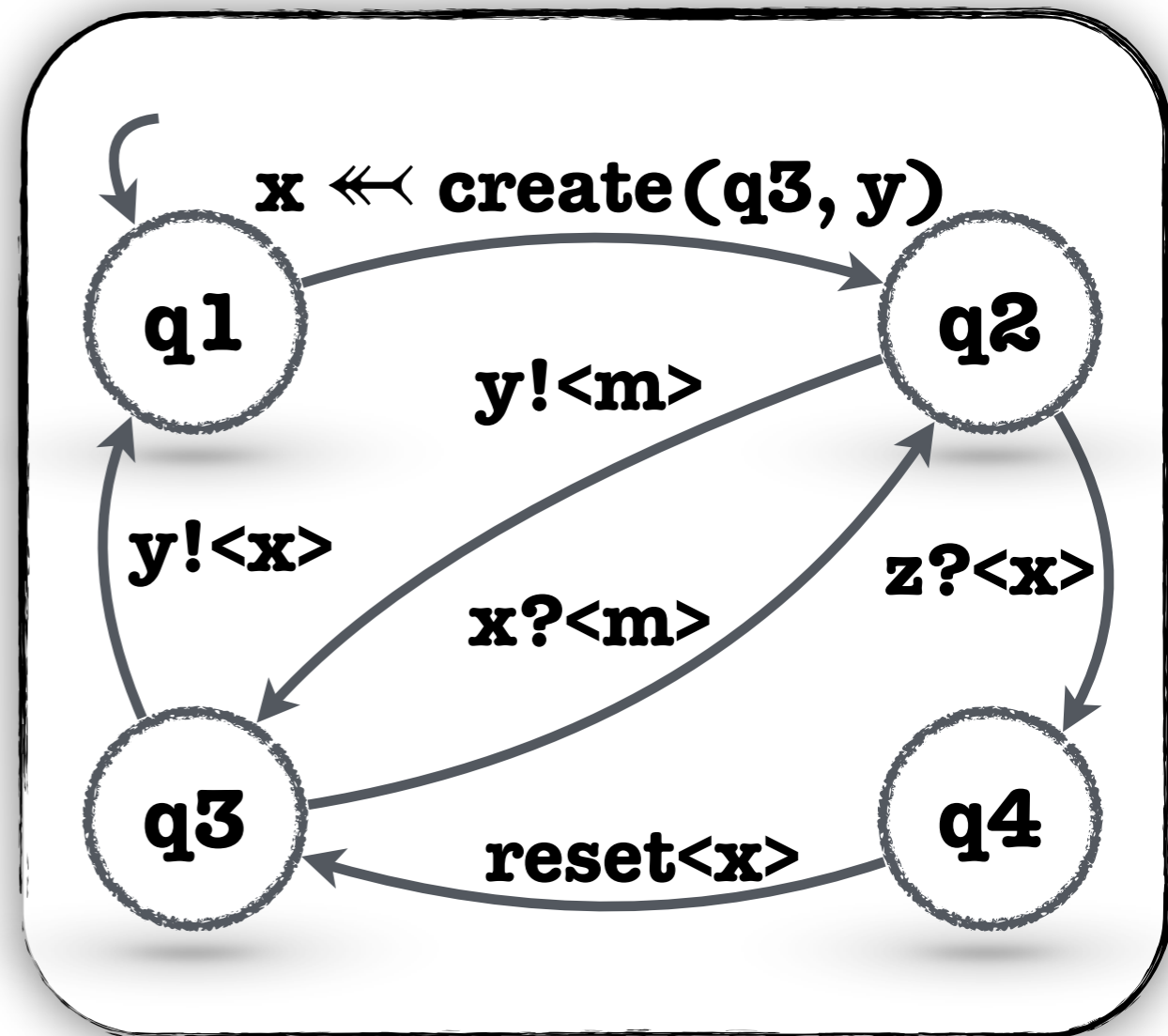
Verification of Dynamic Register Automata

Configuration

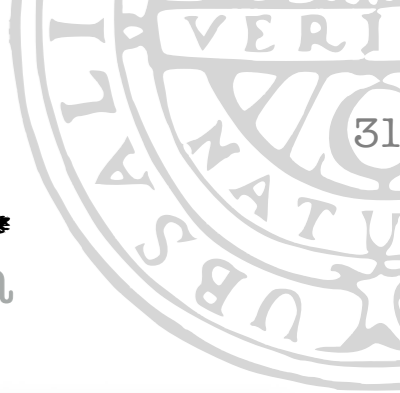
Communication graph



Process Model



Dynamic Register Automata

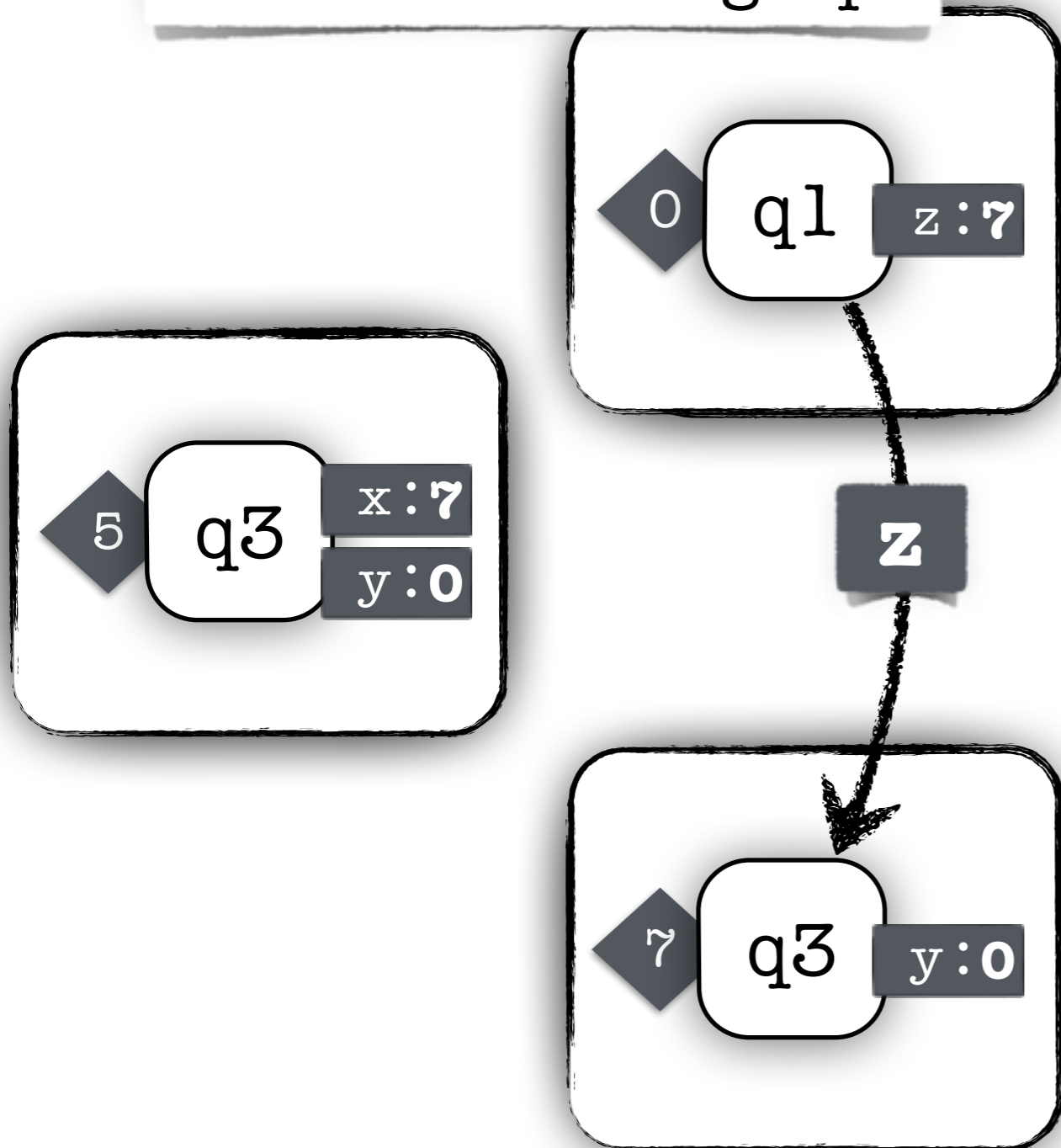


Verification of Dynamic Register Automata

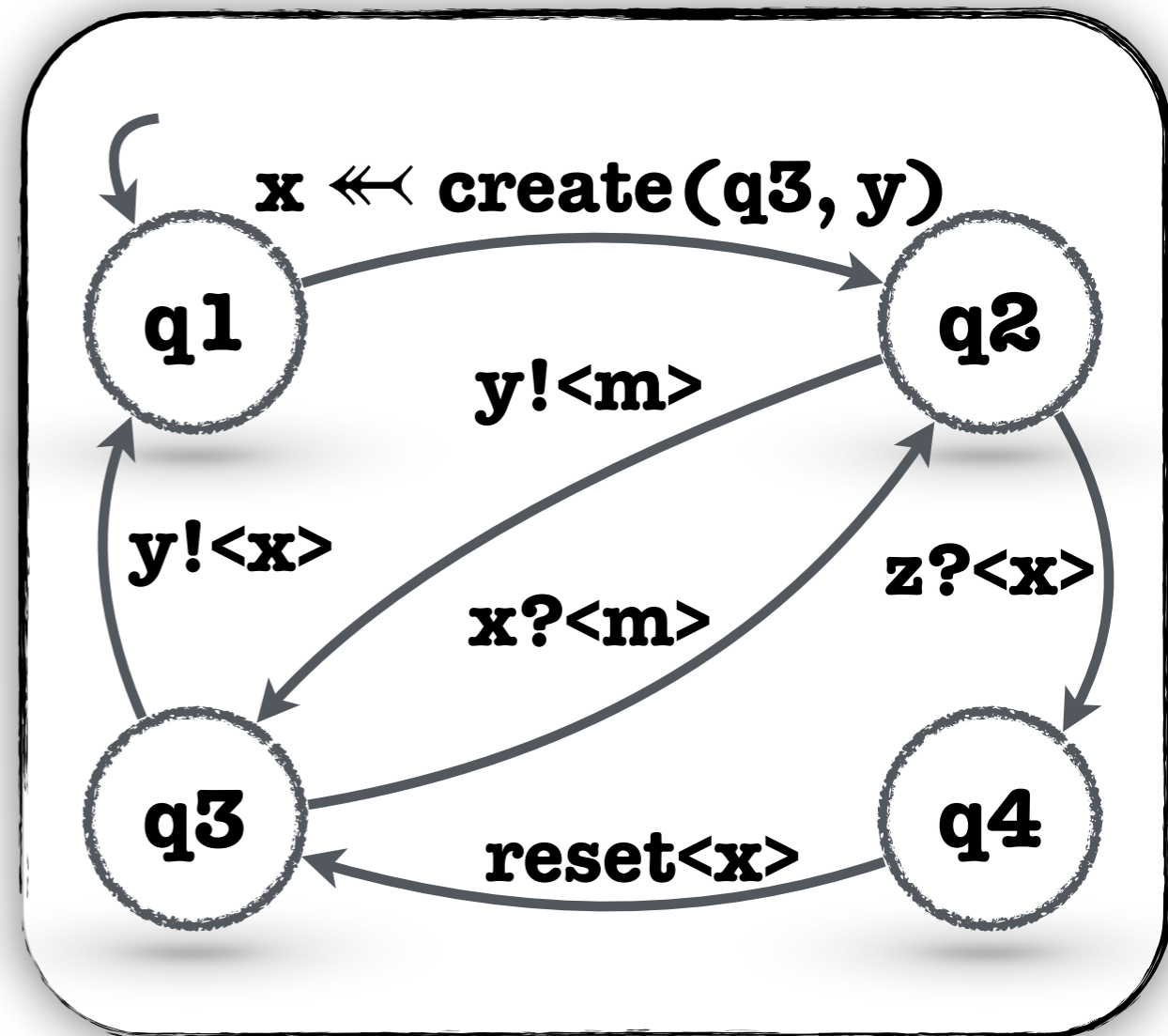
Formal Model

Configuration

Communication graph



Process Model



Dynamic Register Automata

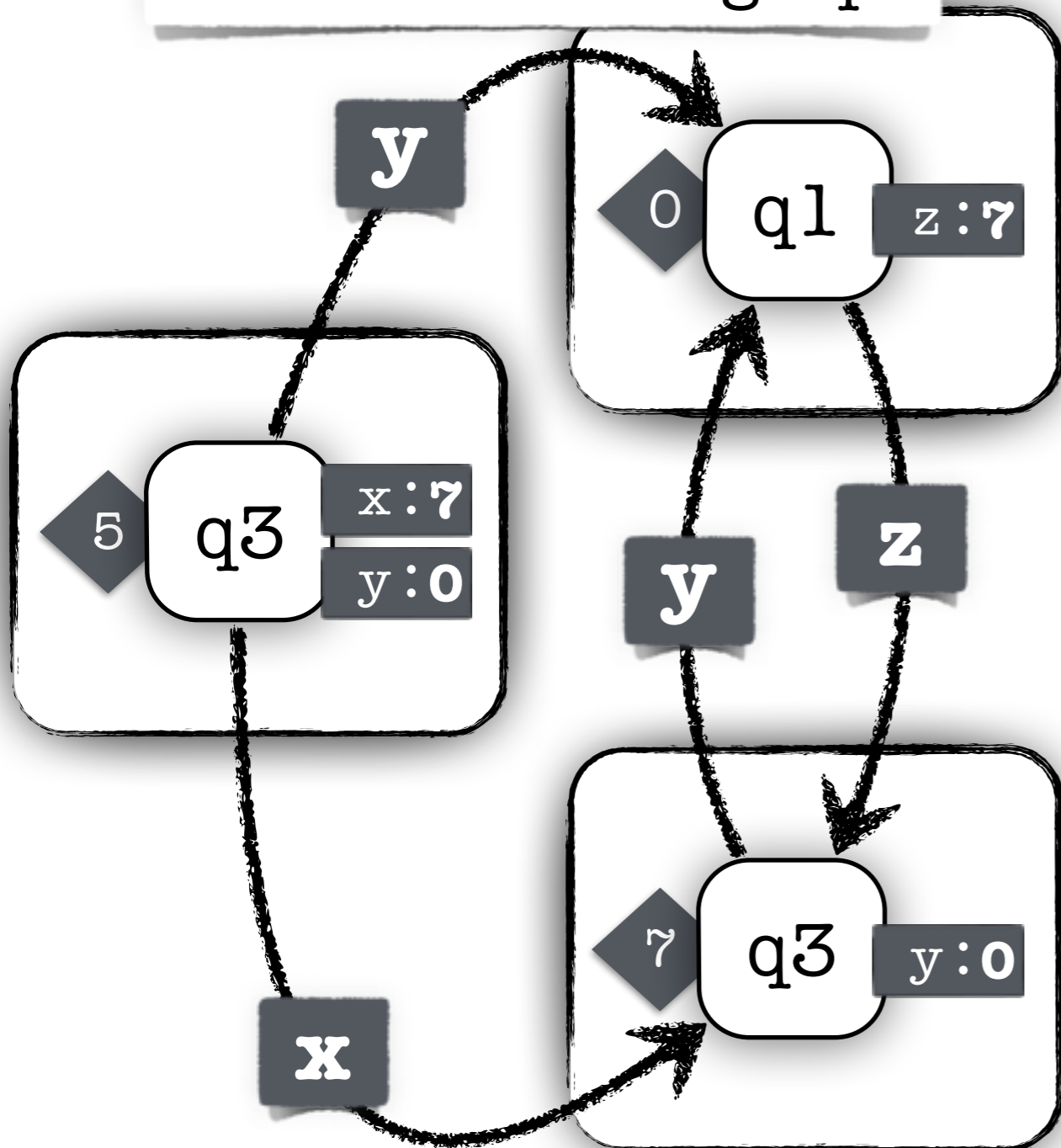


Formal Model

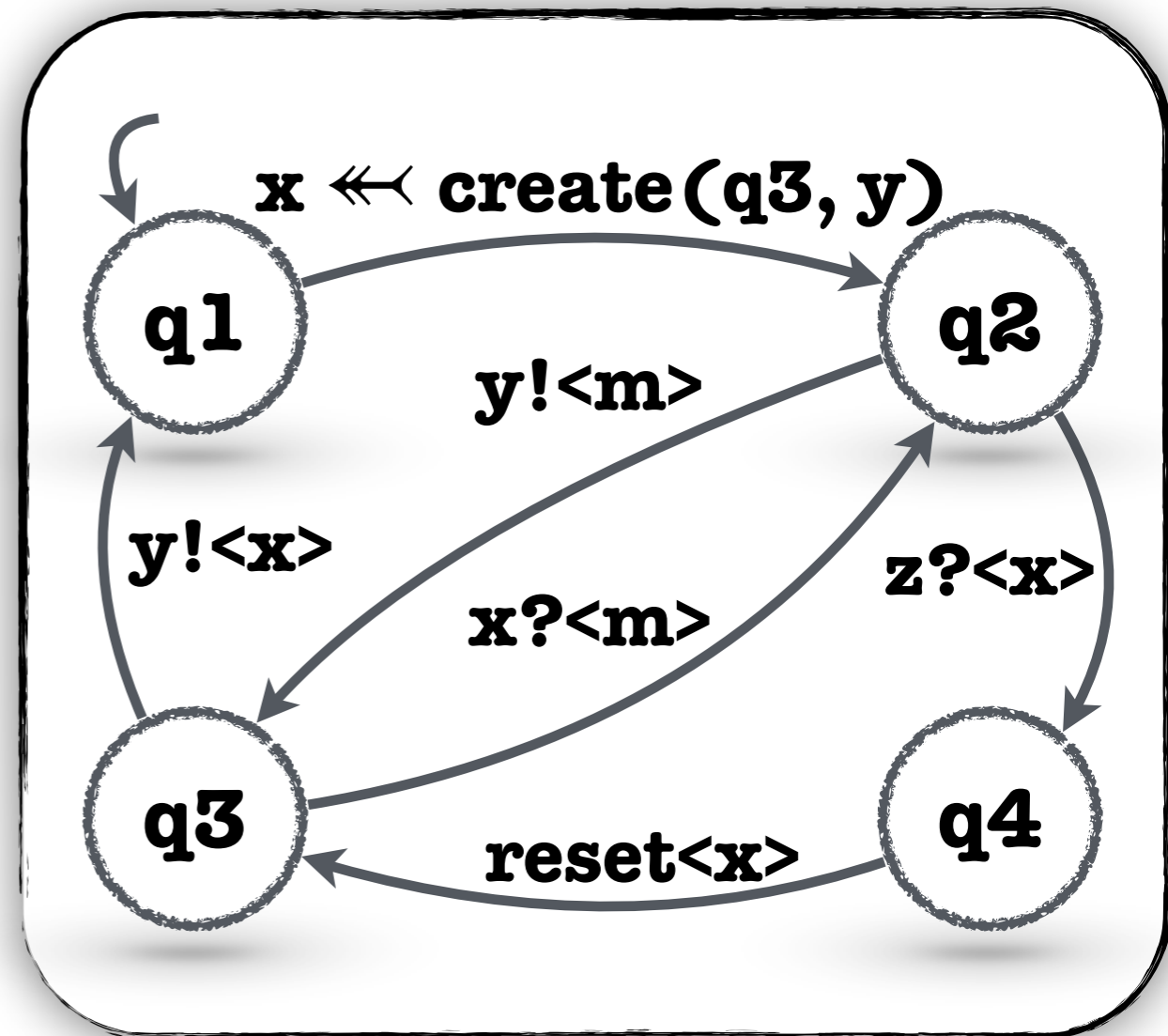
Verification of Dynamic Register Automata

Configuration

Communication graph



Process Model



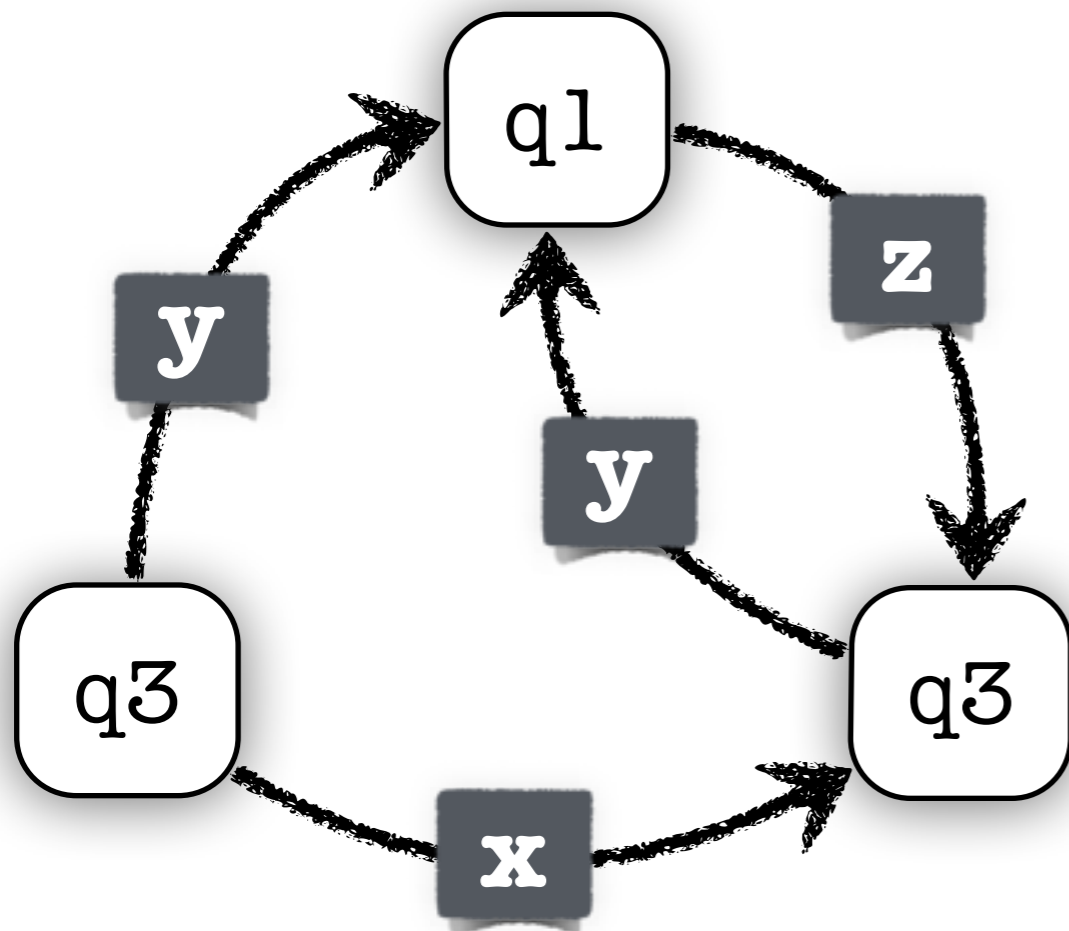
Dynamic Register Automata



Verification of Dynamic Register Automata

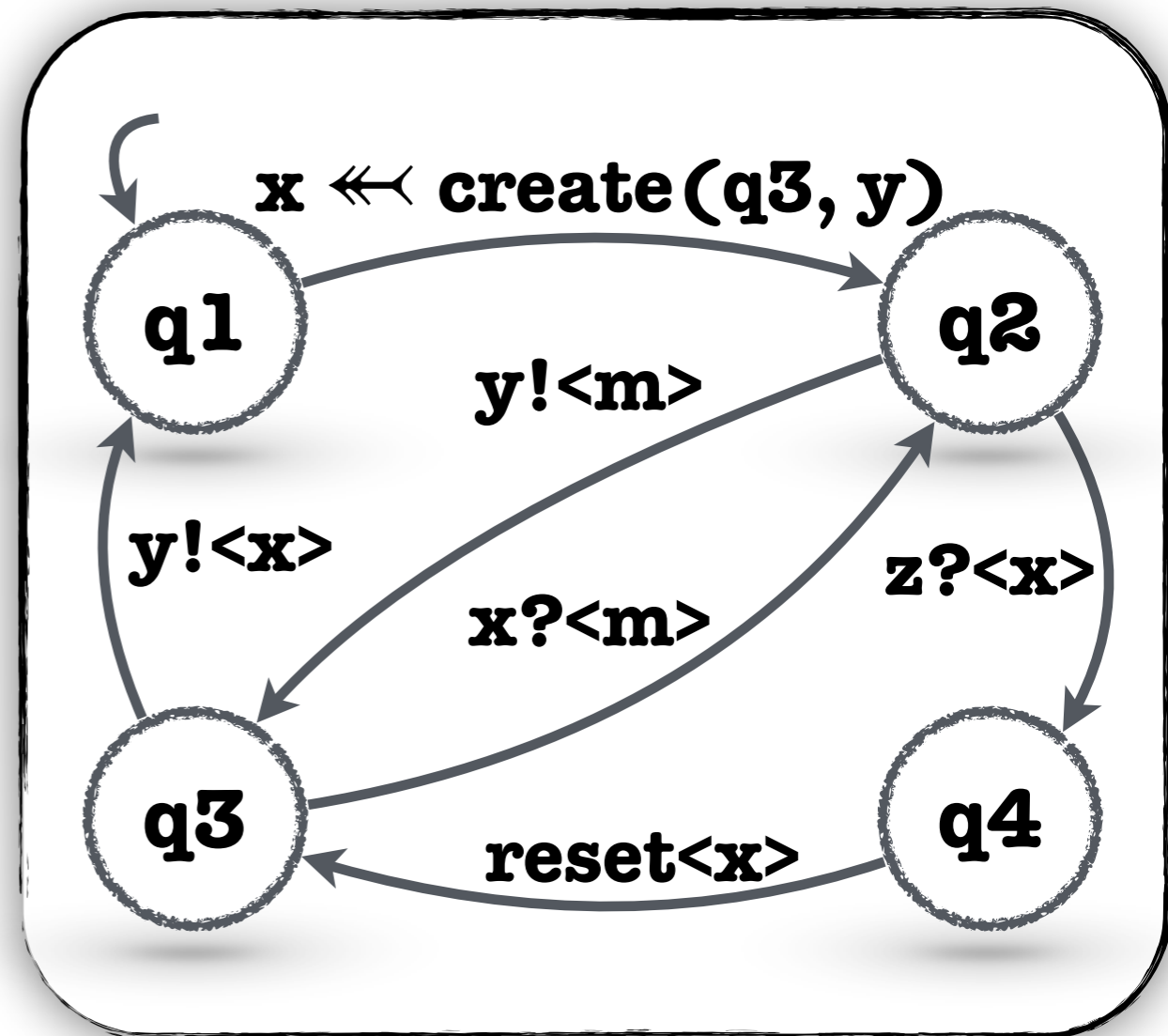
Formal Model

Configuration

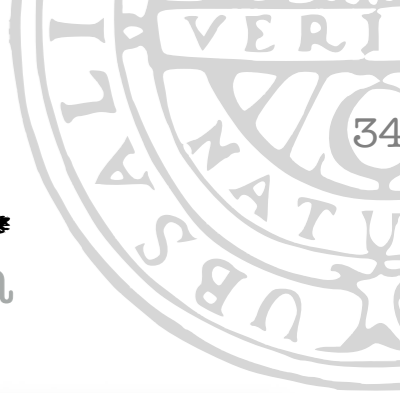


Communication graph

Process Model



Dynamic Register Automata

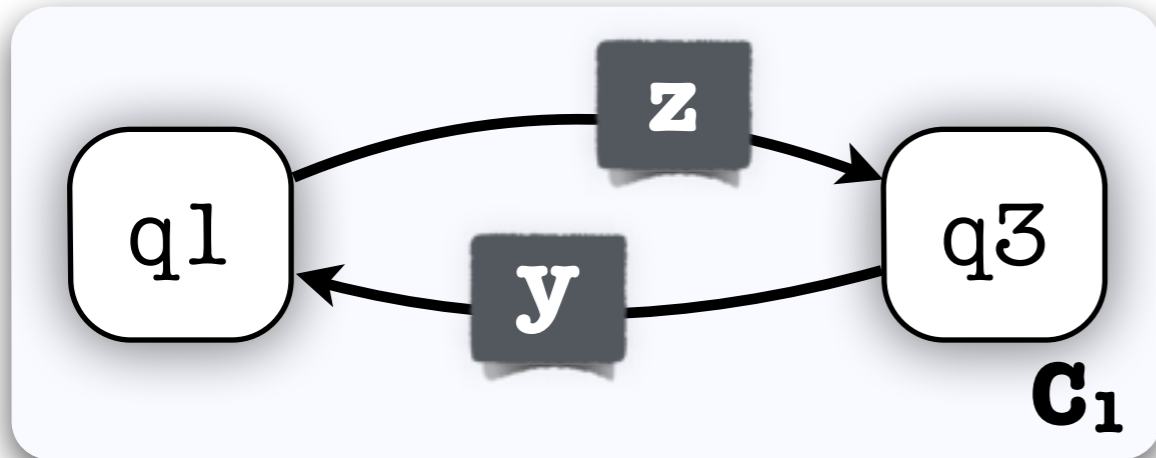


Verification of Dynamic Register Automata

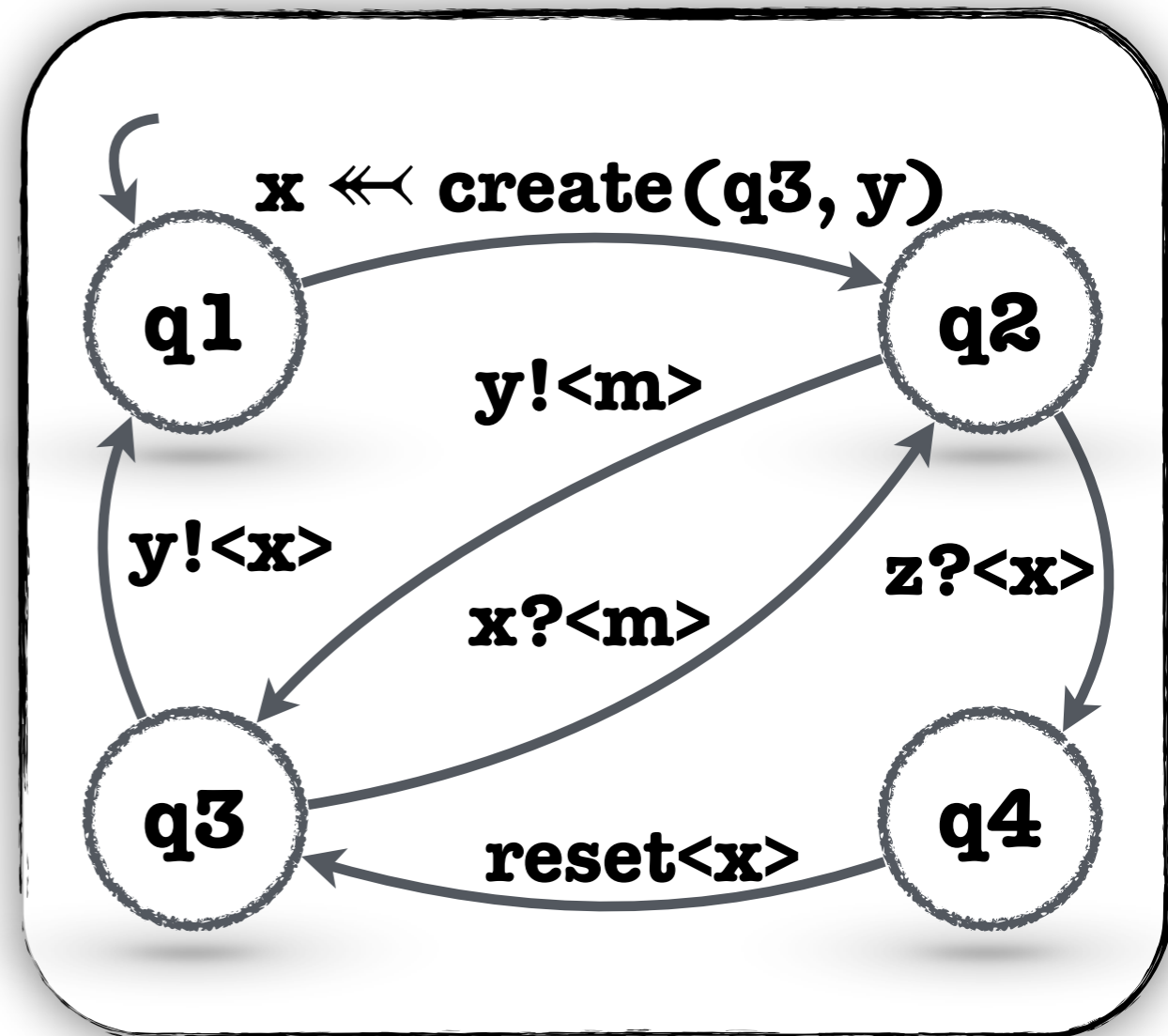
Formal Model

Configuration

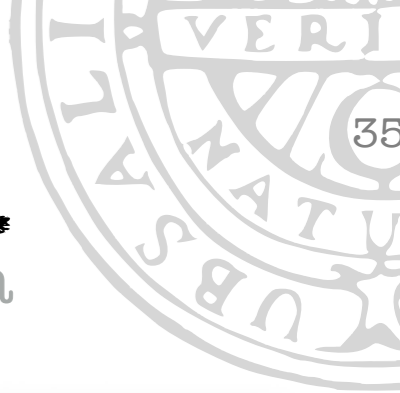
Transition Relation



Process Model



Dynamic Register Automata



Verification of Dynamic Register Automata

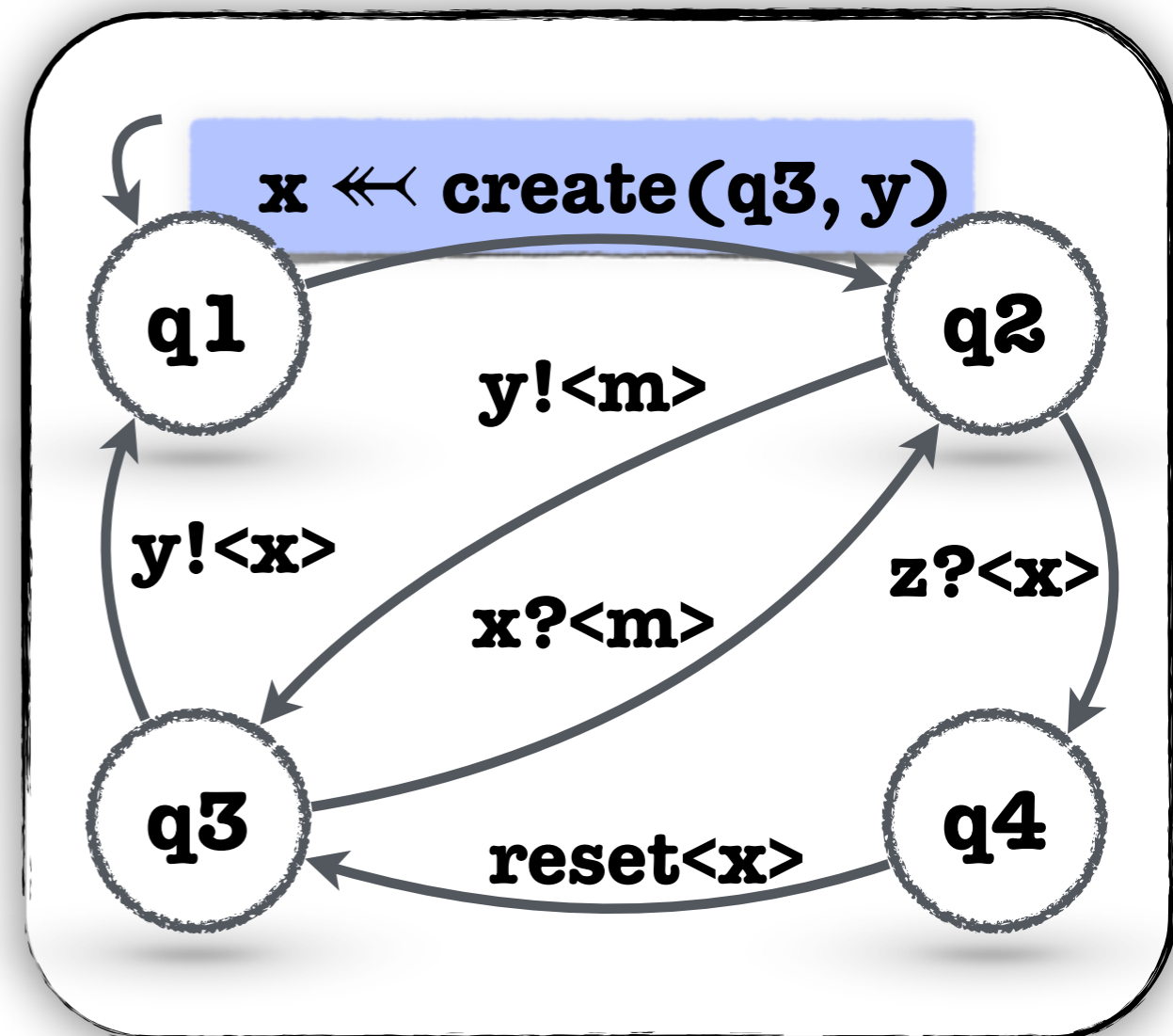
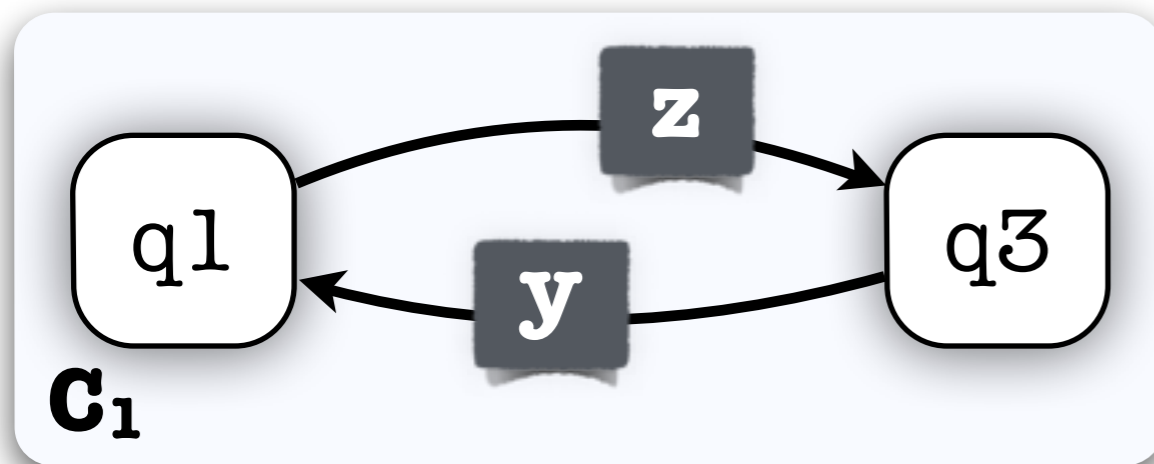
Formal Model

Configuration

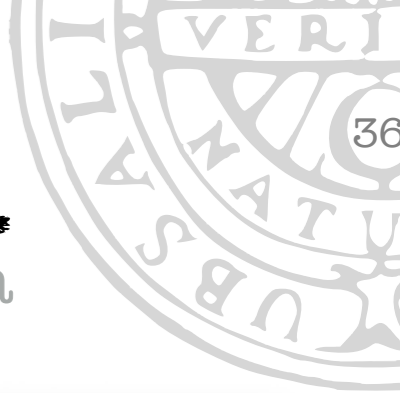
Transition Relation

Process Creation

Process Model



Dynamic Register Automata



Verification of Dynamic Register Automata

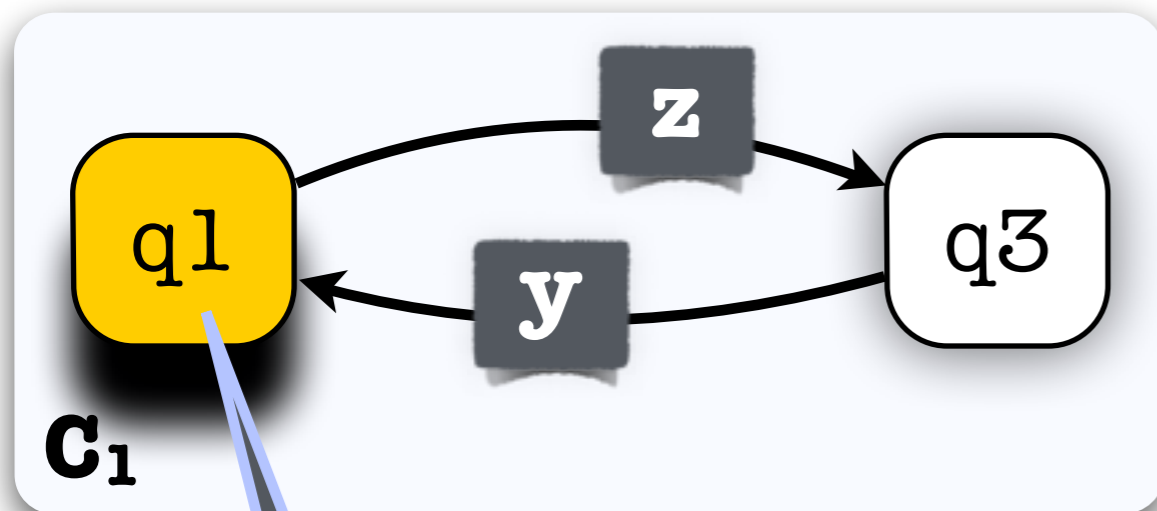
Formal Model

Configuration

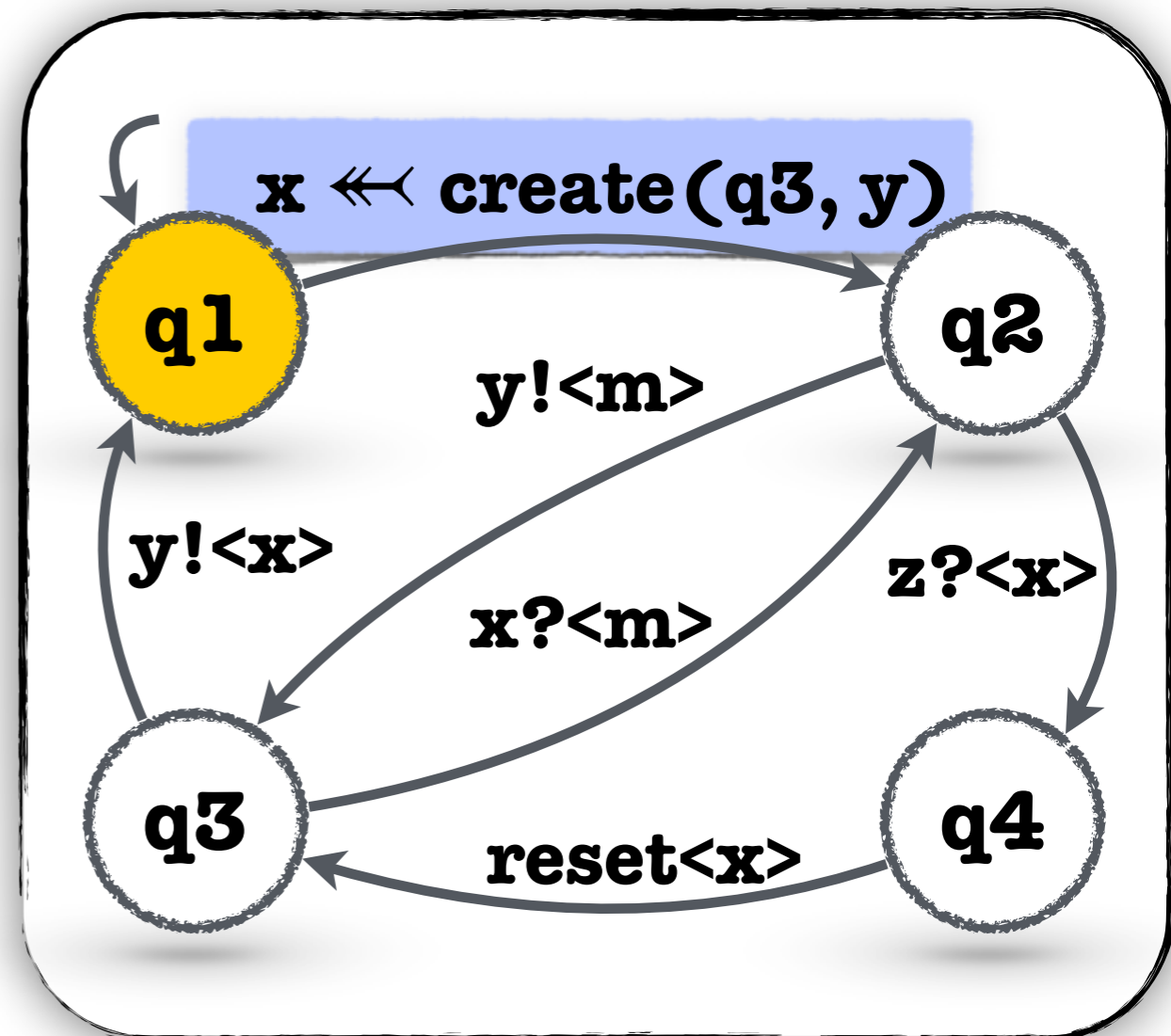
Transition Relation

Process Creation

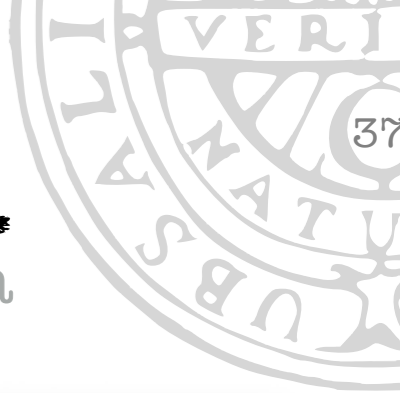
Process Model



Creating Process



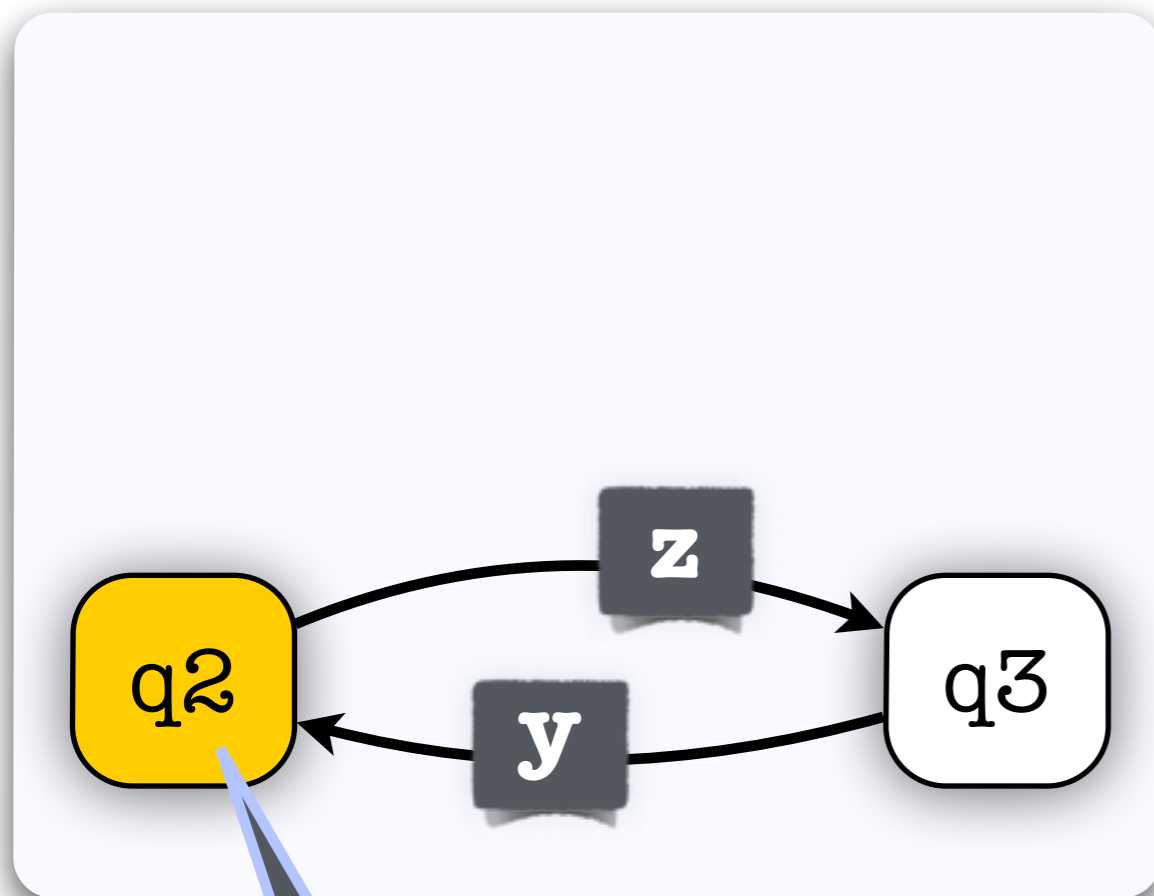
Dynamic Register Automata



Verification of Dynamic Register Automata

Formal Model

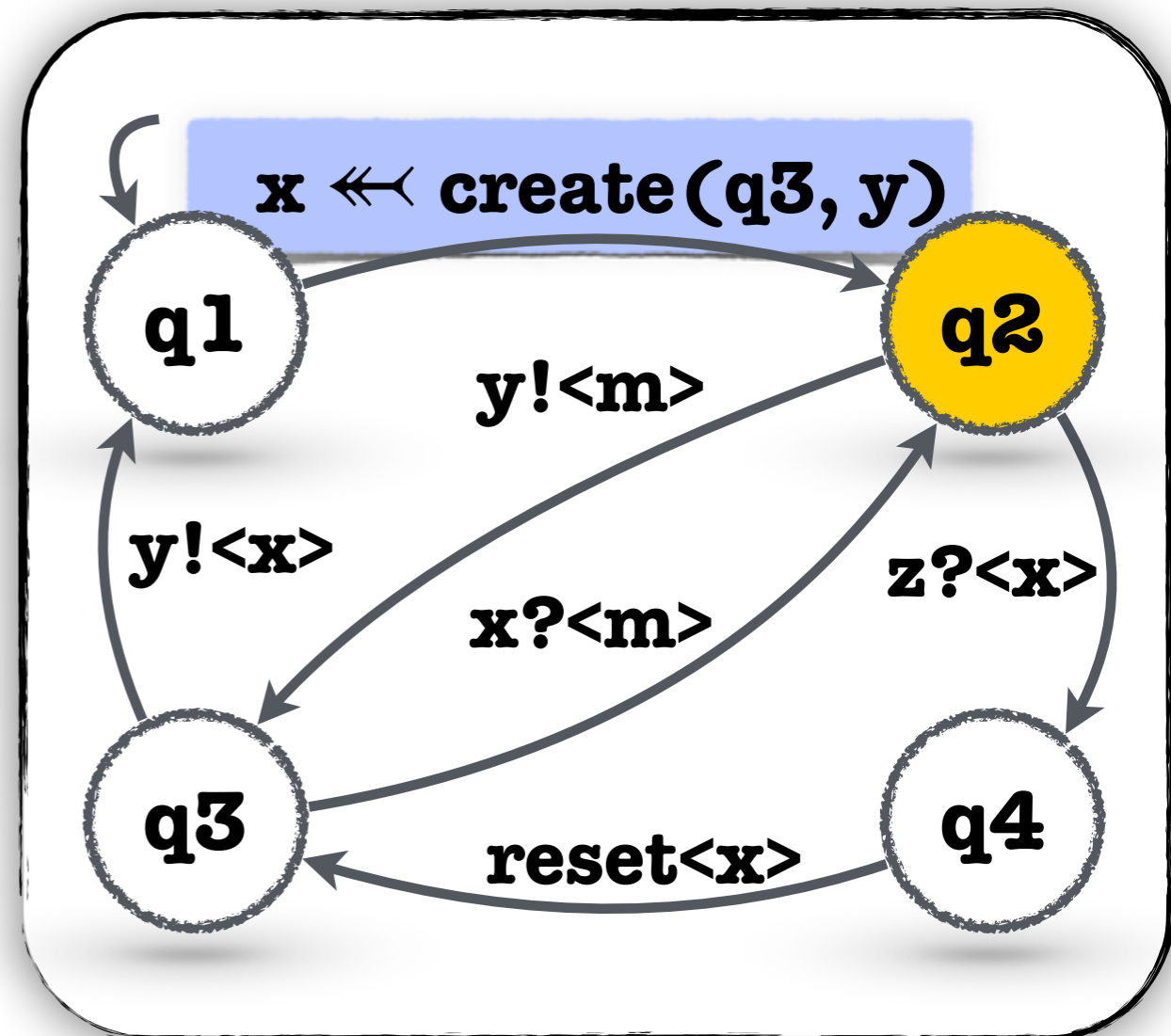
Configuration
Transition Relation



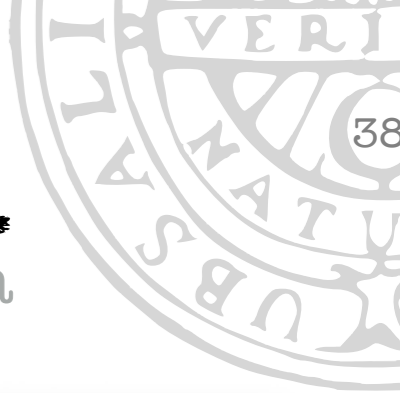
Creating Process

Process Model

Process Creation



Dynamic Register Automata

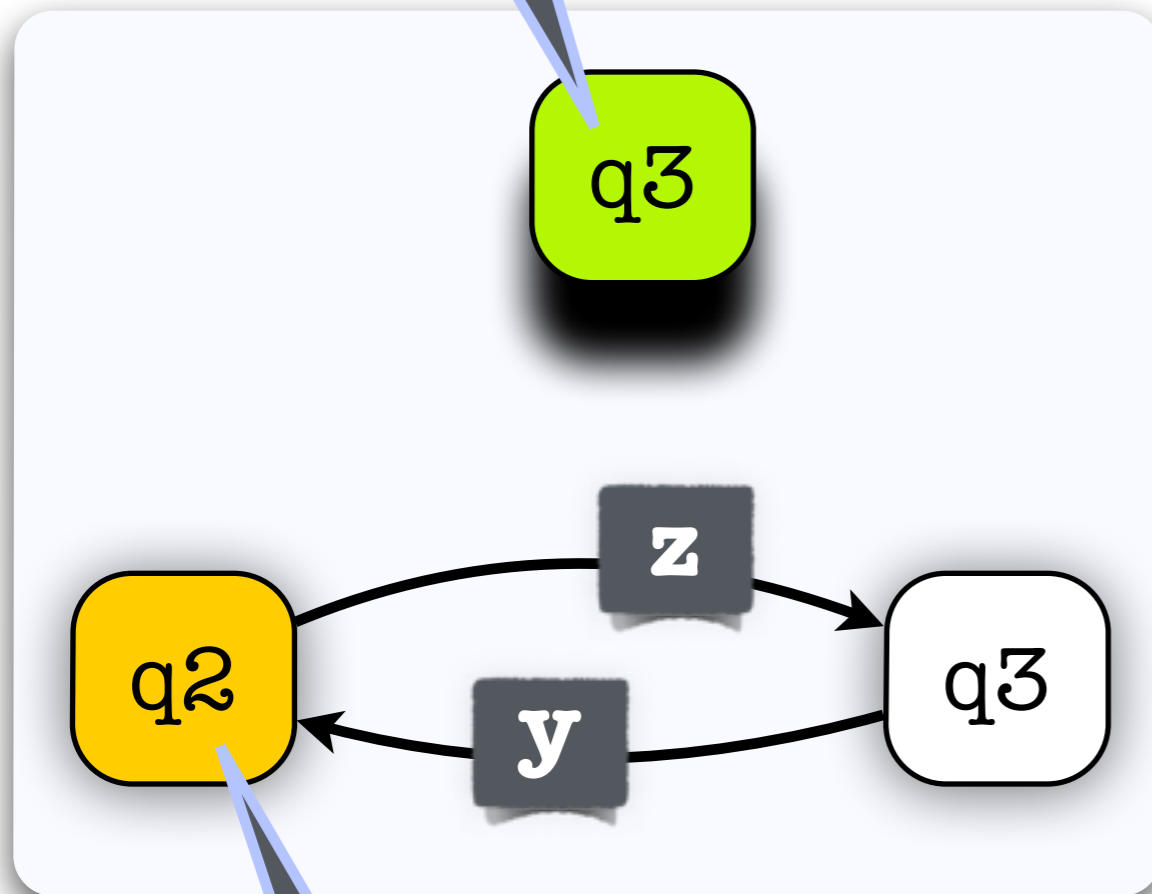


Verification of Dynamic Register Automata

Formal Model

Configuration
Transition Relation

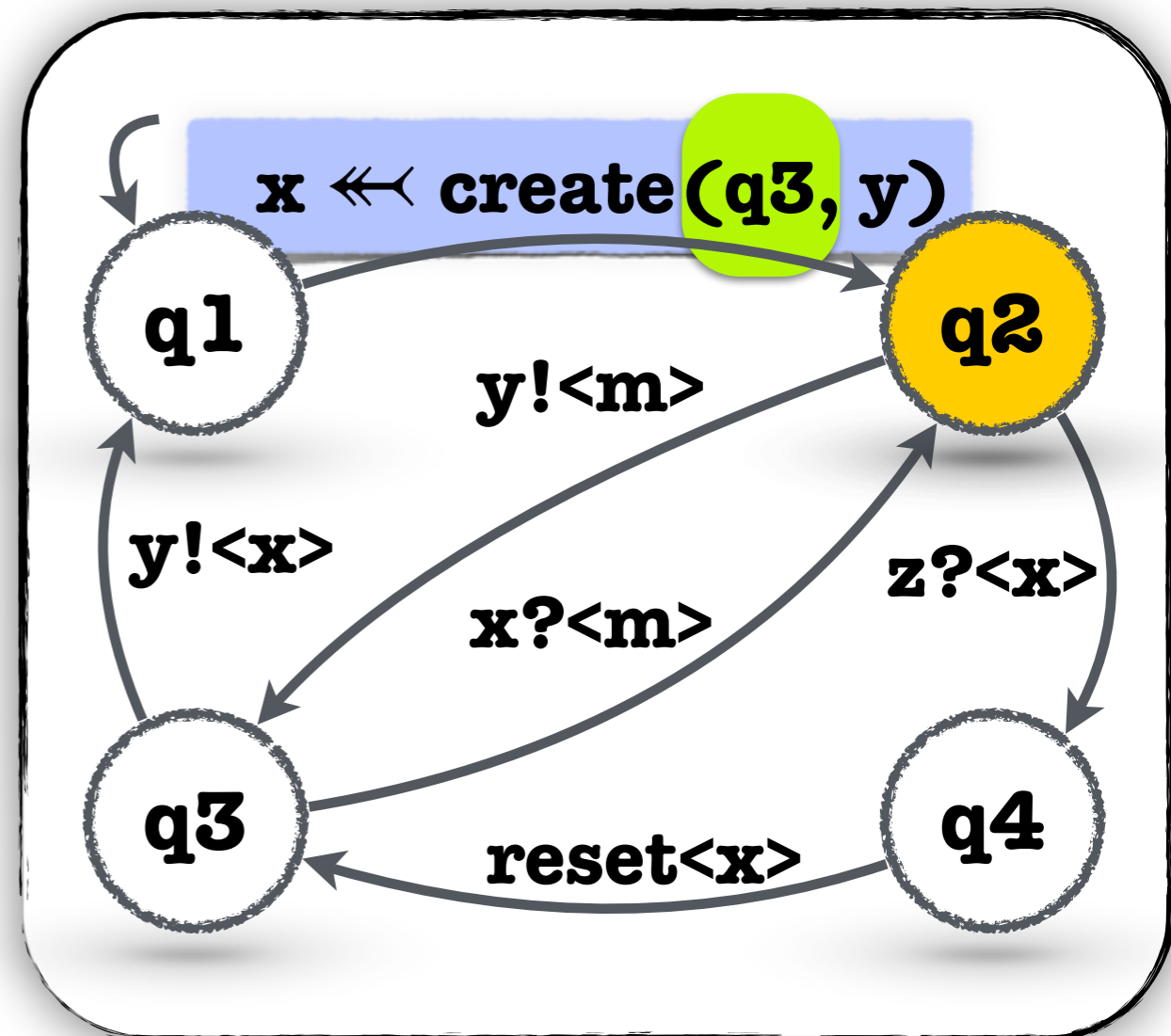
Created Process



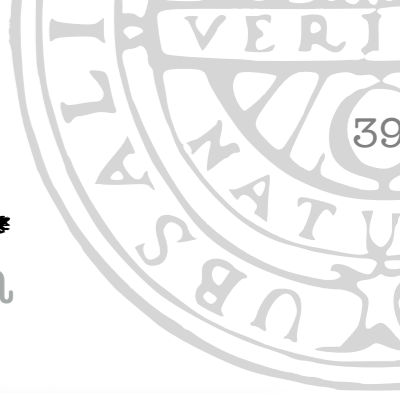
Creating Process

Process Model

Process Creation



Dynamic Register Automata

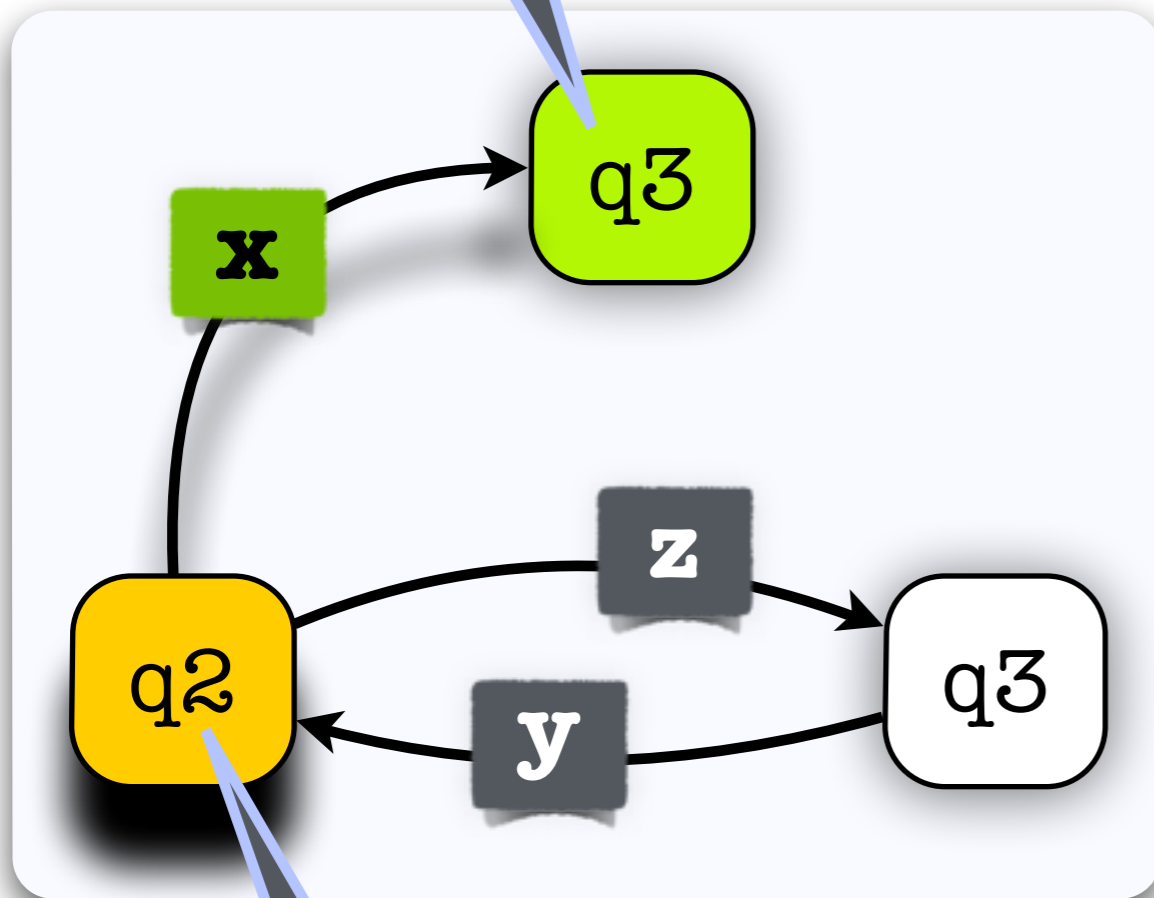


Verification of Dynamic Register Automata

Formal Model

Configuration
Transition Relation

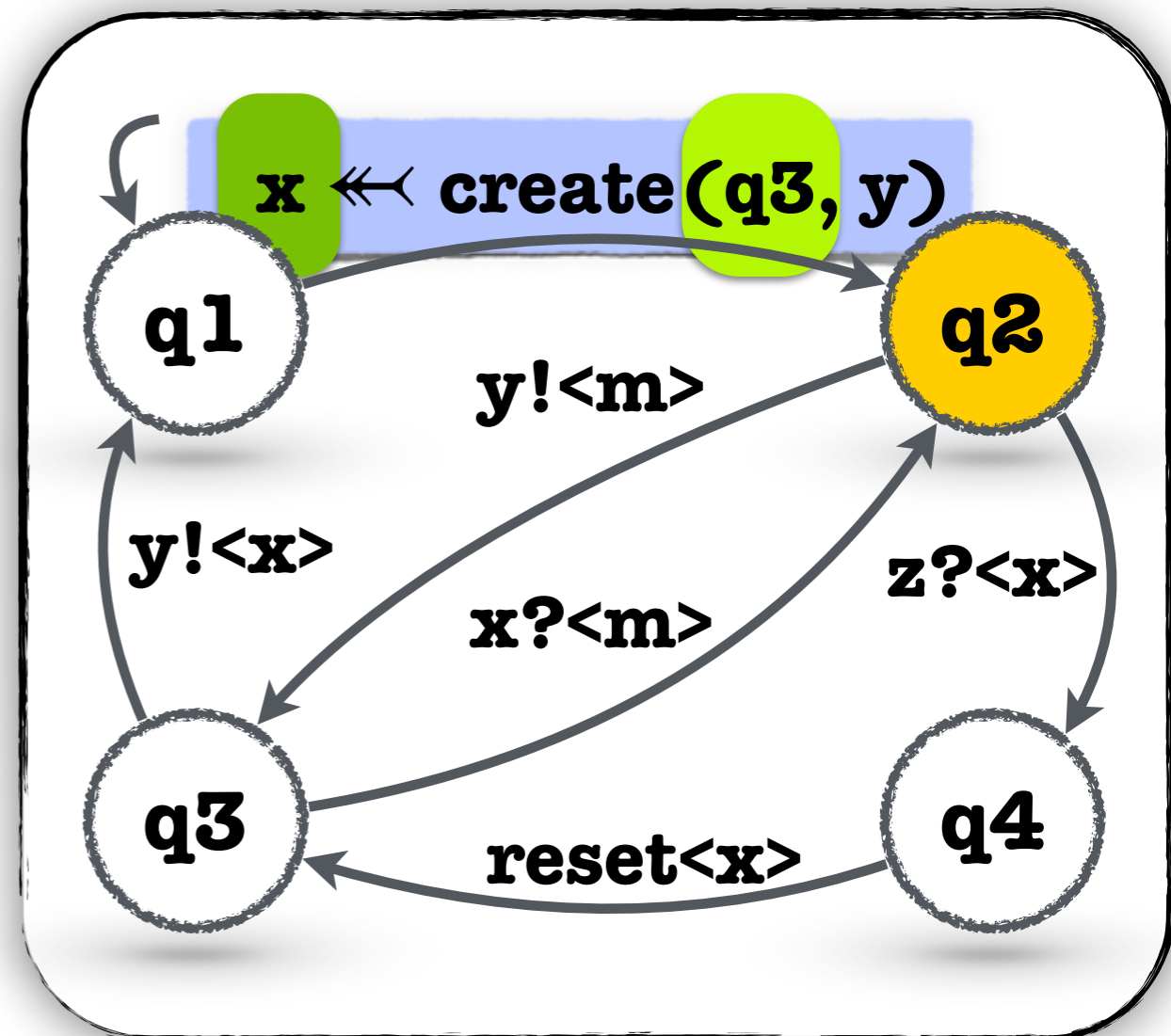
Created Process



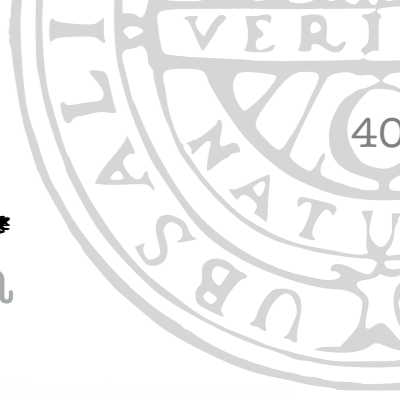
Creating Process

Process Model

Process Creation



Dynamic Register Automata

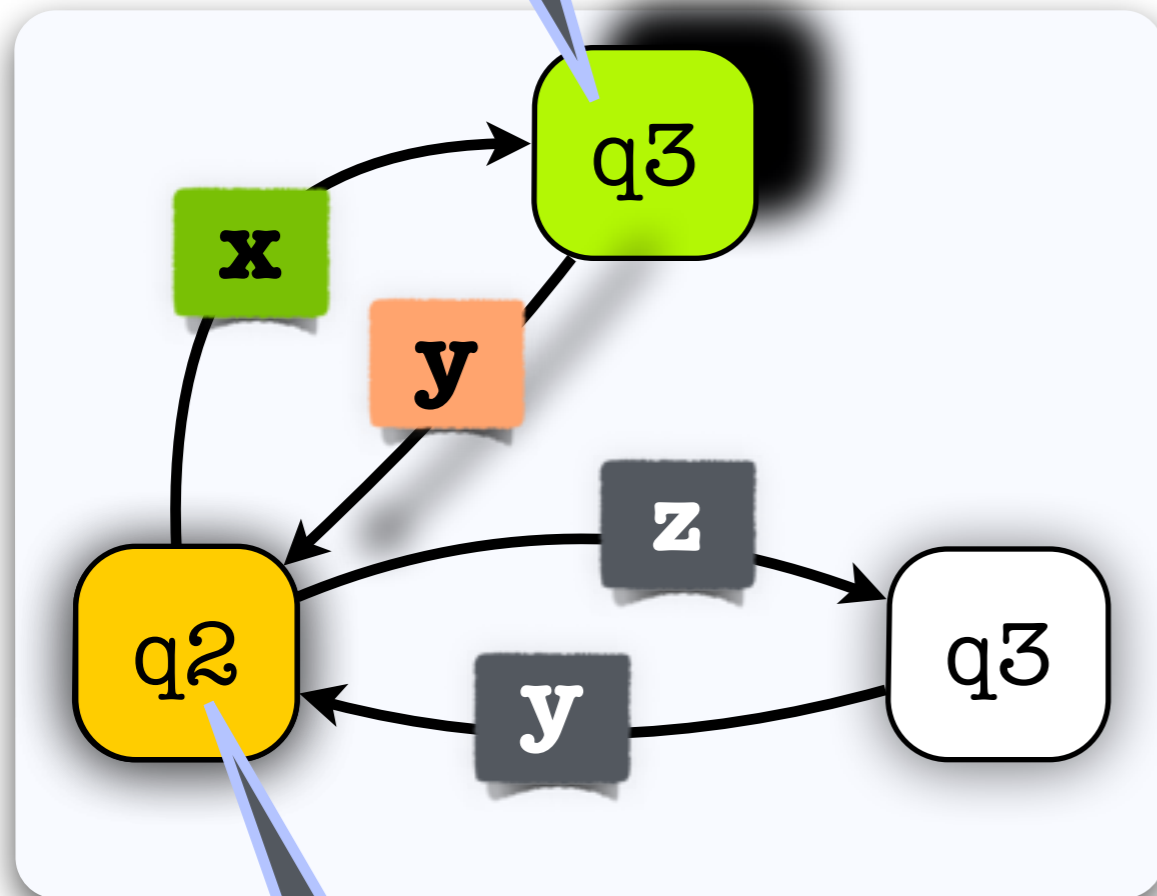


Verification of Dynamic Register Automata

Formal Model

Configuration
Transition Relation

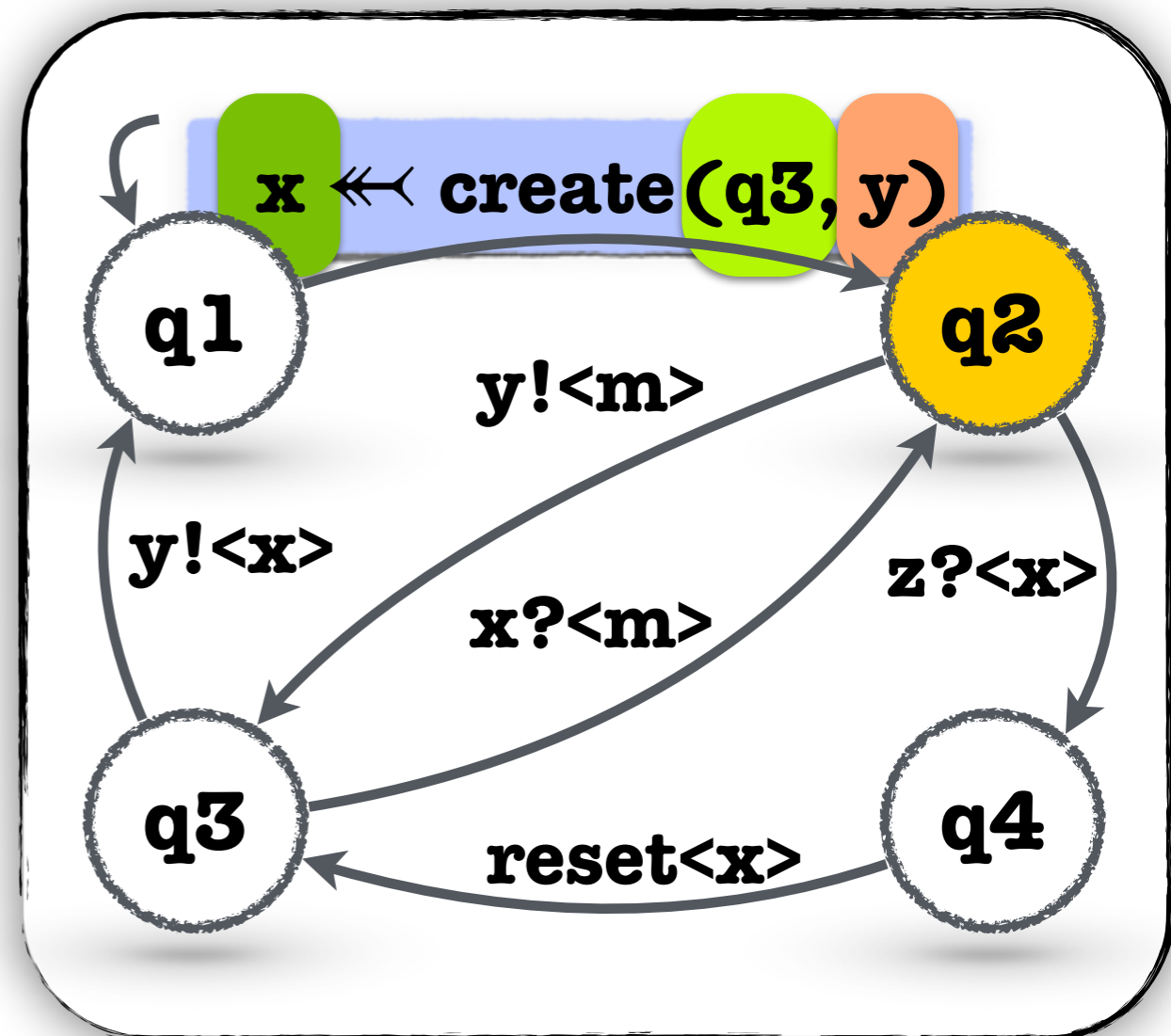
Created Process



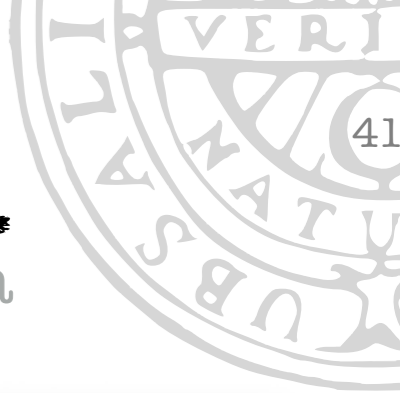
Creating Process

Process Model

Process Creation



Dynamic Register Automata

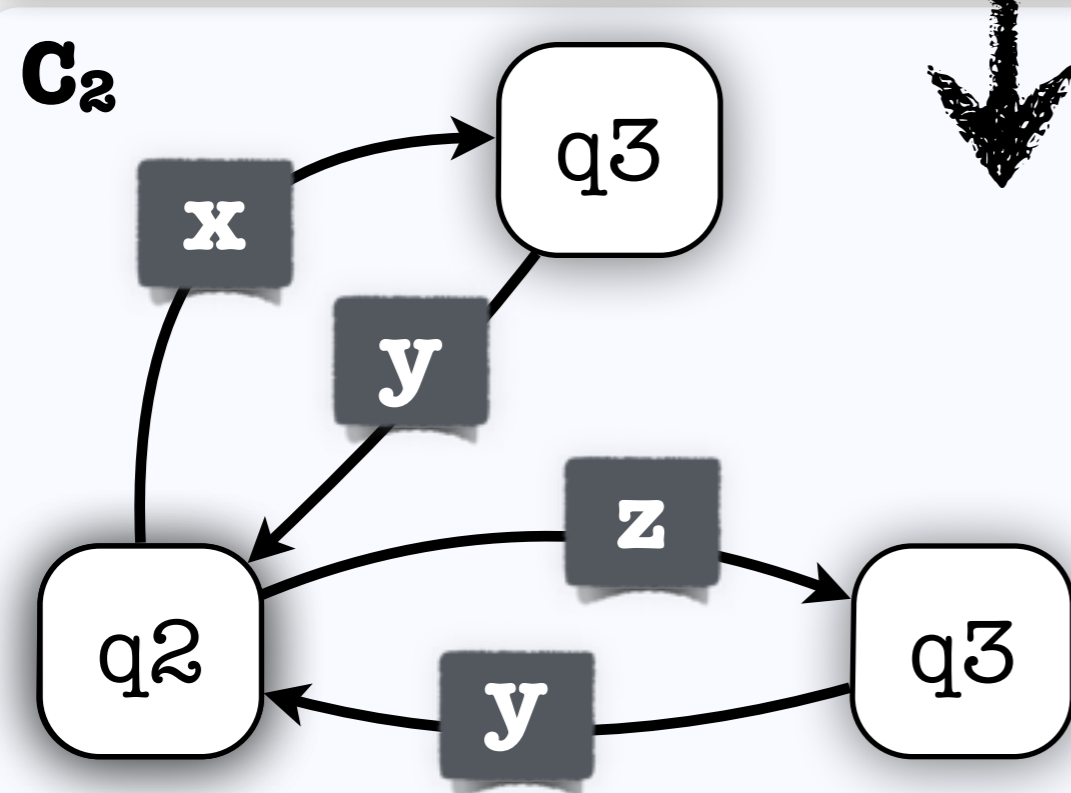
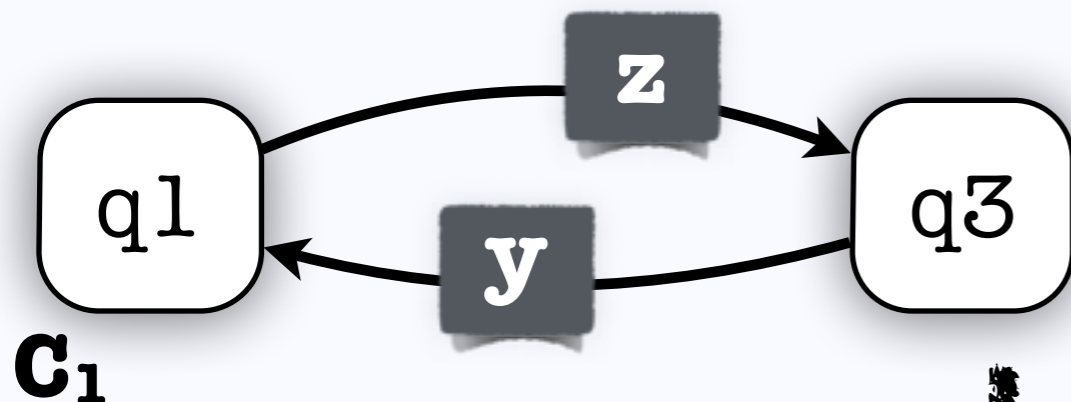


Verification of Dynamic Register Automata

Formal Model

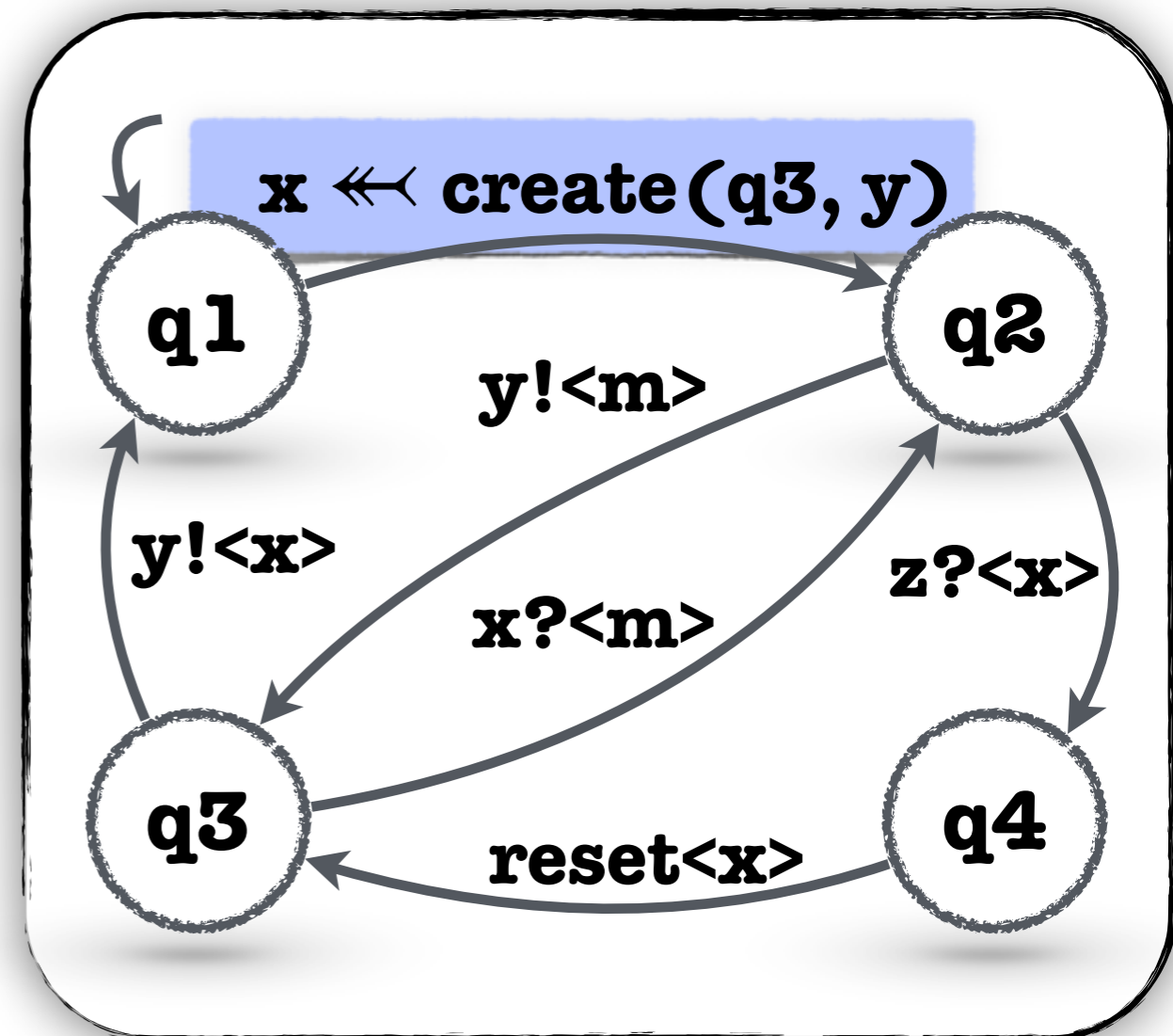
Configuration

Transition Relation

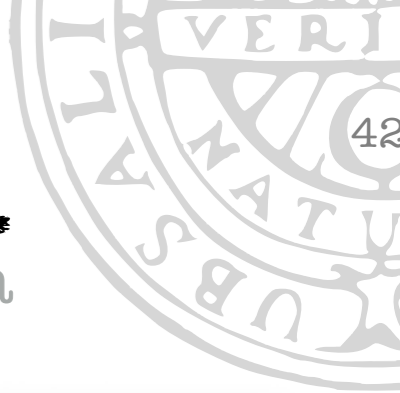


Process Model

Process Creation



Dynamic Register Automata



Verification of Dynamic Register Automata

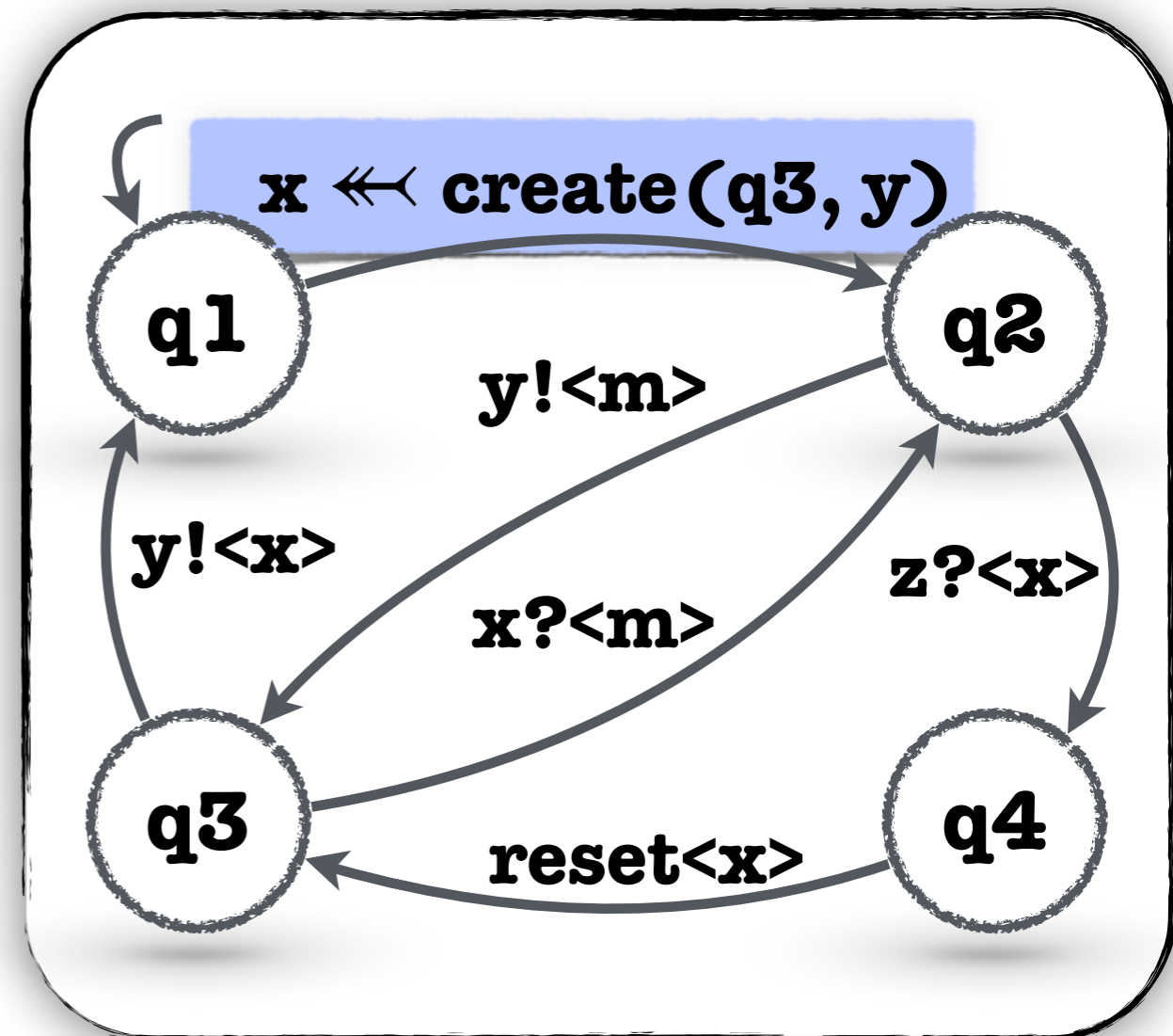
Formal Model

Configuration

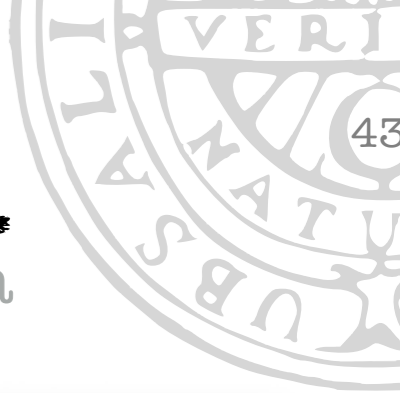
Transition Relation

Process Creation

Process Model



Dynamic Register Automata



Verification of Dynamic Register Automata

Formal Model

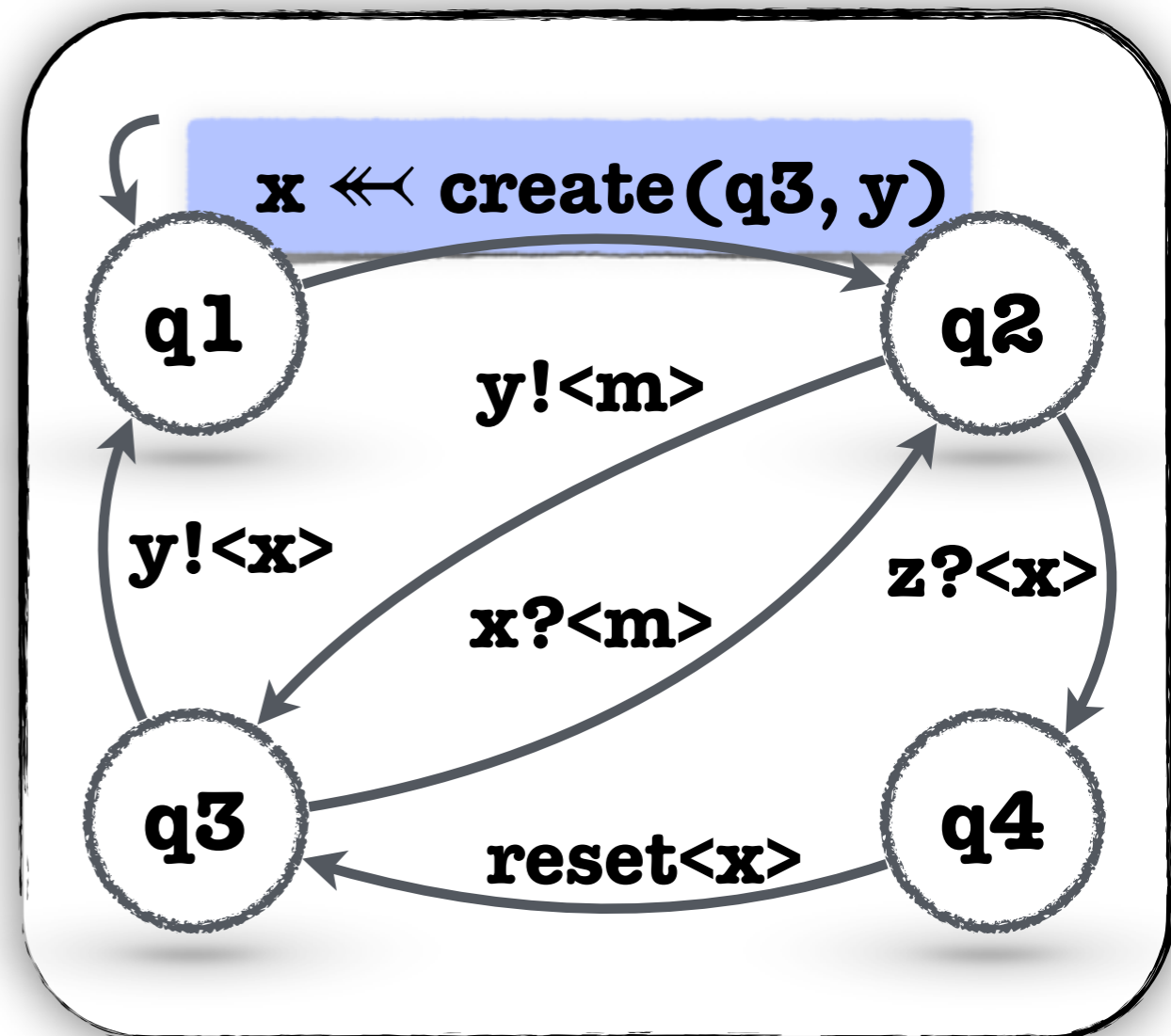
Configuration

Transition Relation

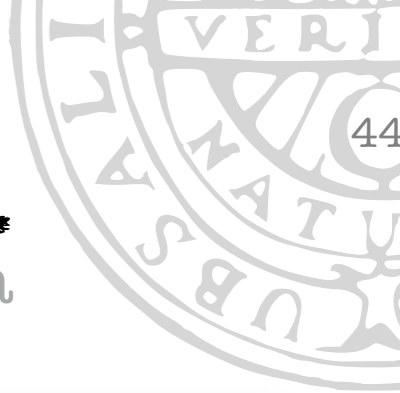
Process Creation

Send & Receive ID

Process Model



Dynamic Register Automata



Verification of Dynamic Register Automata

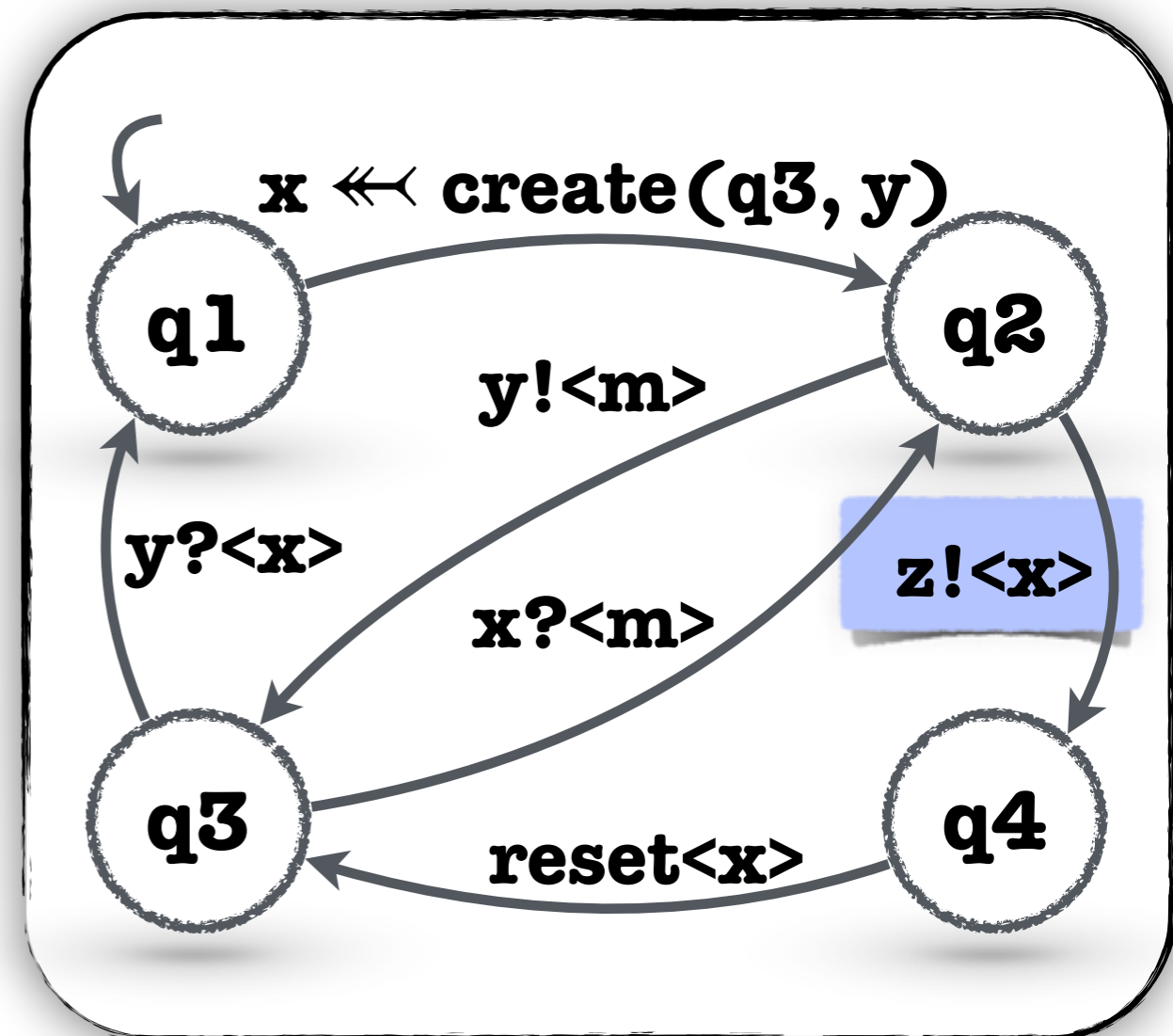
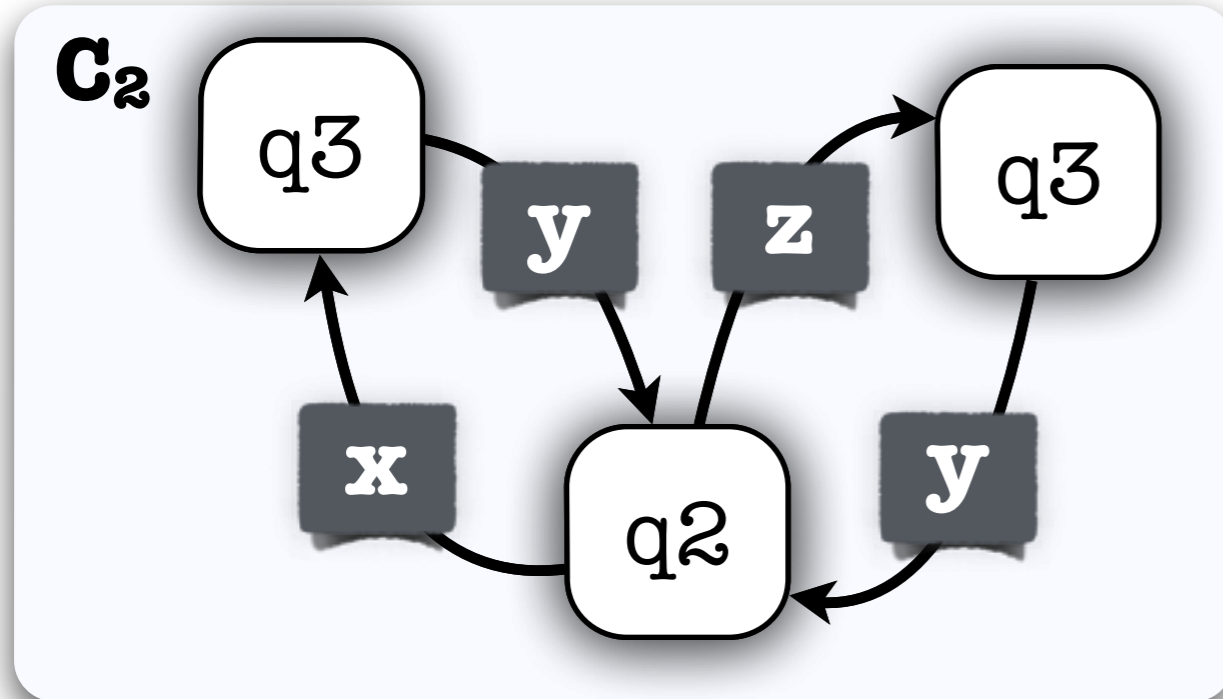
Formal Model

Configuration

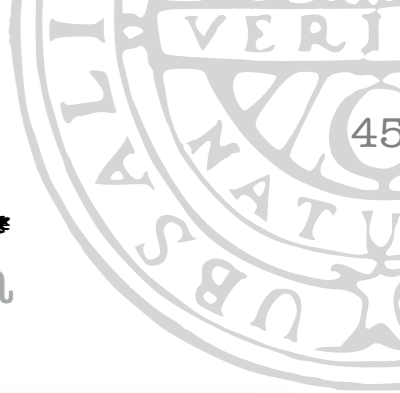
Transition Relation

Send & Receive ID

Process Model



Dynamic Register Automata



Verification of Dynamic Register Automata

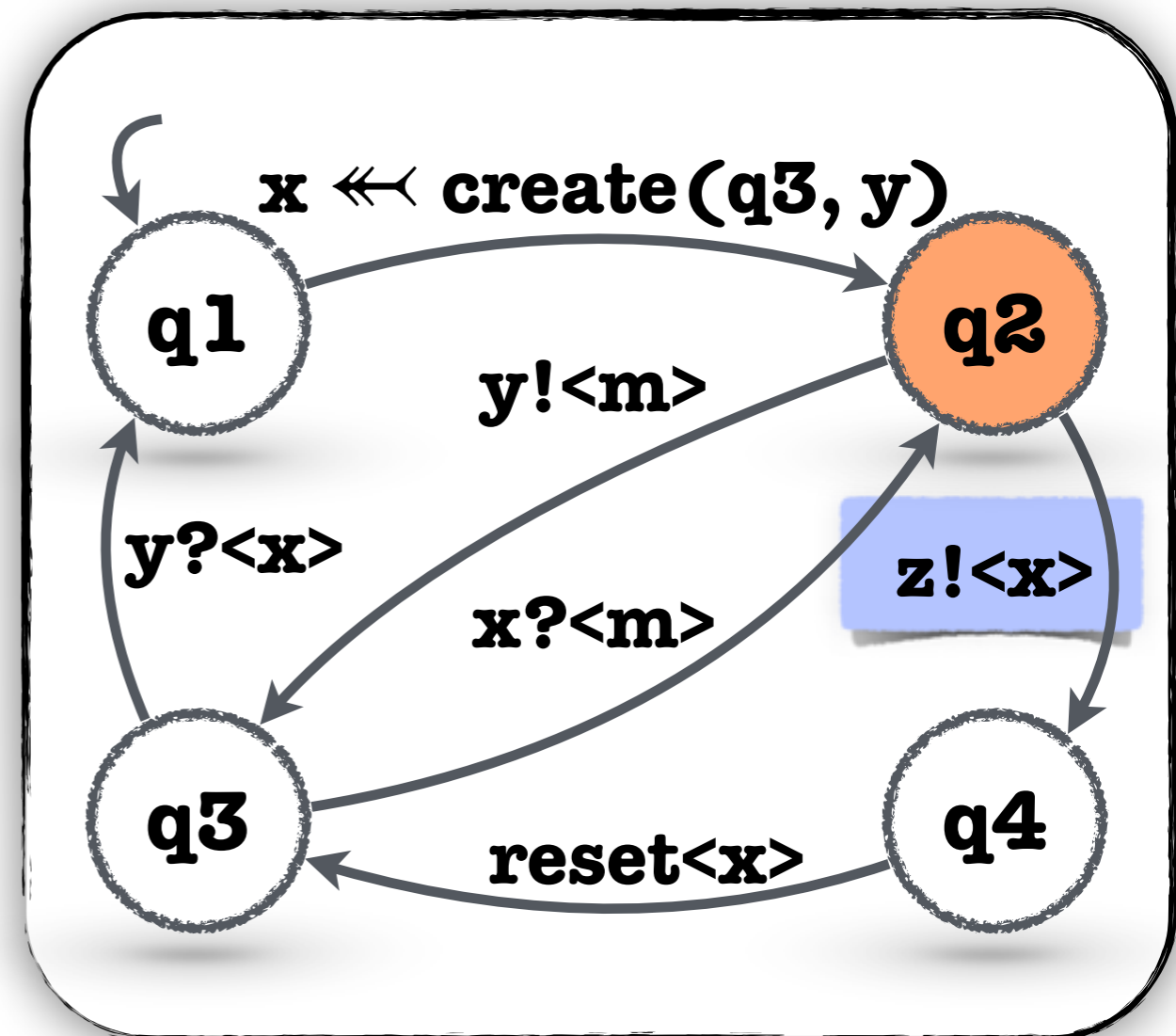
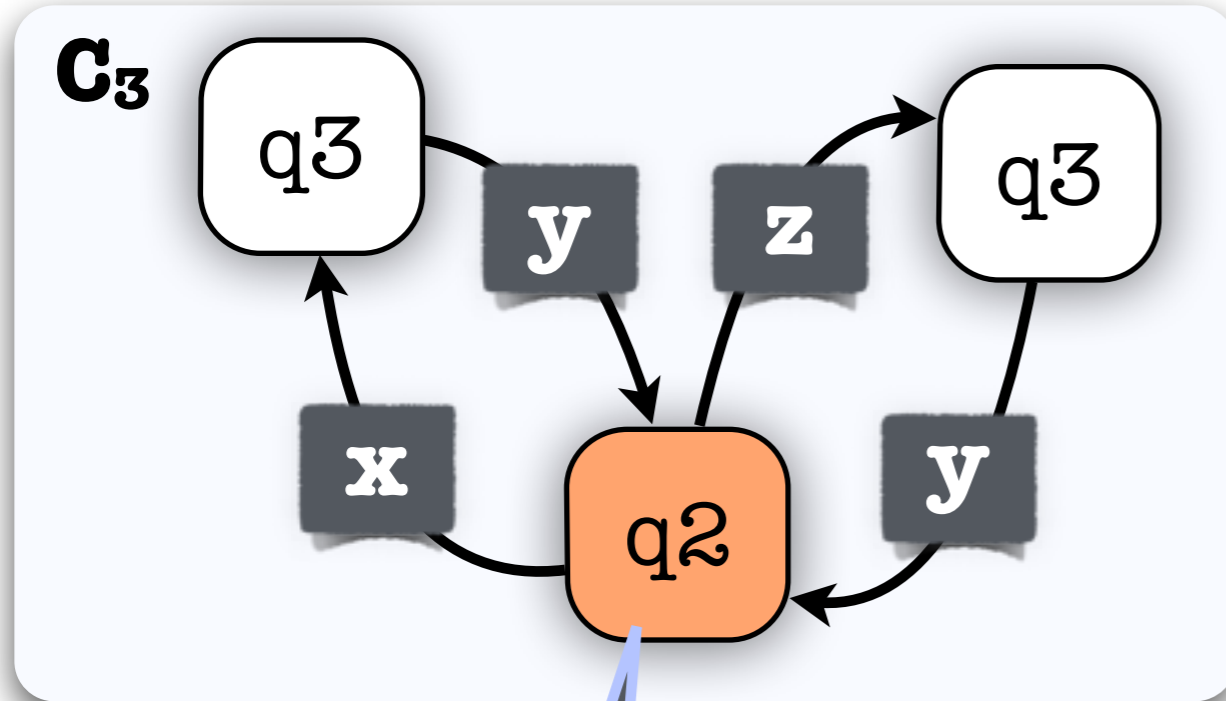
Formal Model

Configuration

Transition Relation

Send & Receive ID

Process Model



Sender

Dynamic Register Automata



Verification of Dynamic Register Automata

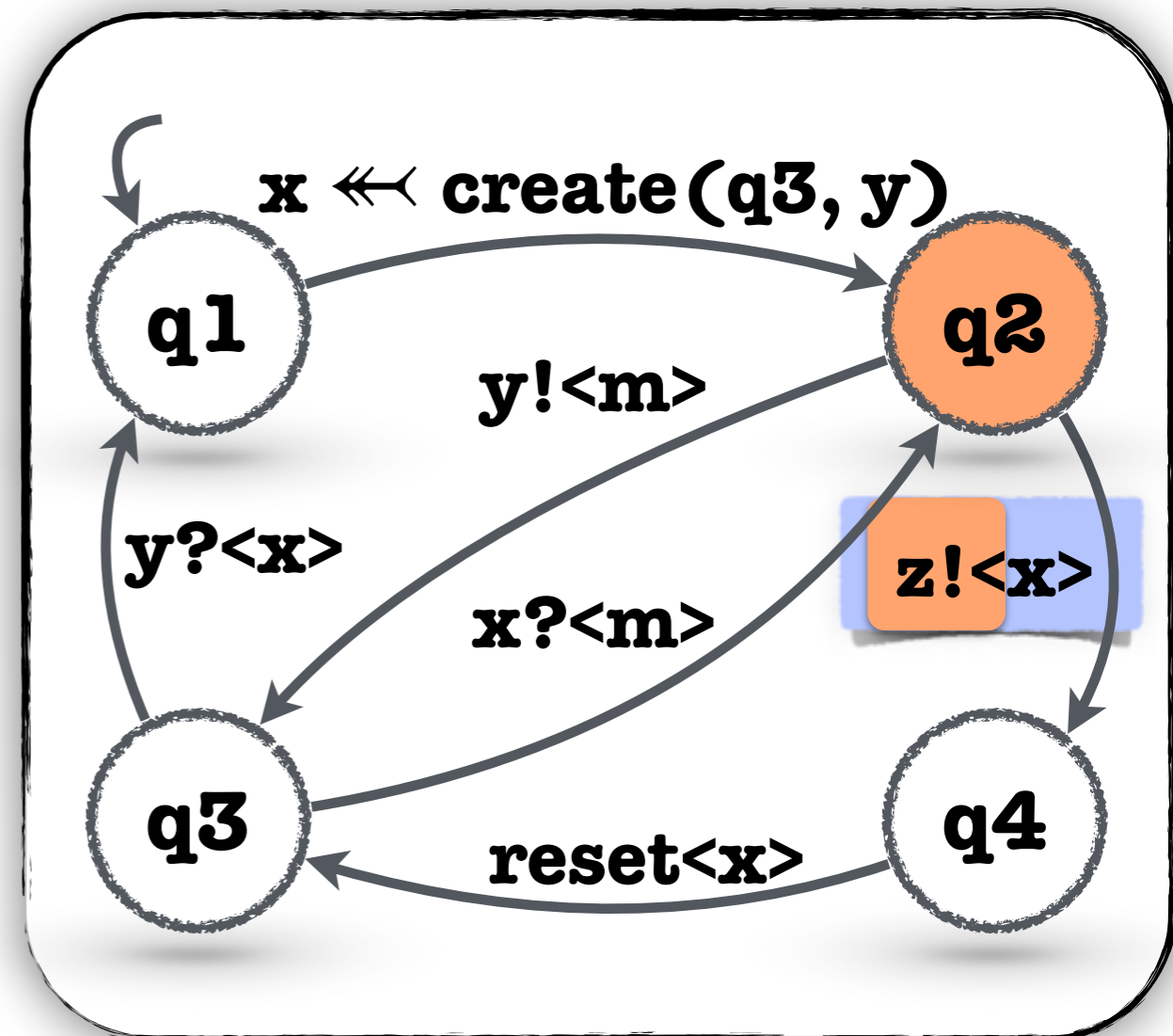
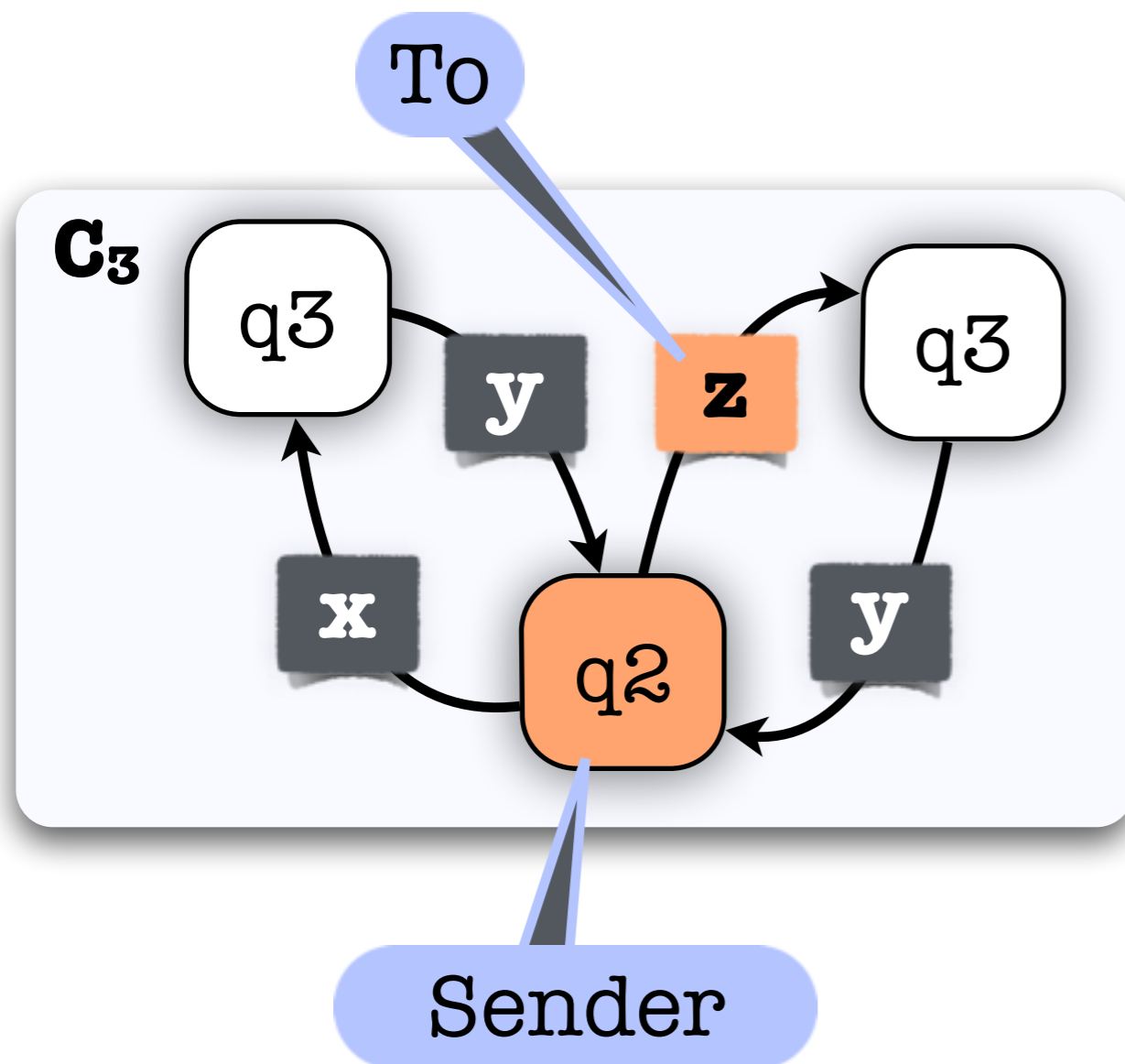
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Configuration

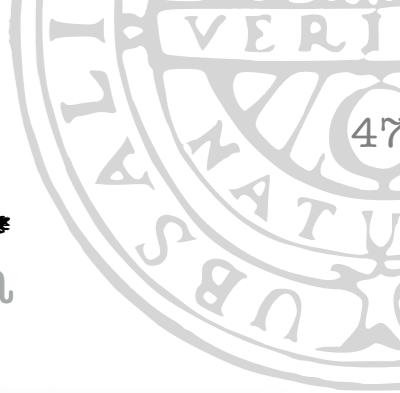
Transition Relation

Send & Receive ID

Process Model



Dynamic Register Automata



Verification of Dynamic Register Automata

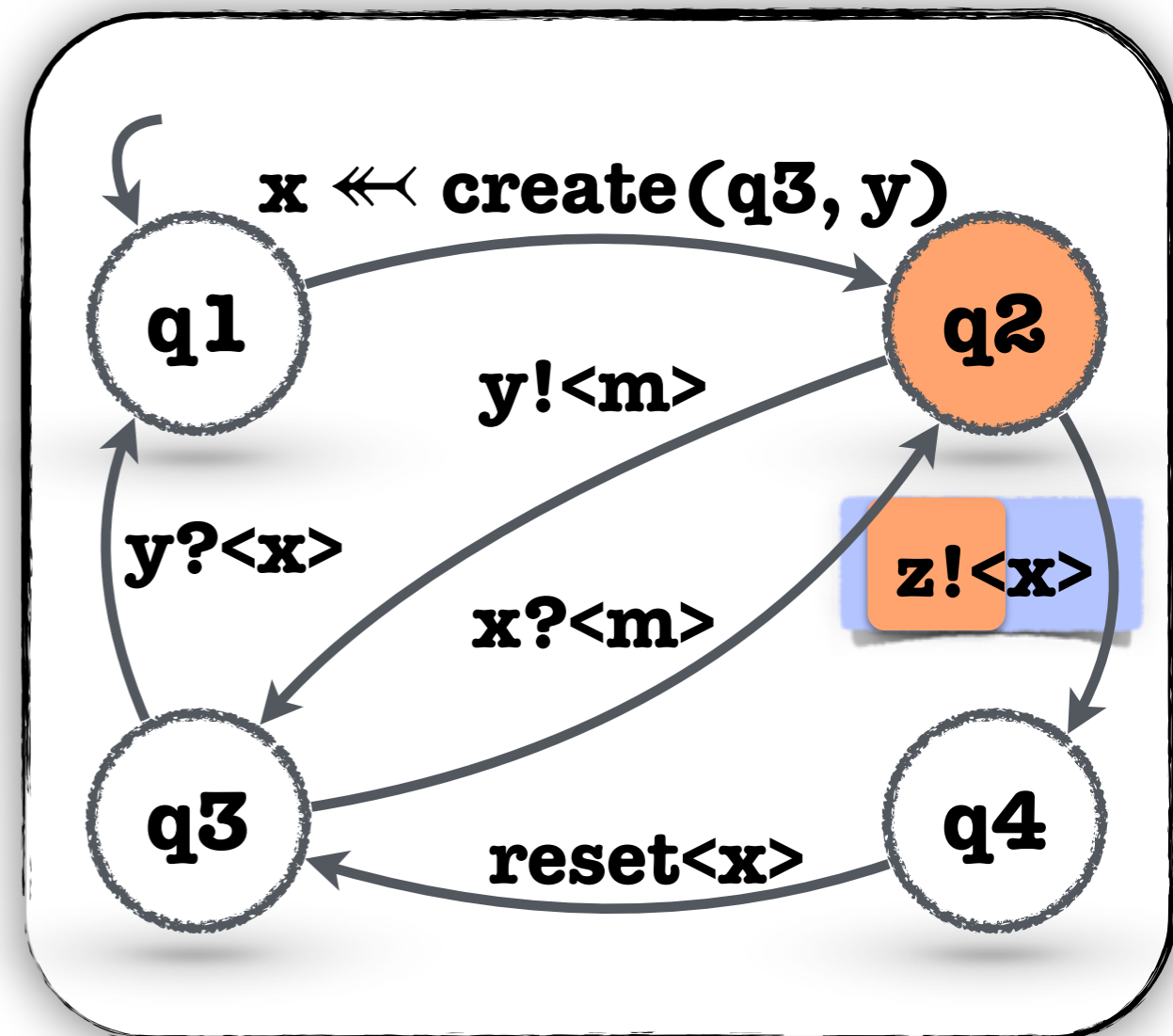
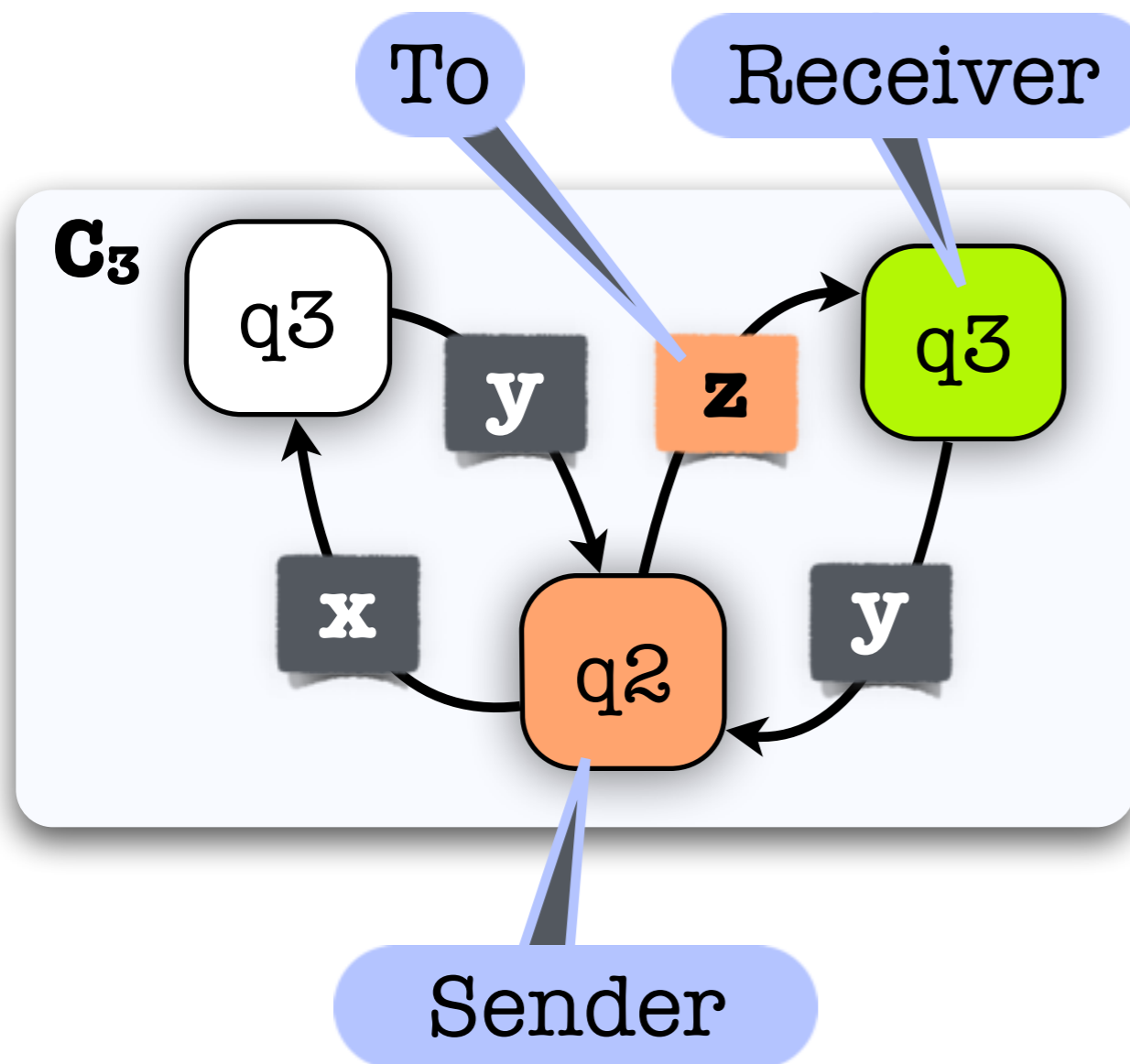
Formal Model

Configuration

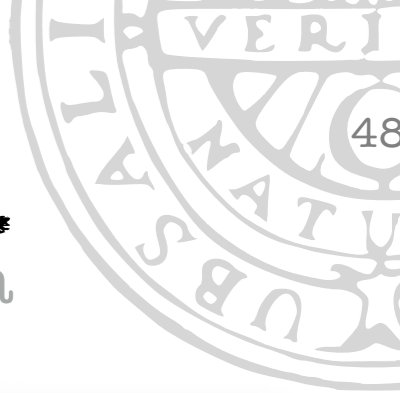
Transition Relation

Send & Receive ID

Process Model



Dynamic Register Automata



Formal Model

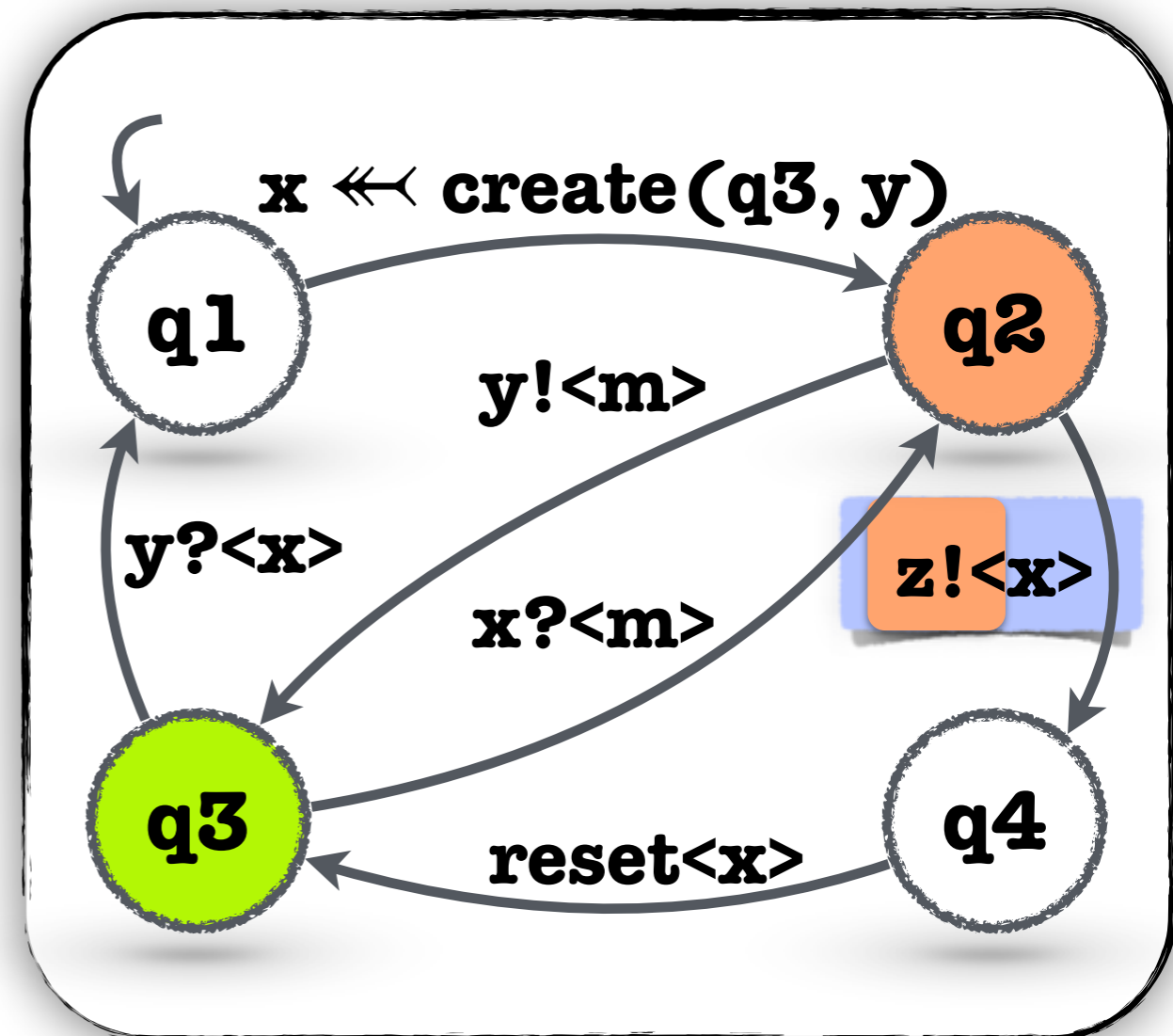
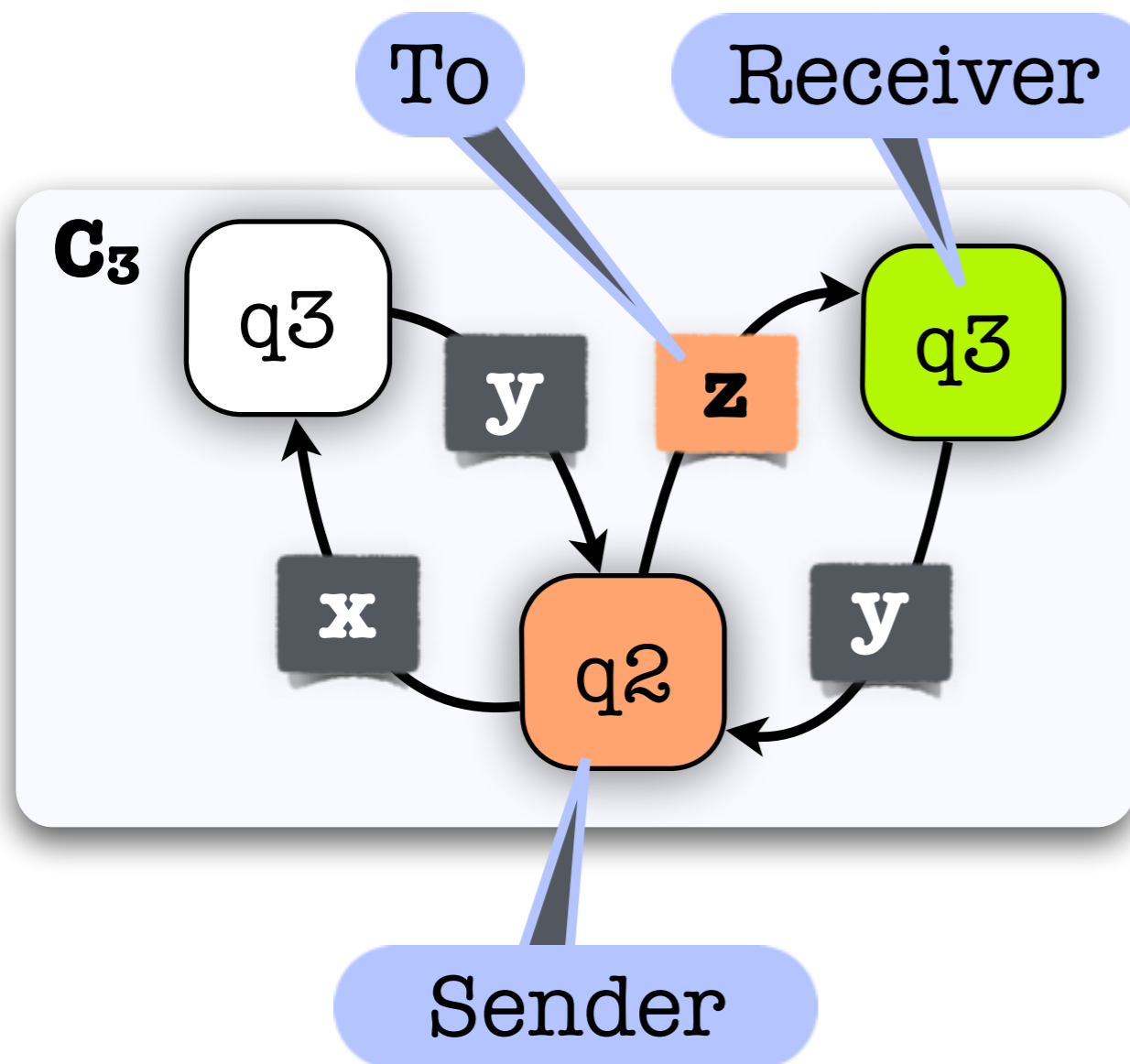
Verification of Dynamic Register Automata

Configuration

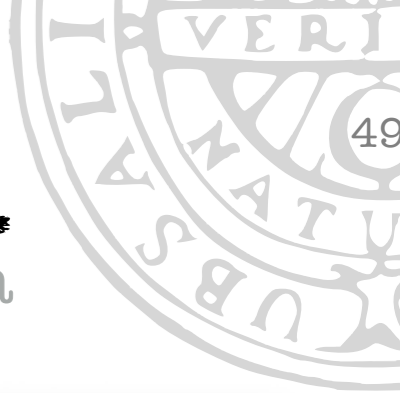
Transition Relation

Send & Receive ID

Process Model



Dynamic Register Automata



Formal Model

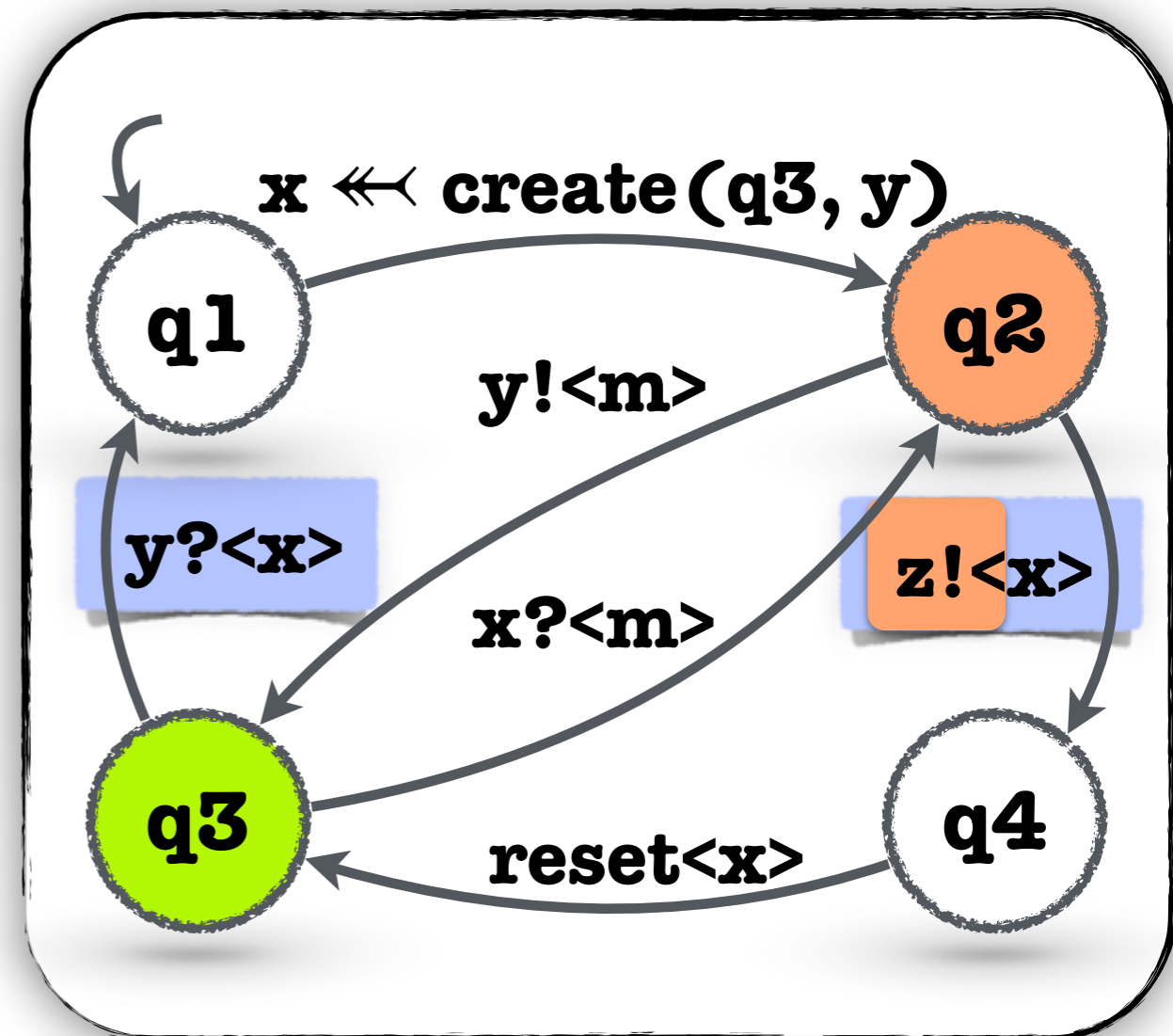
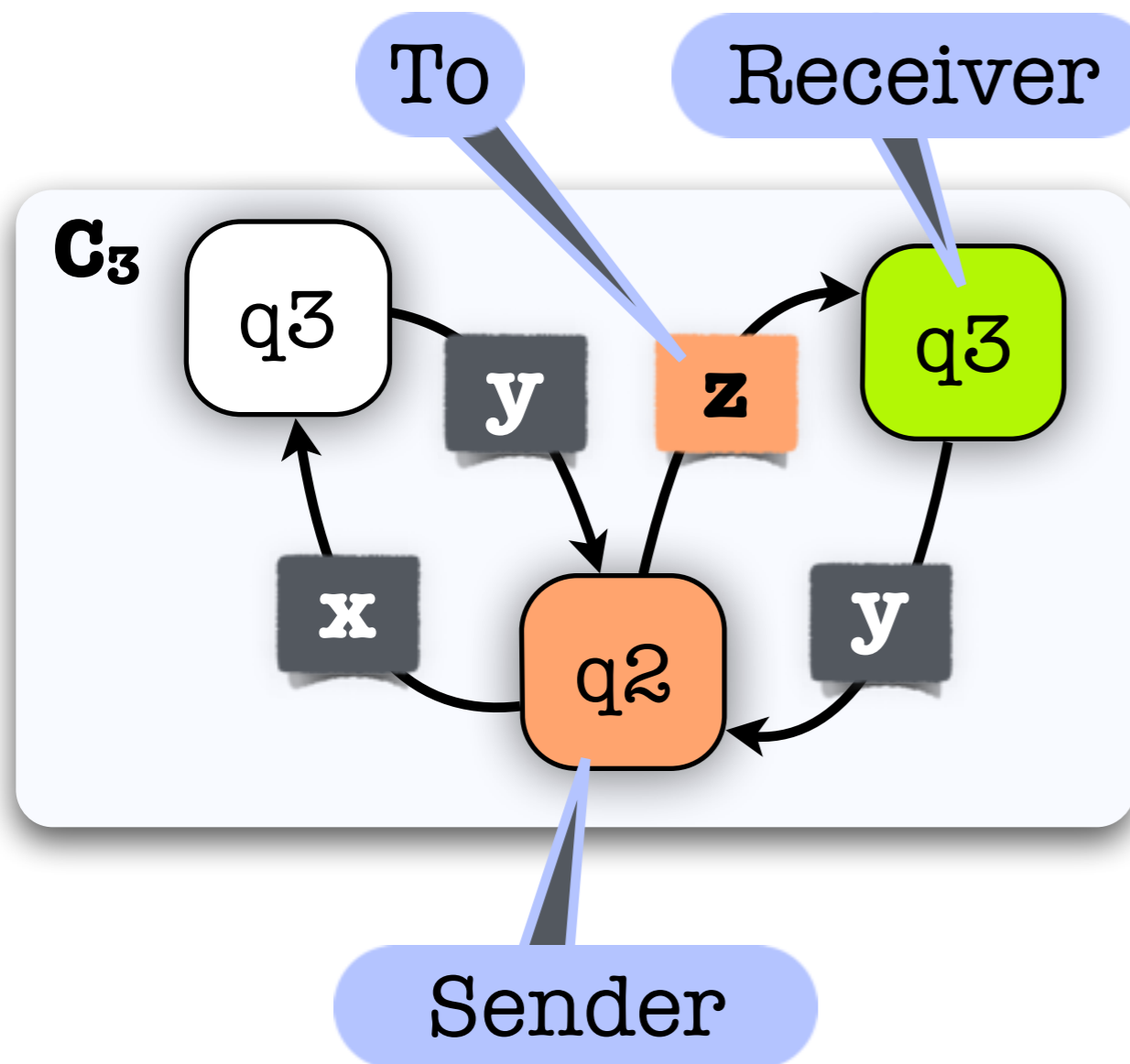
Verification of Dynamic Register Automata

Configuration

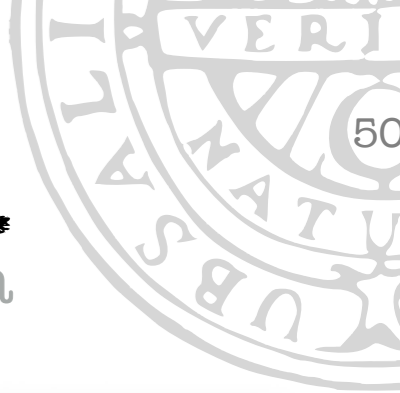
Transition Relation

Send & Receive ID

Process Model



Dynamic Register Automata



Formal Model

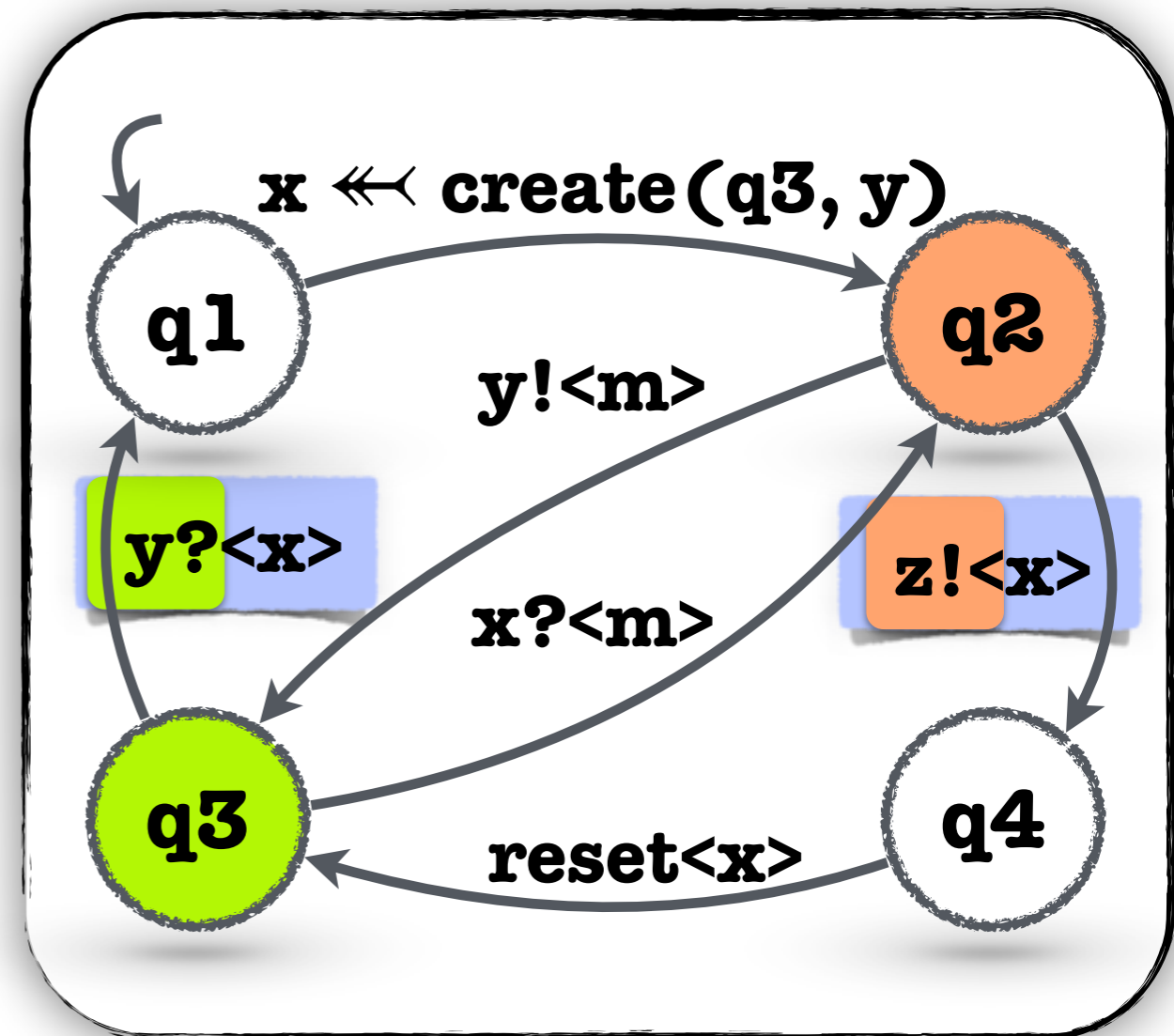
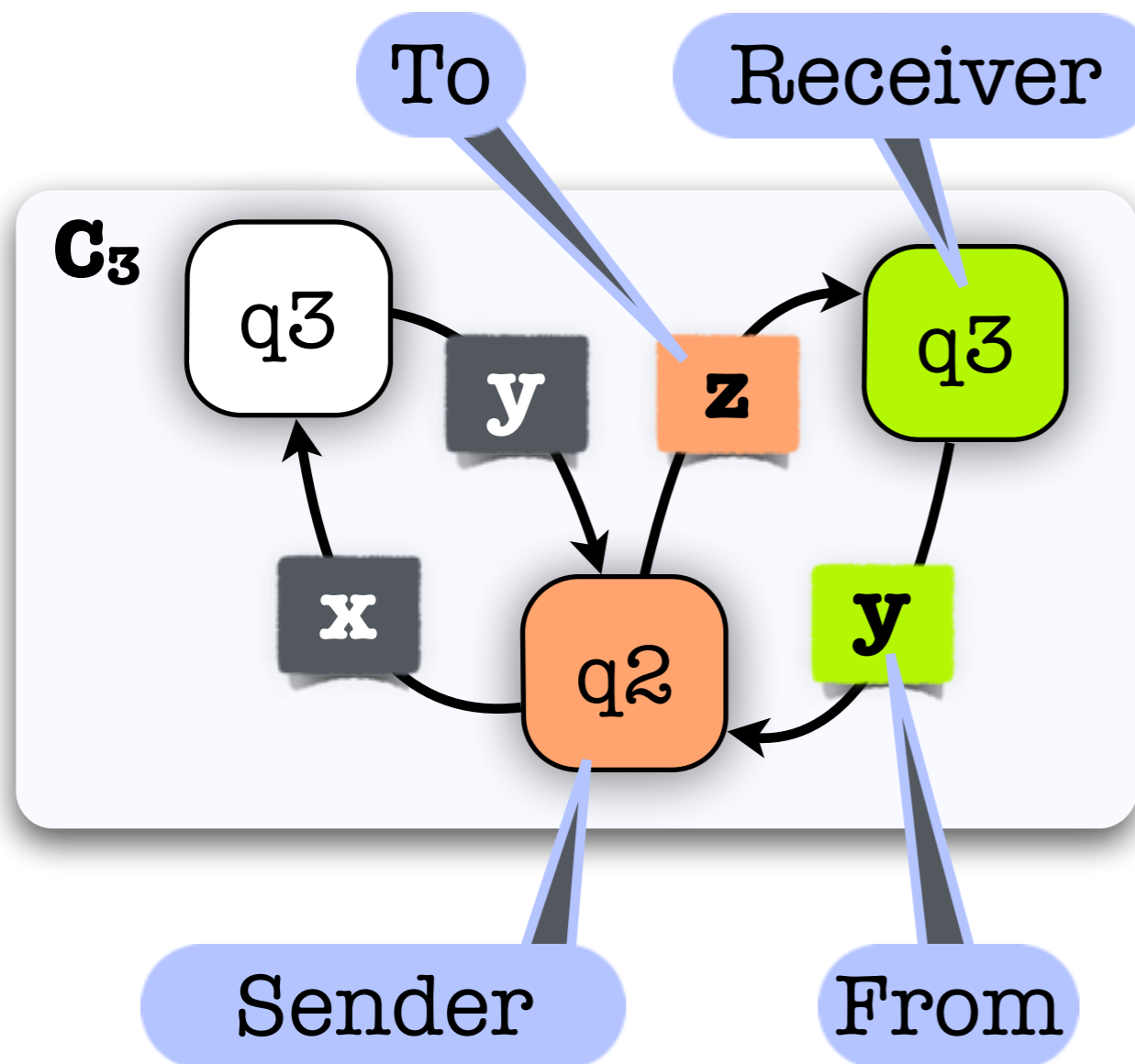
Verification of Dynamic Register Automata

Configuration

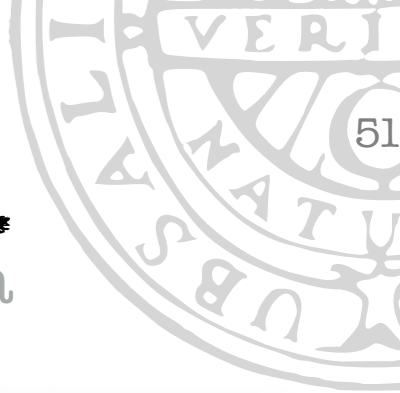
Transition Relation

Send & Receive ID

Process Model



Dynamic Register Automata



Formal Model

Verification of Dynamic Register Automata

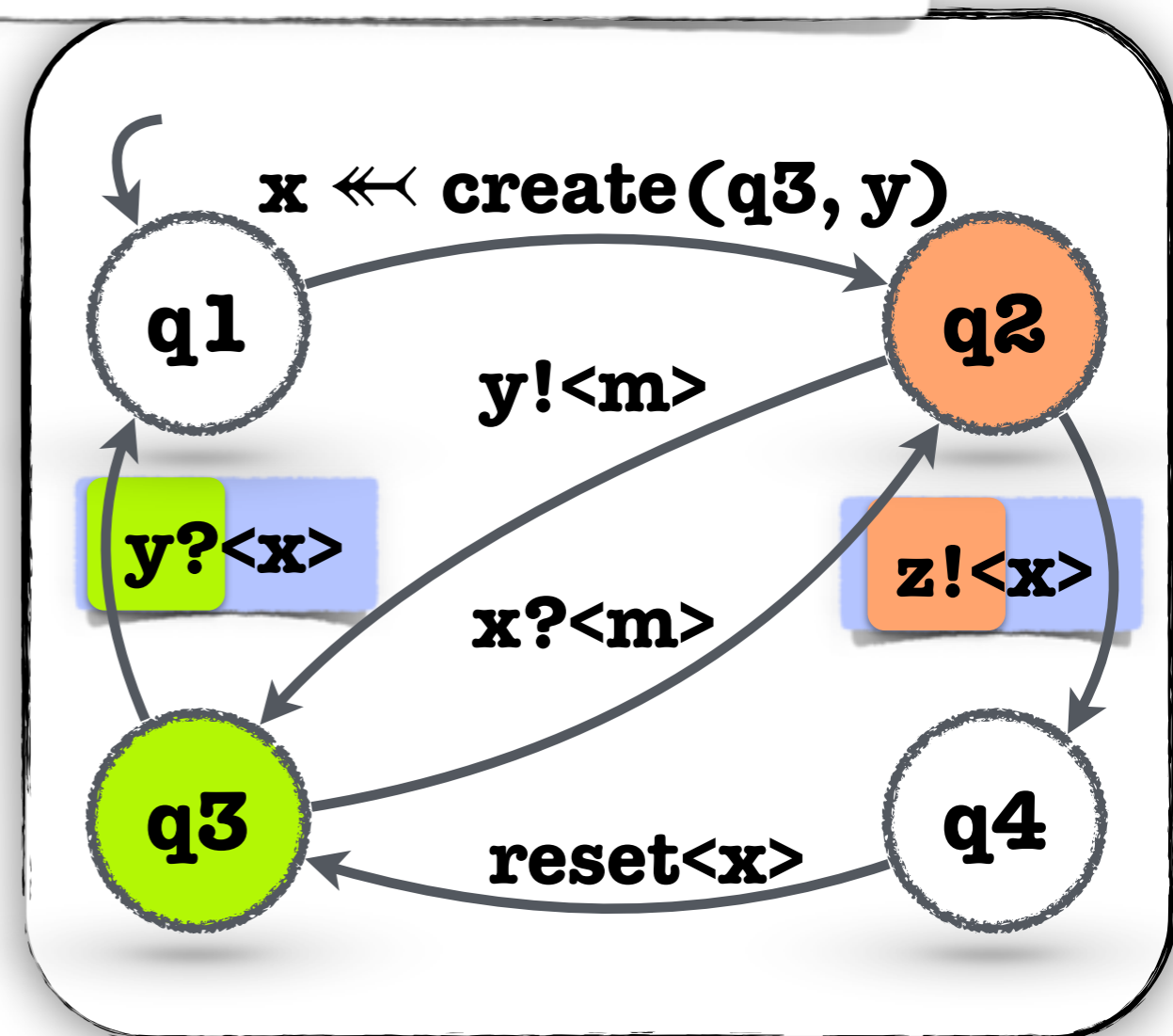
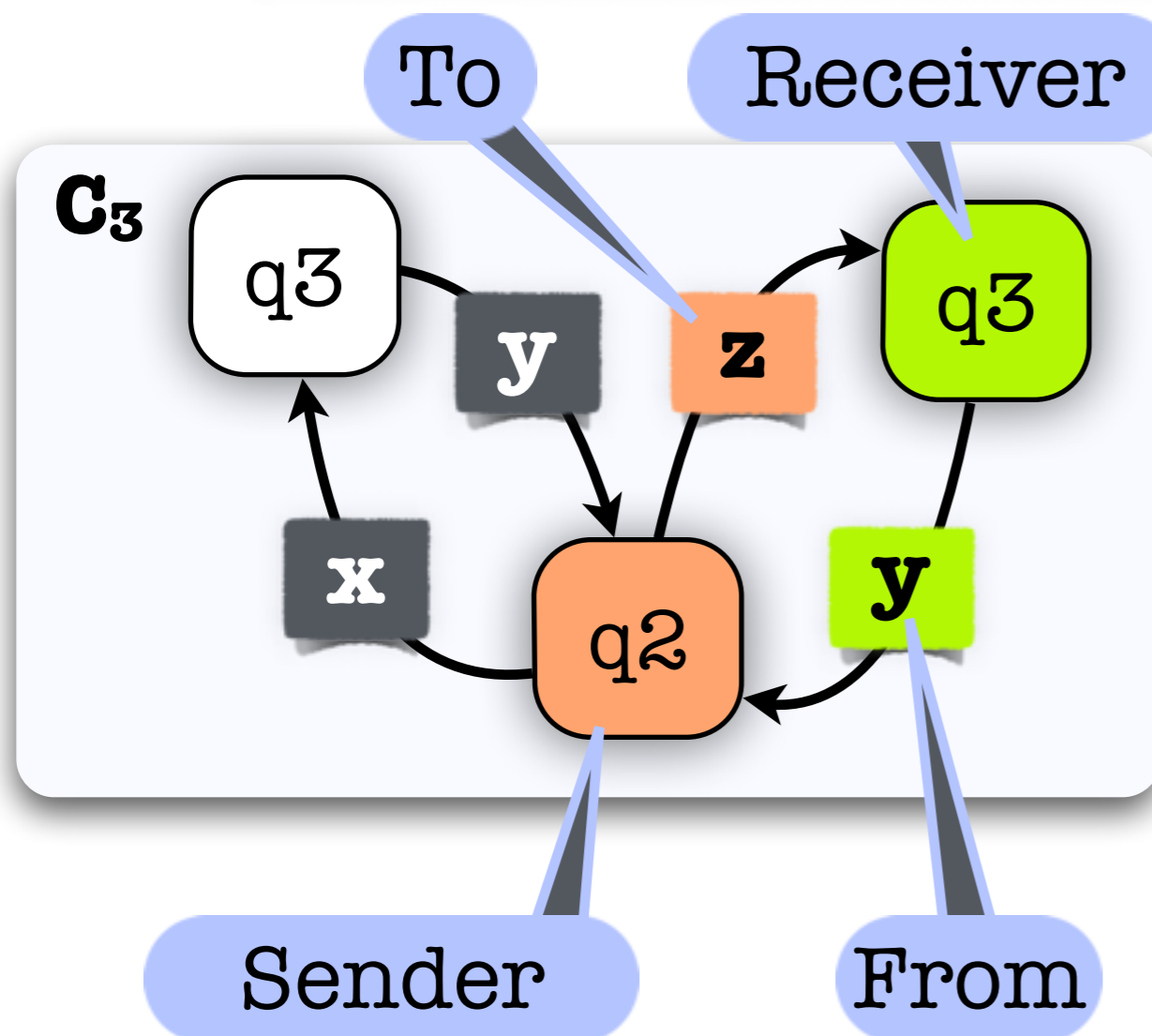
Configuration

Transition Relation

Process Model

Send & Receive ID

Point-To-Point, Rendez-Vous communication



Dynamic Register Automata



Verification of Dynamic Register Automata

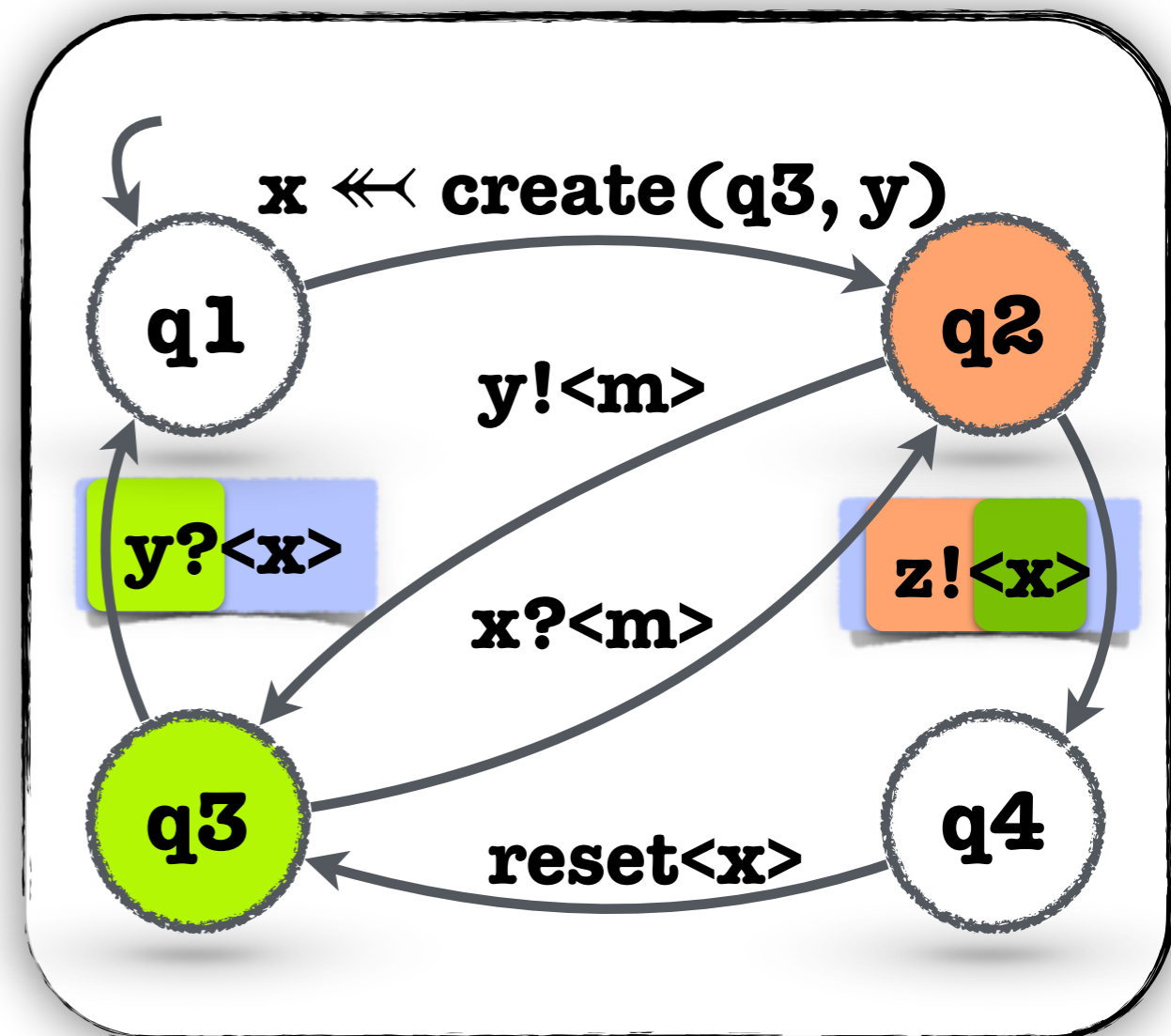
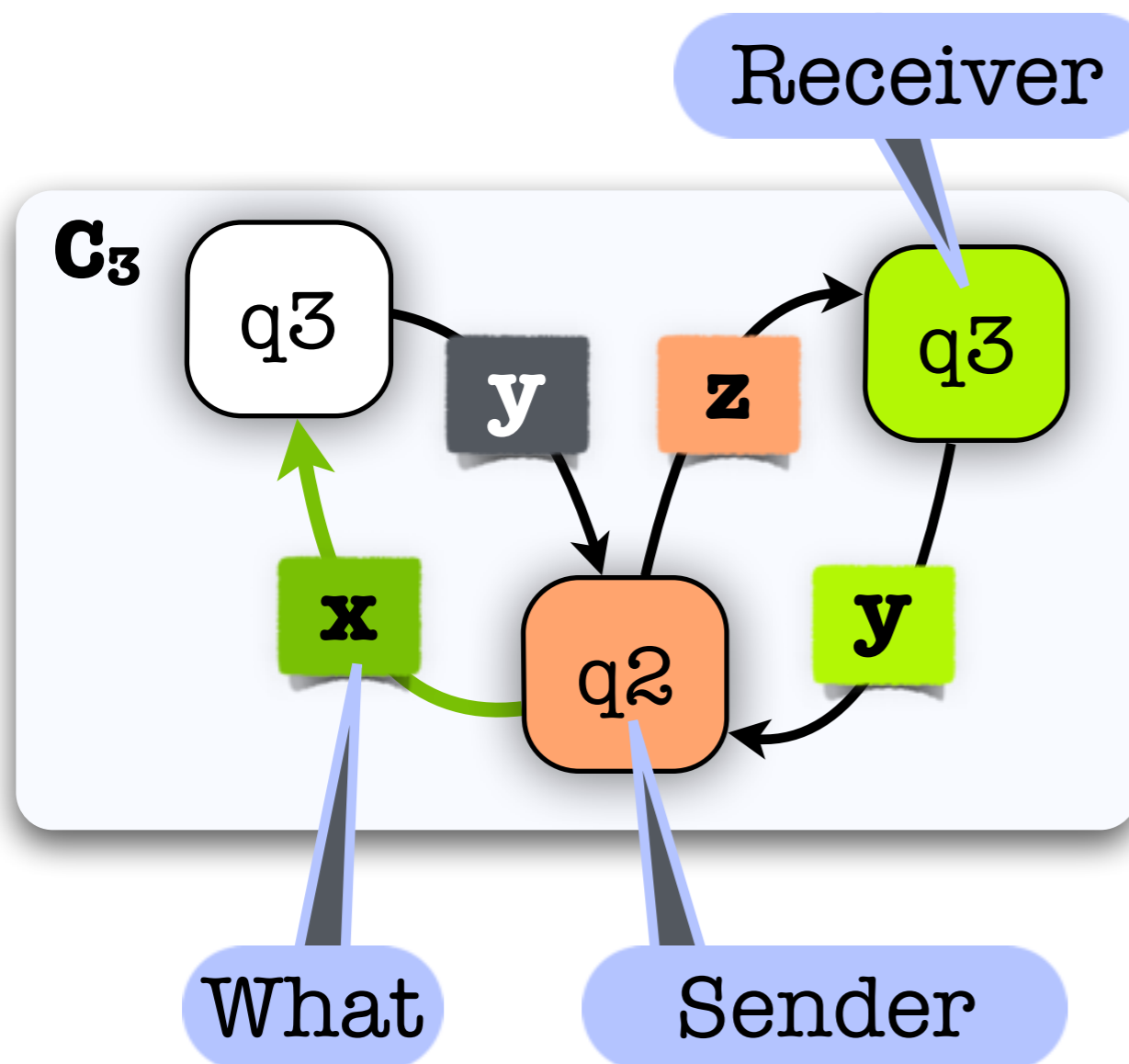
Formal Model

Configuration

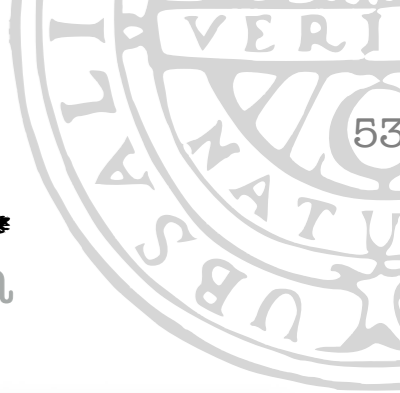
Transition Relation

Send & Receive ID

Process Model



Dynamic Register Automata



Verification of Dynamic Register Automata

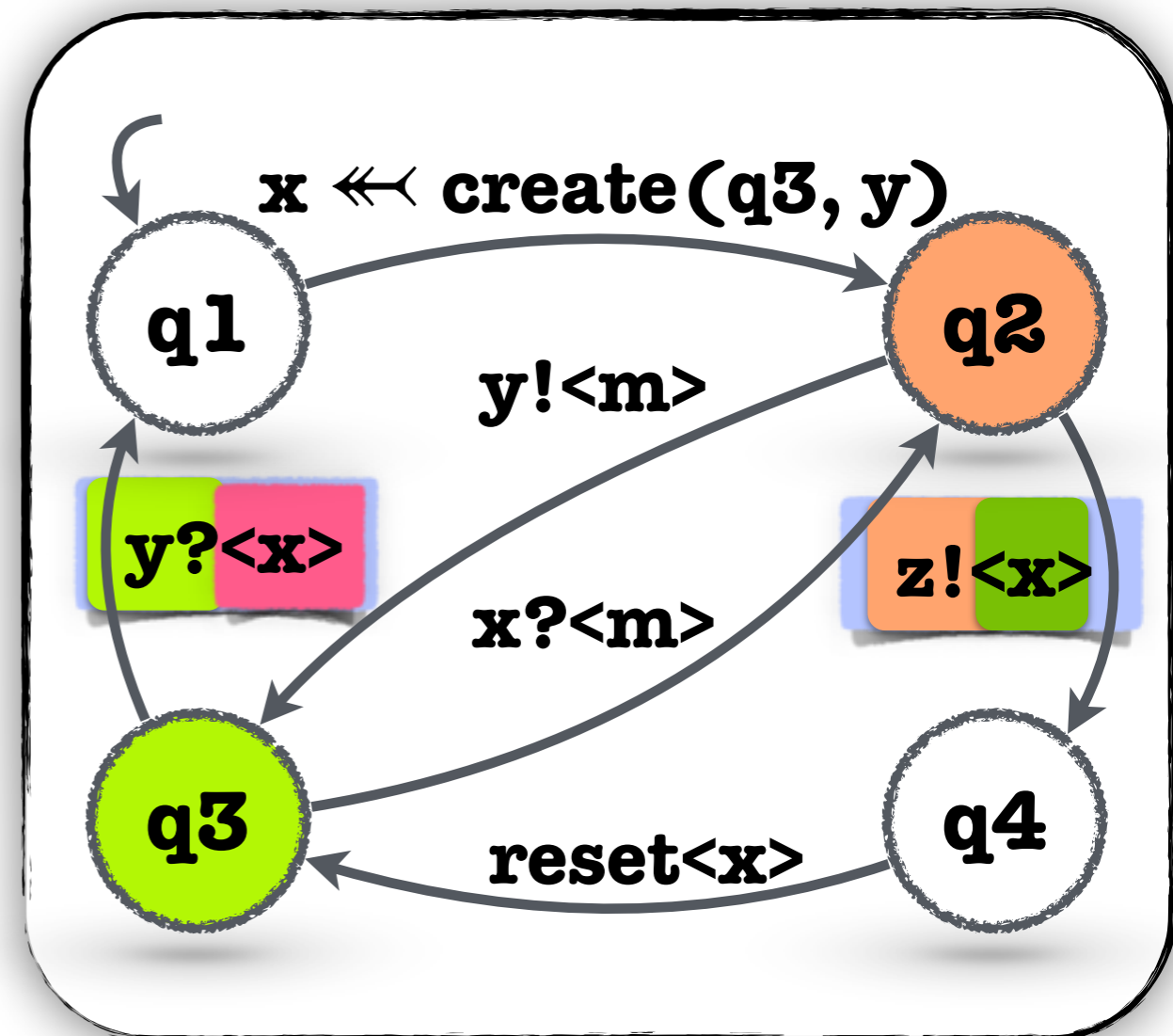
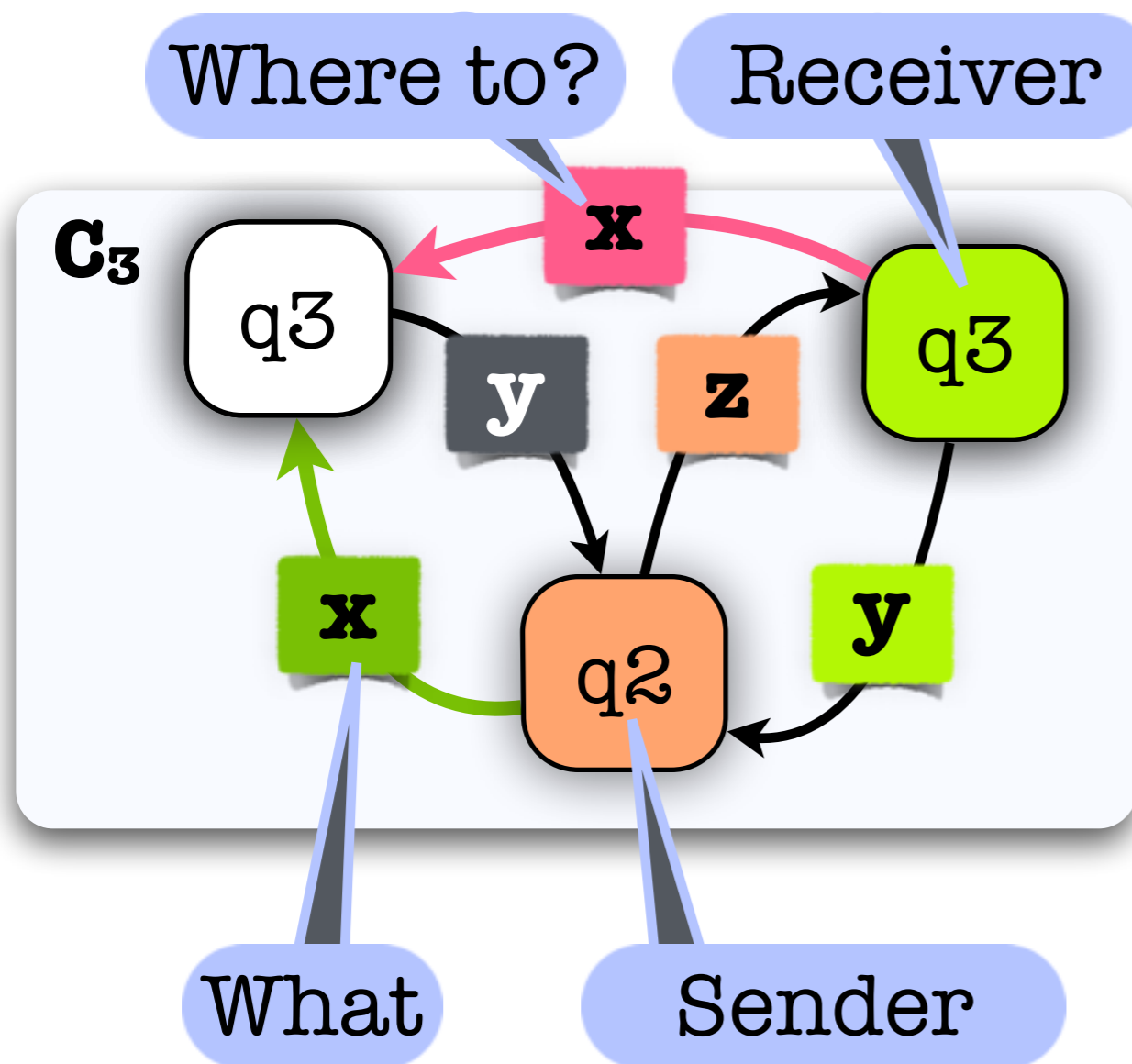
Formal Model

Configuration

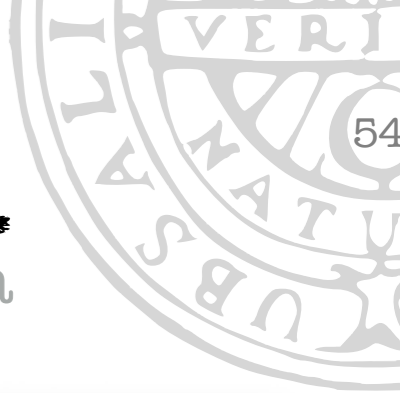
Transition Relation

Send & Receive ID

Process Model



Dynamic Register Automata



Verification of Dynamic Register Automata

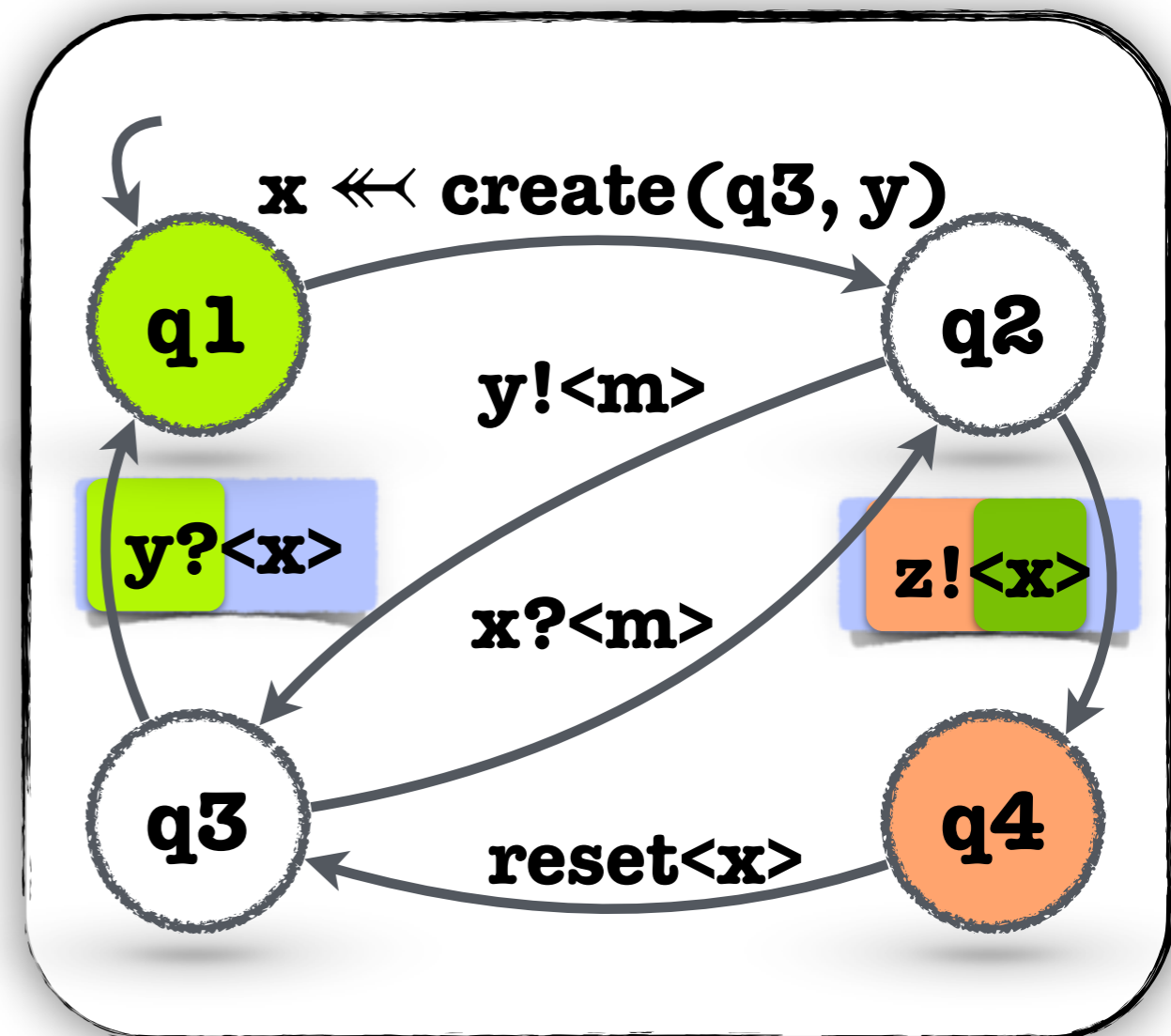
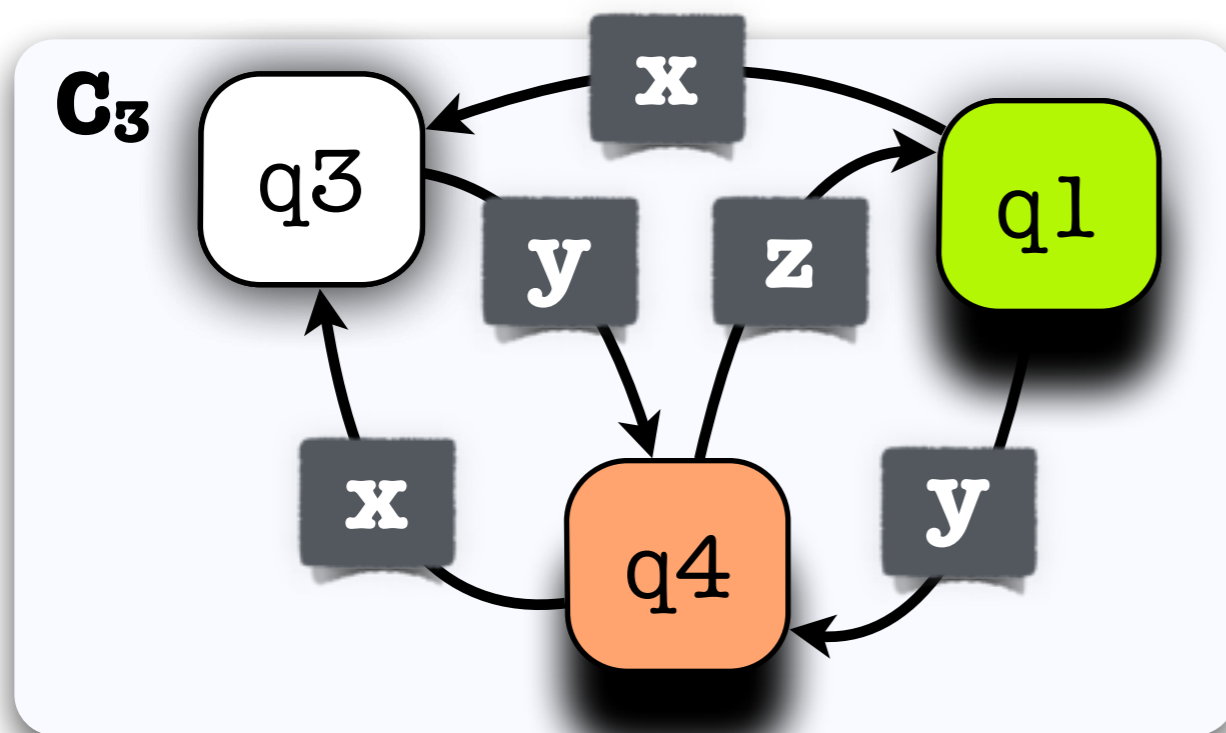
Formal Model

Configuration

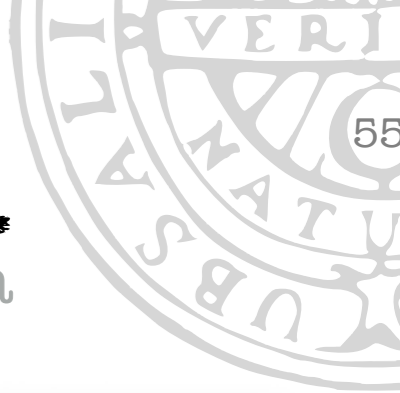
Transition Relation

Send & Receive ID

Process Model



Dynamic Register Automata



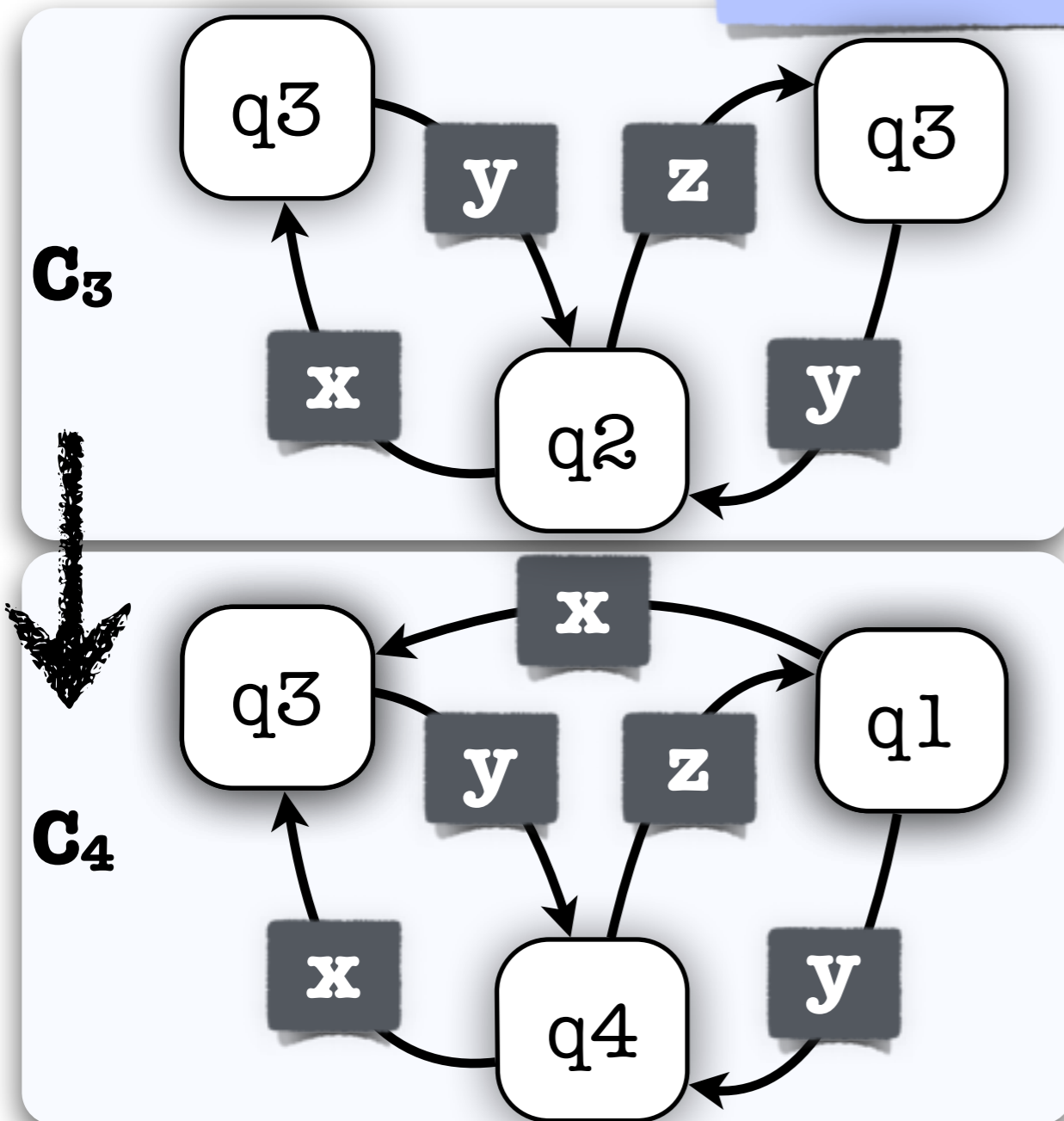
Verification of Dynamic Register Automata

Formal Model

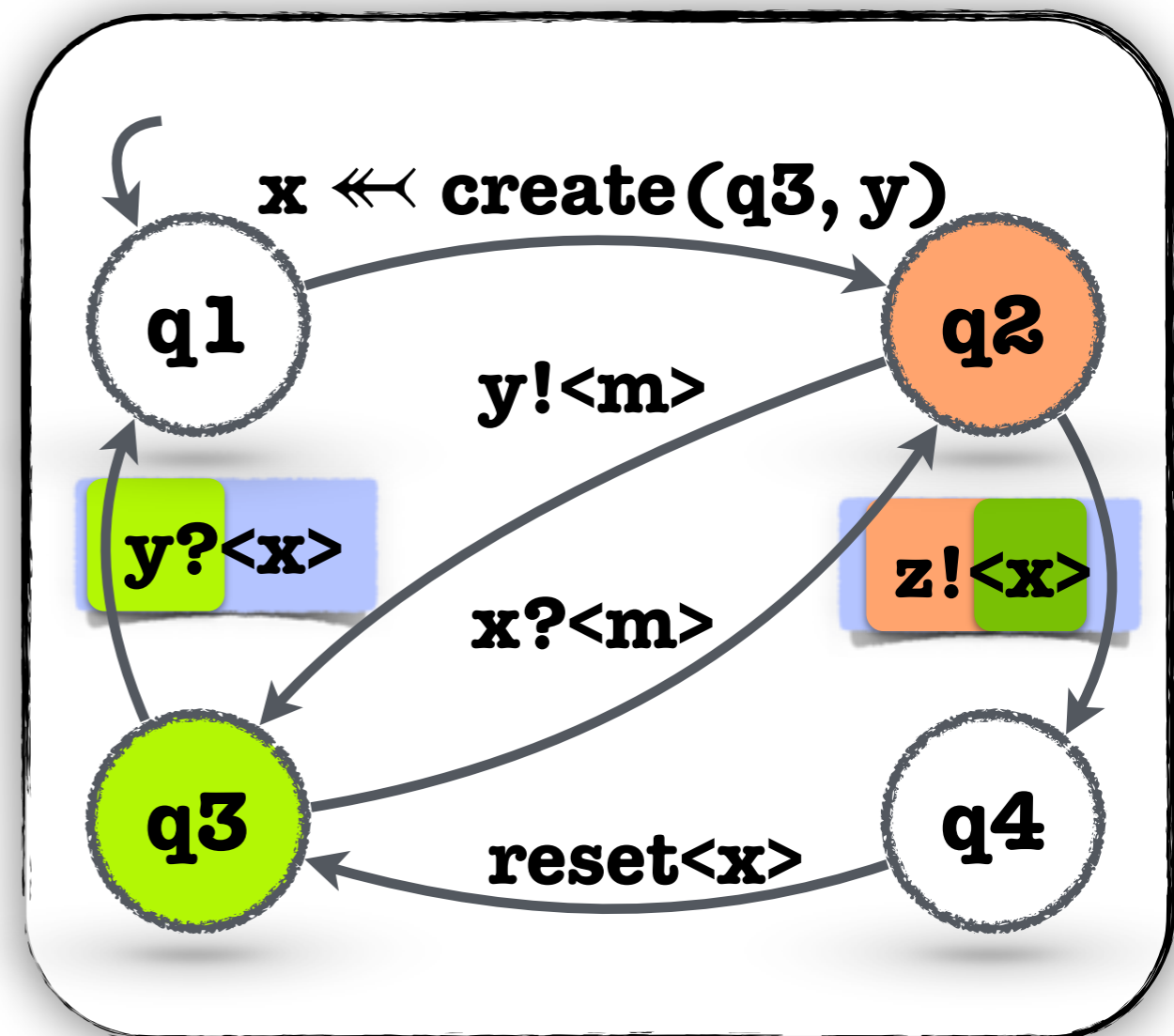
Configuration

Transition Relation

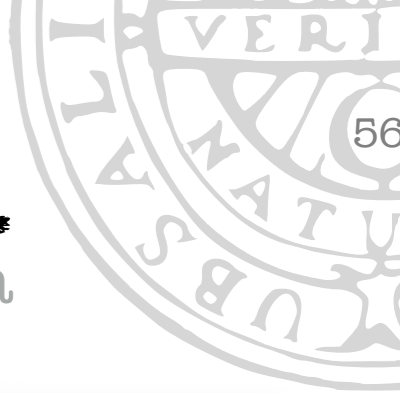
Send & Receive ID



Process Model



Dynamic Register Automata



Verification of Dynamic Register Automata

Formal Model

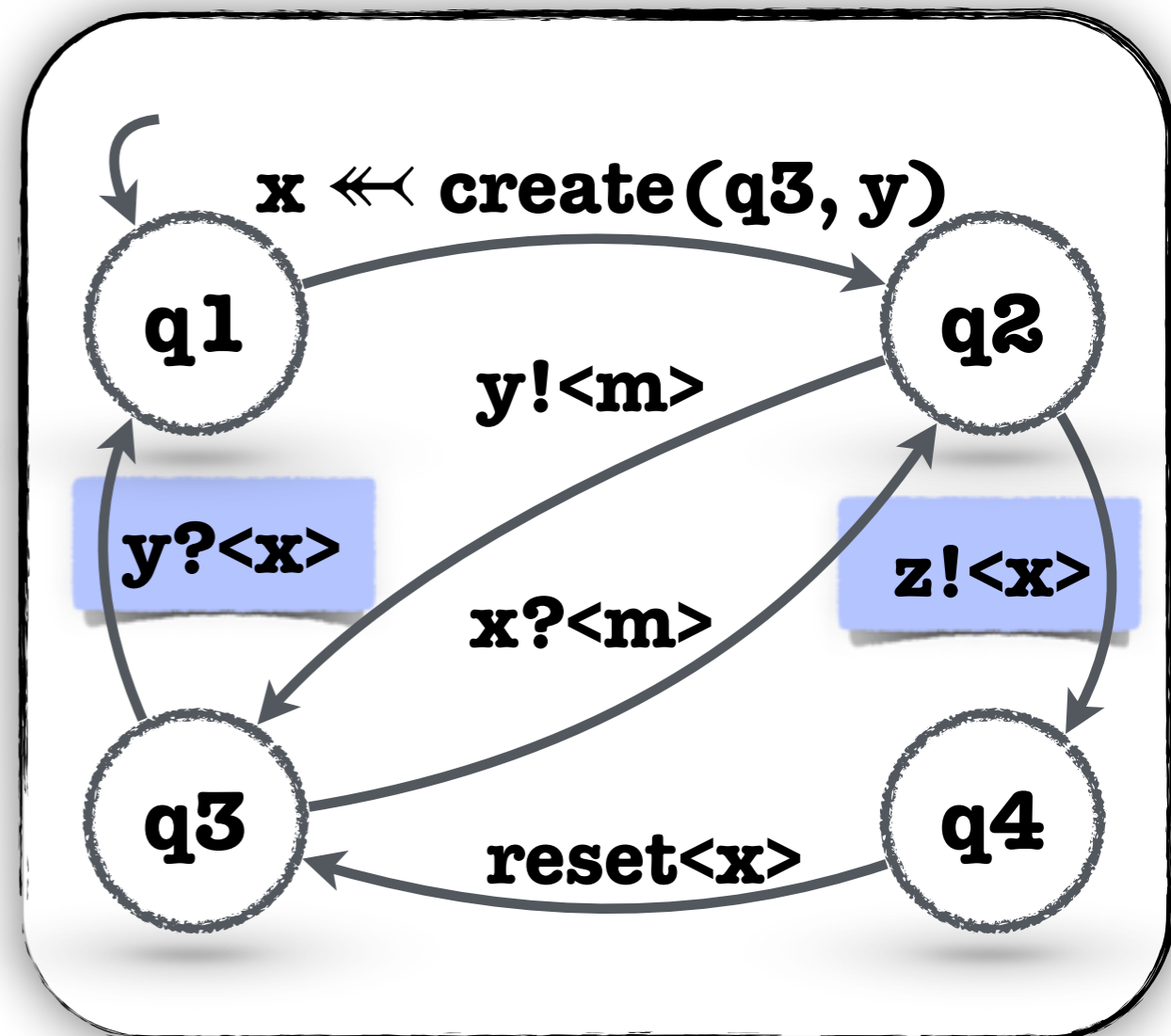
Configuration

Transition Relation

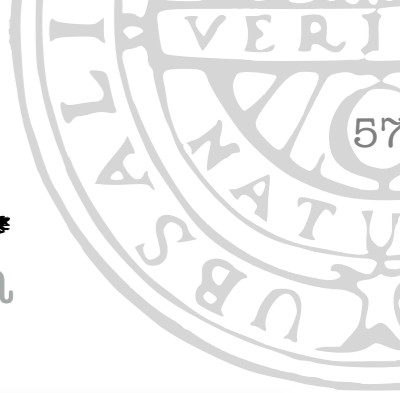
Process Creation

Send & Receive ID

Process Model



Dynamic Register Automata



Verification of Dynamic Register Automata

Formal Model

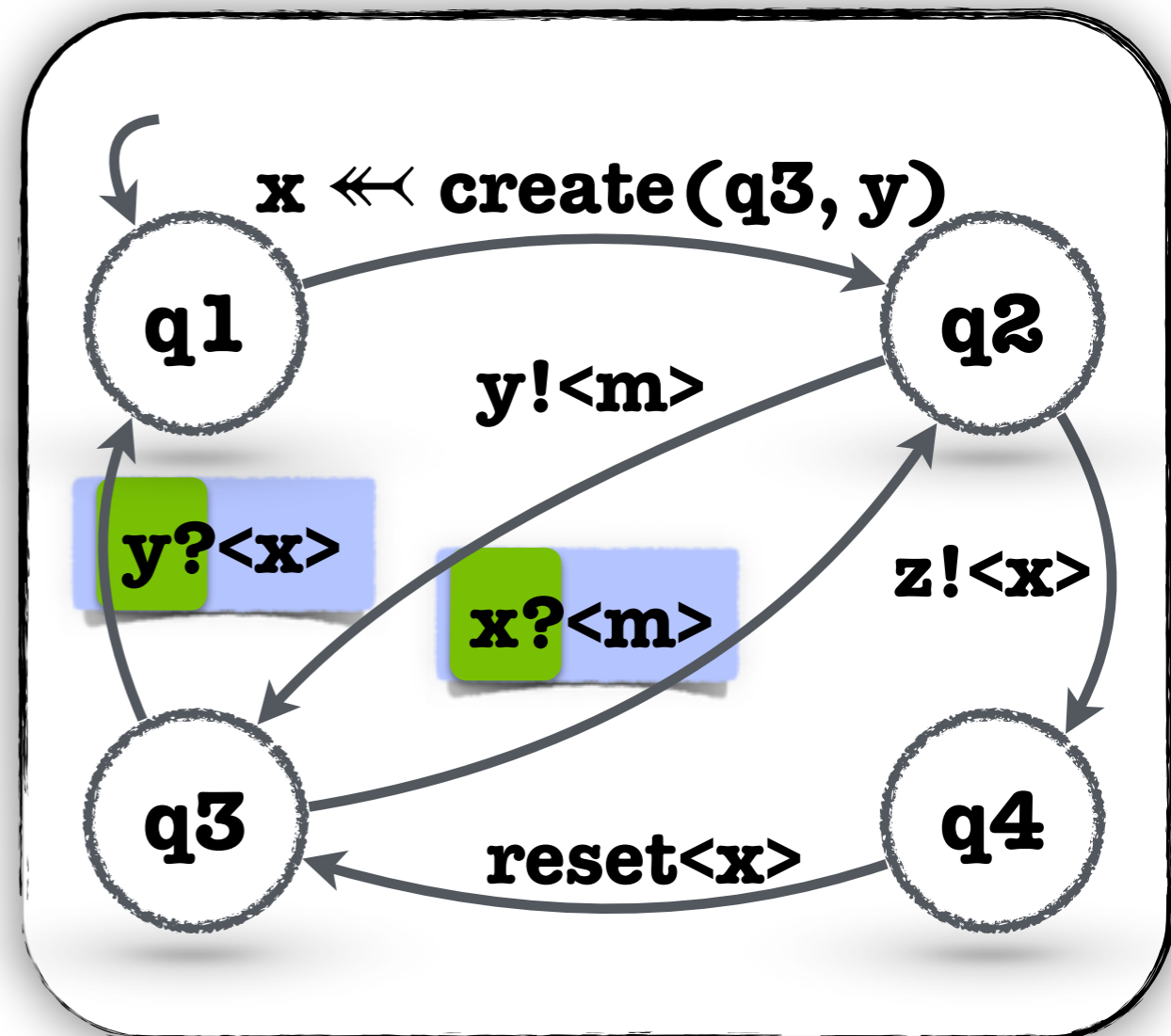
Configuration

Transition Relation

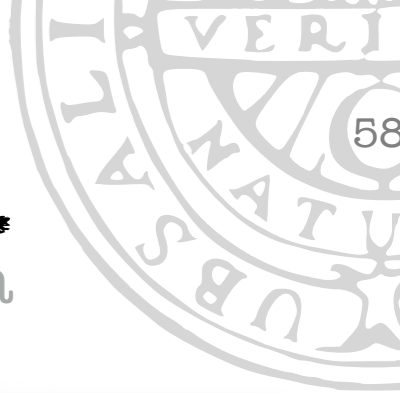
Process Creation

Send & Receive ID

Process Model



Dynamic Register Automata



Verification of Dynamic Register Automata

Formal Model

Configuration

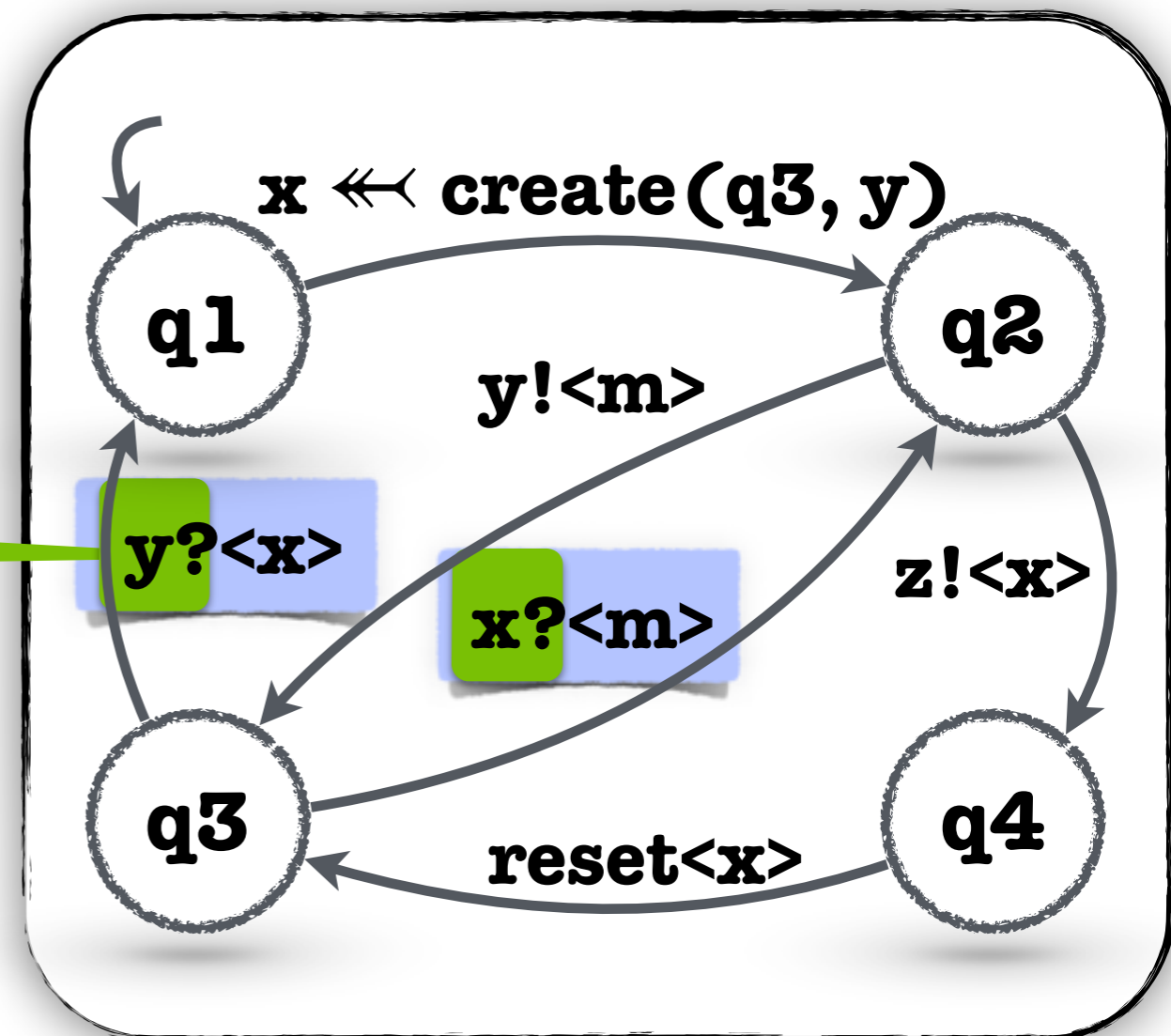
Process Model

Transition Relation

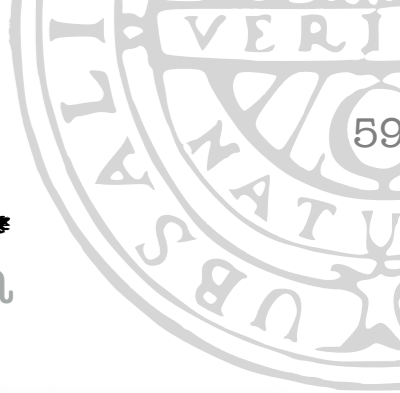
Process Creation

Send & Receive ID

Selective Receive



Dynamic Register Automata



Verification of Dynamic Register Automata

Formal Model

Configuration

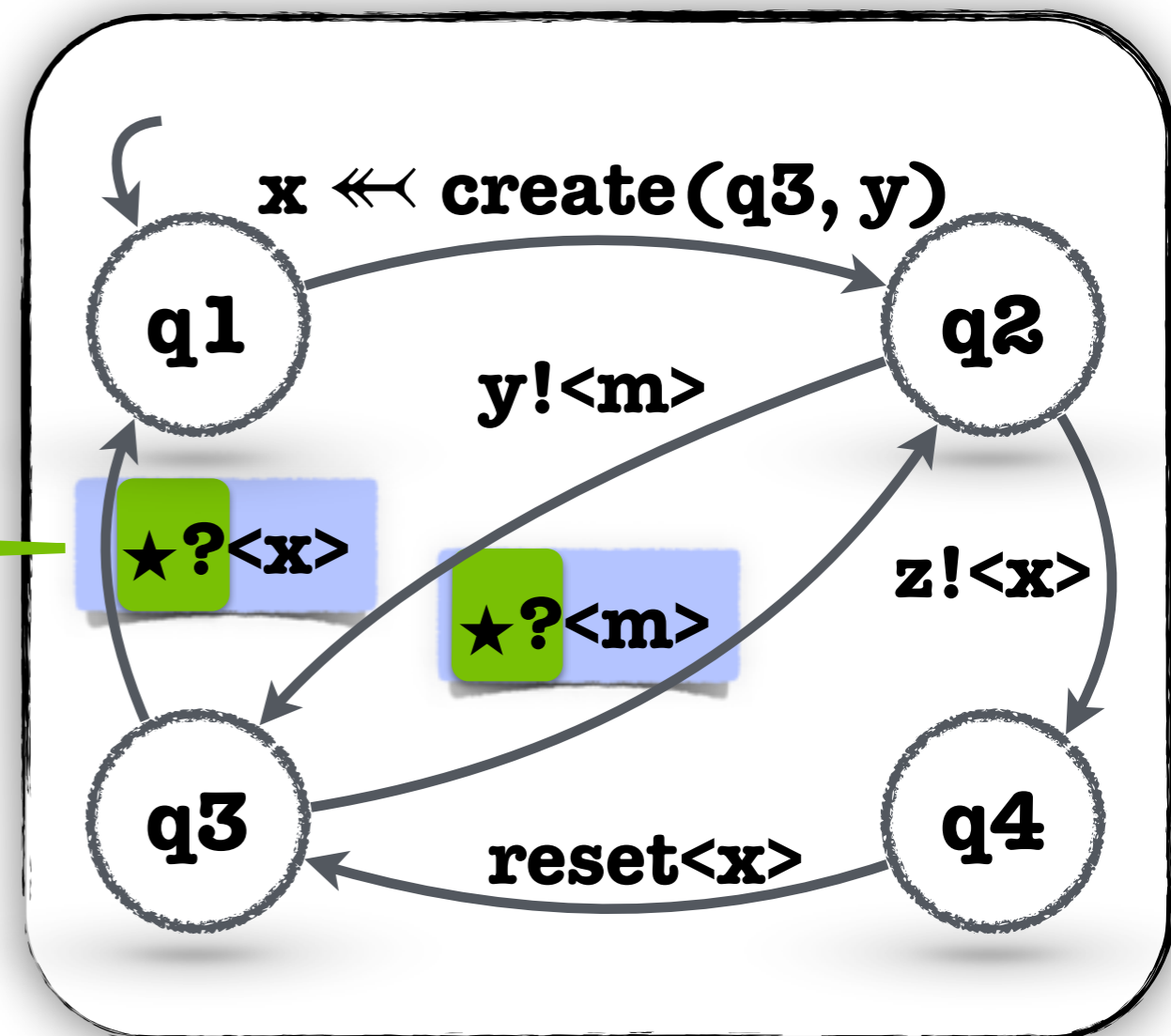
Transition Relation

Process Creation

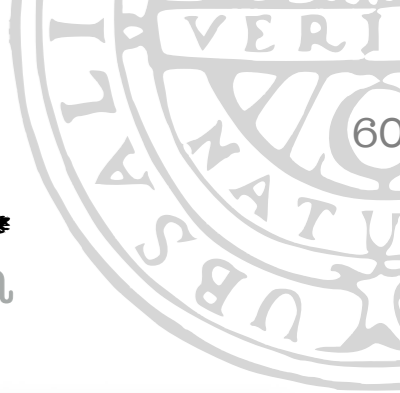
Send & Receive ID

Non Selective Receive

Process Model



Dynamic Register Automata



Verification of Dynamic Register Automata

Formal Model

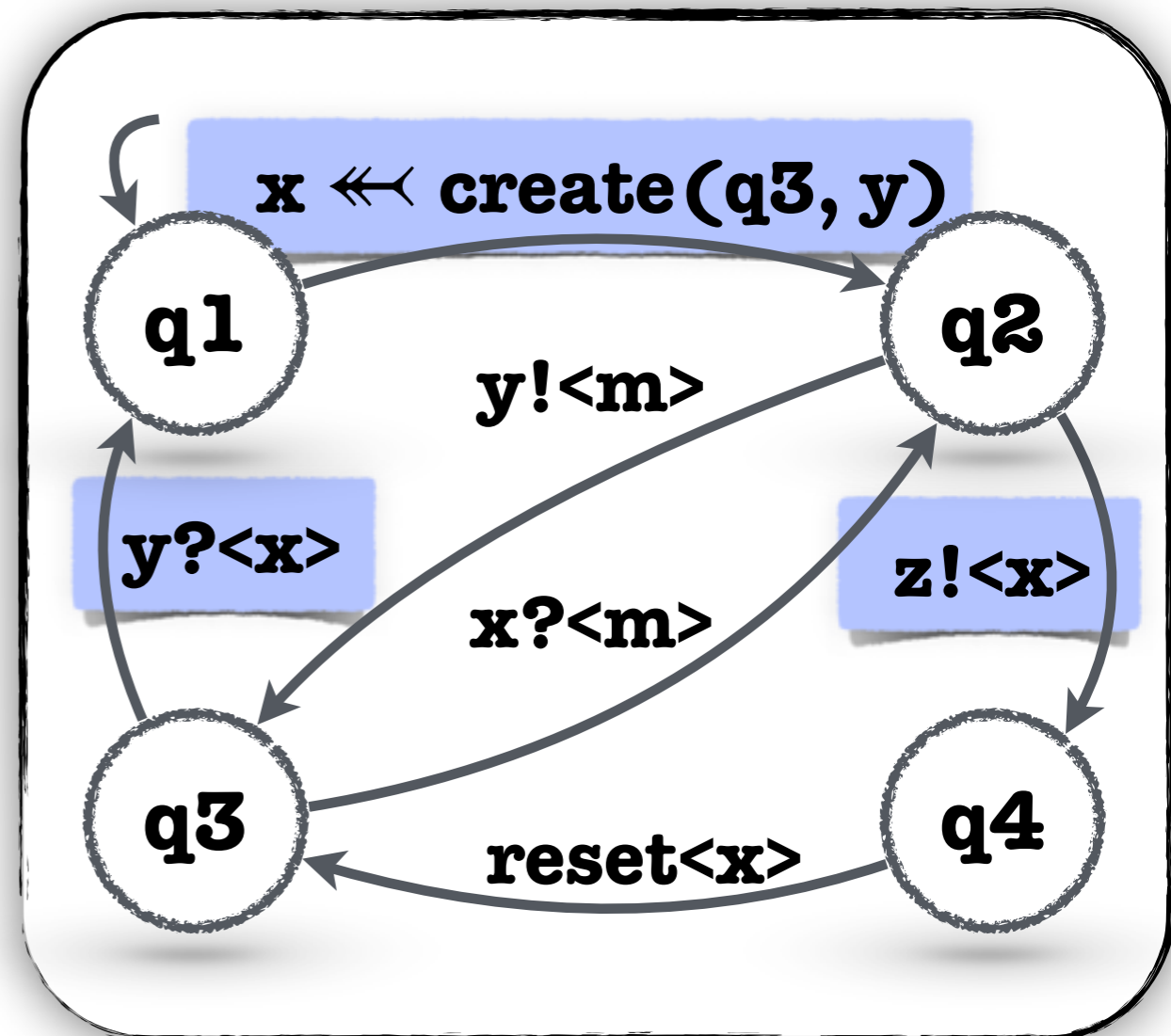
Configuration

Transition Relation

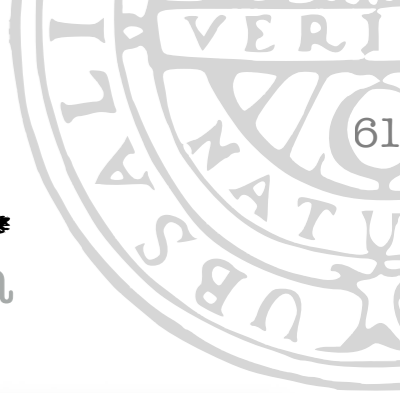
Process Creation

Send & Receive ID

Process Model



Dynamic Register Automata



Verification of Dynamic Register Automata

Formal Model

Configuration

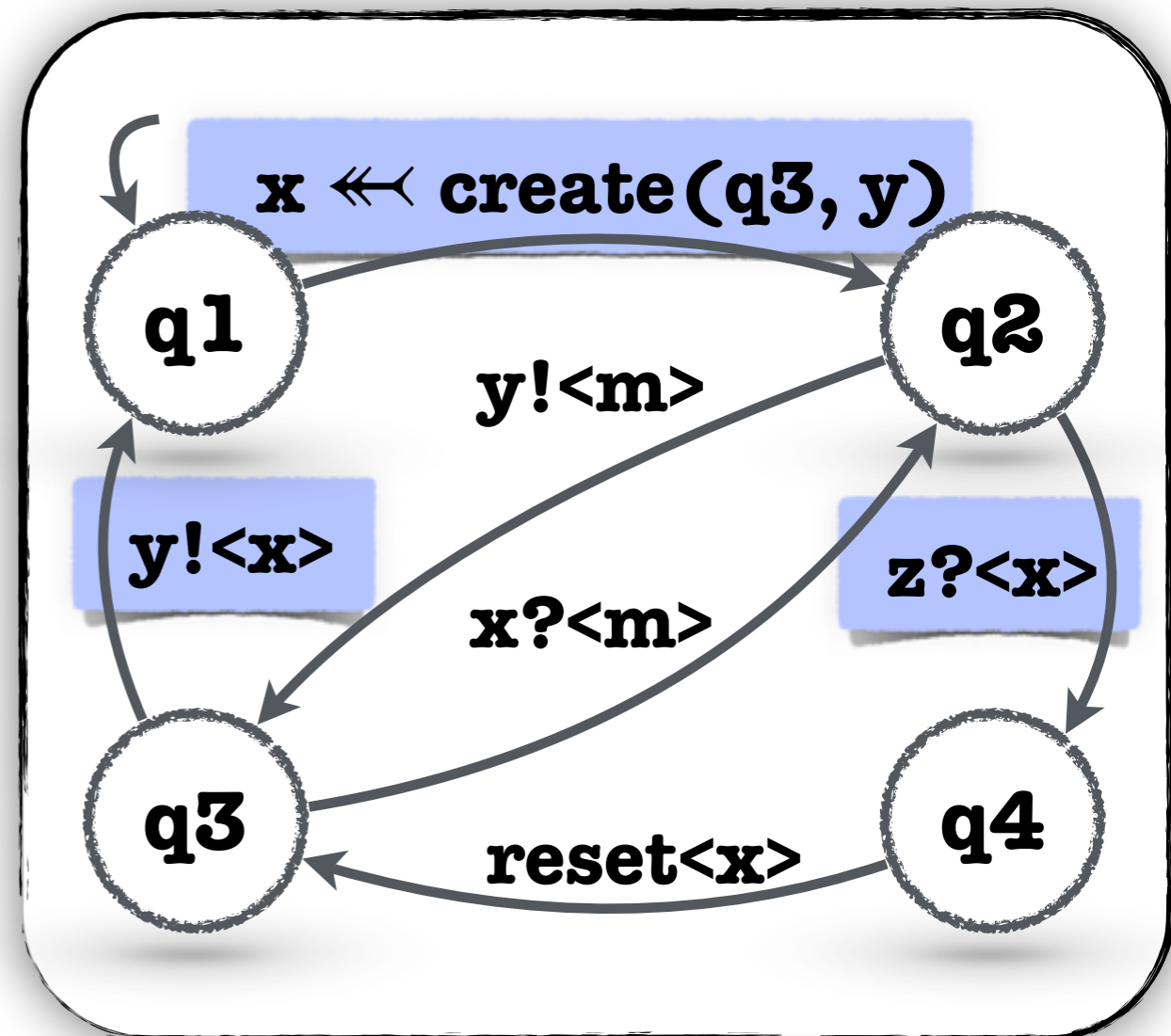
Transition Relation

Process Creation

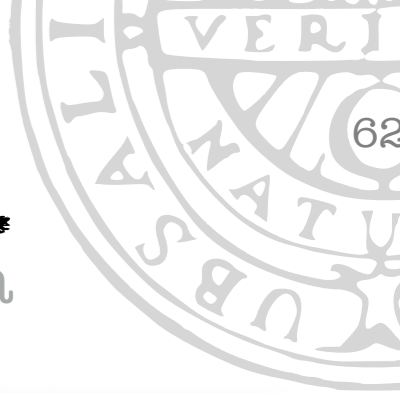
Send & Receive ID

Register Reset

Process Model



Dynamic Register Automata



Verification of Dynamic Register Automata

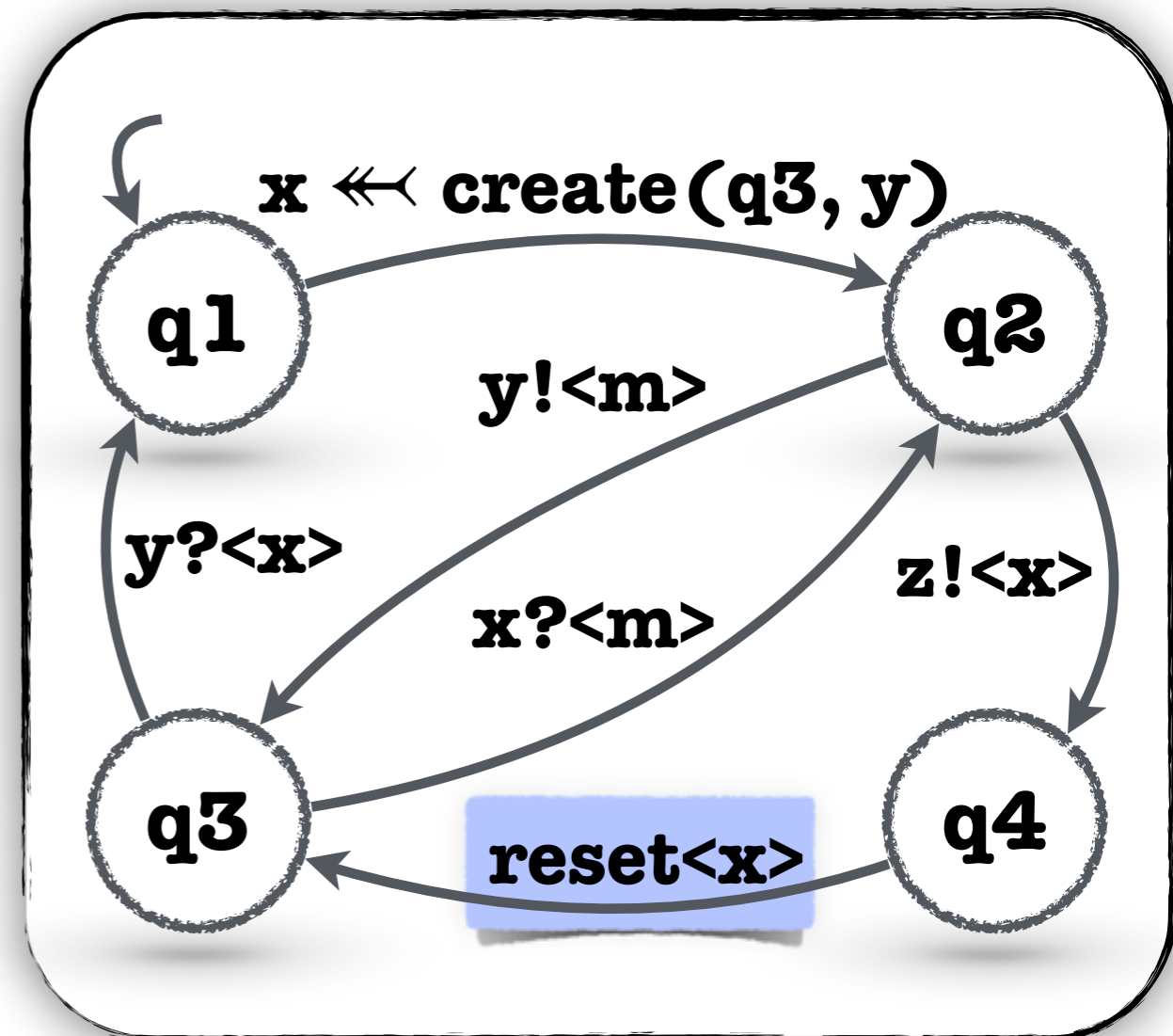
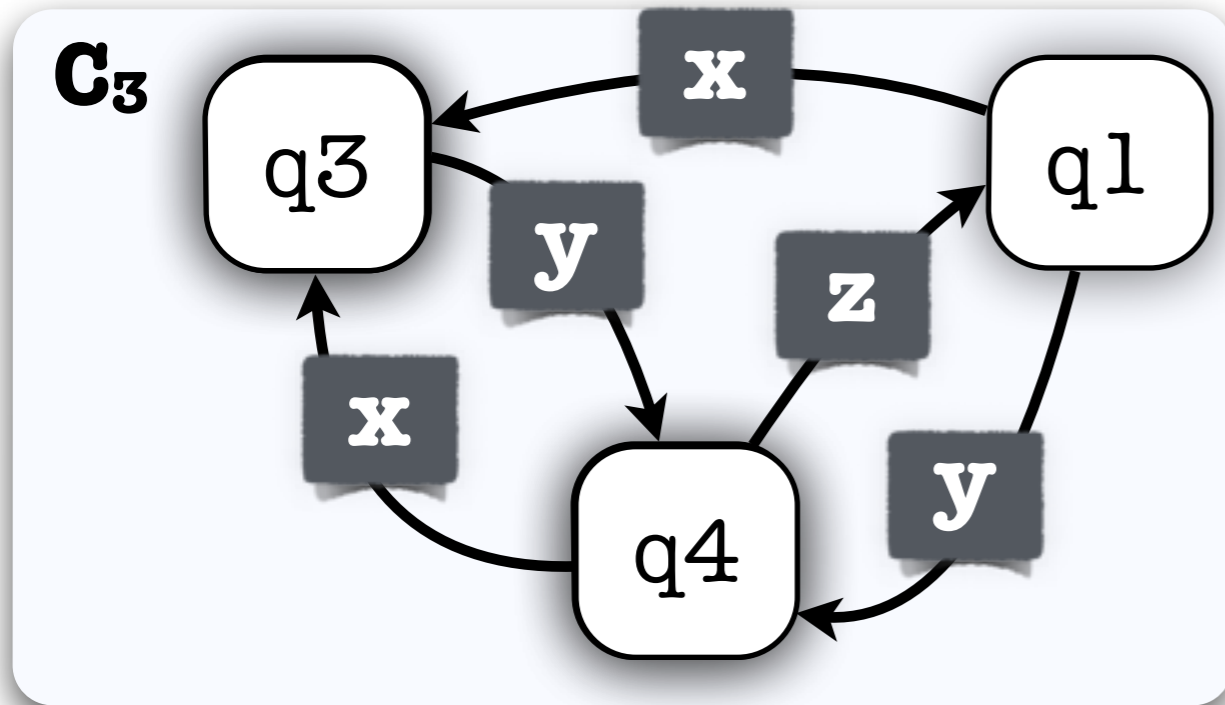
Formal Model

Configuration

Transition Relation

Register Reset

Process Model



Dynamic Register Automata



Verification of Dynamic Register Automata

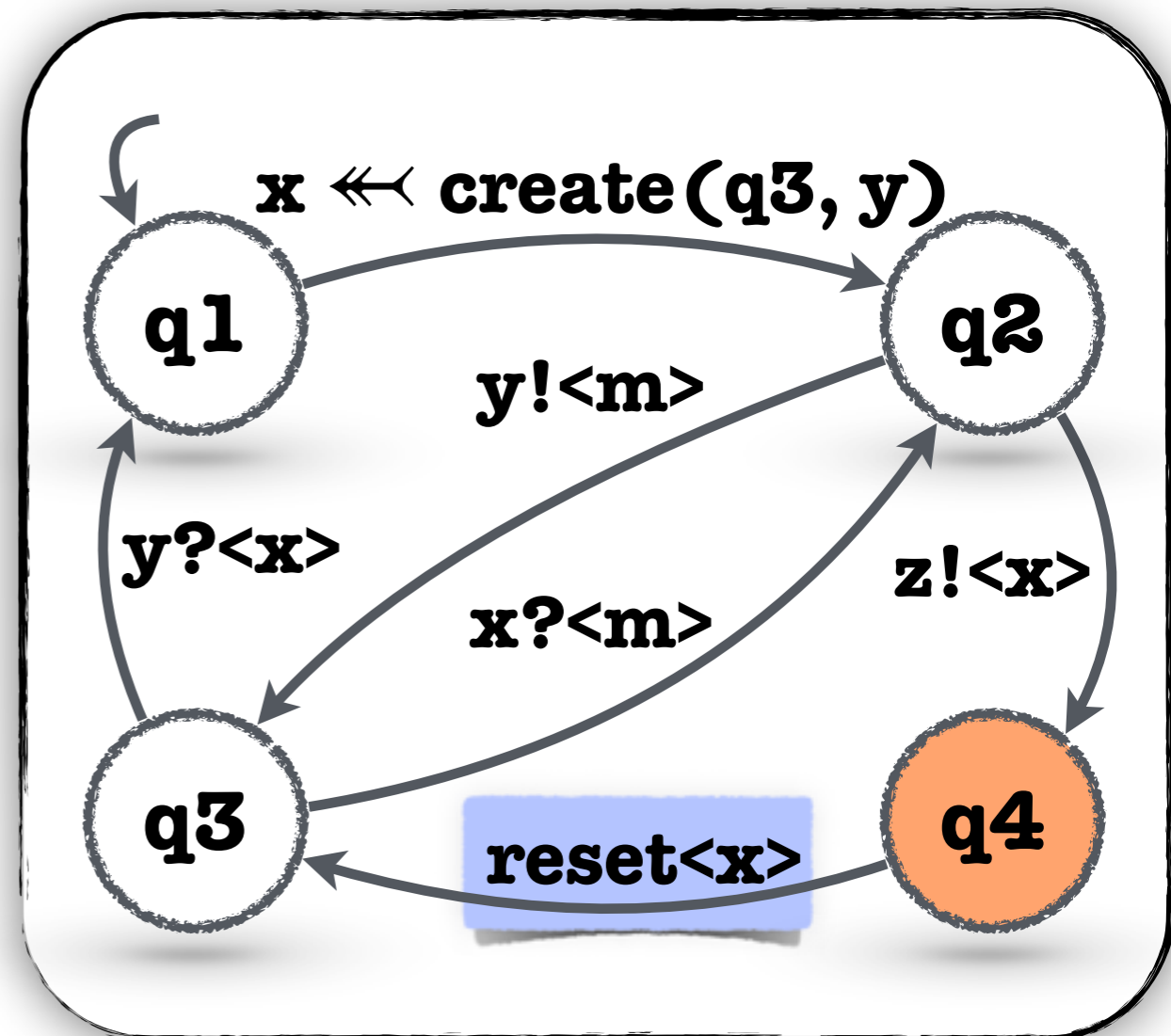
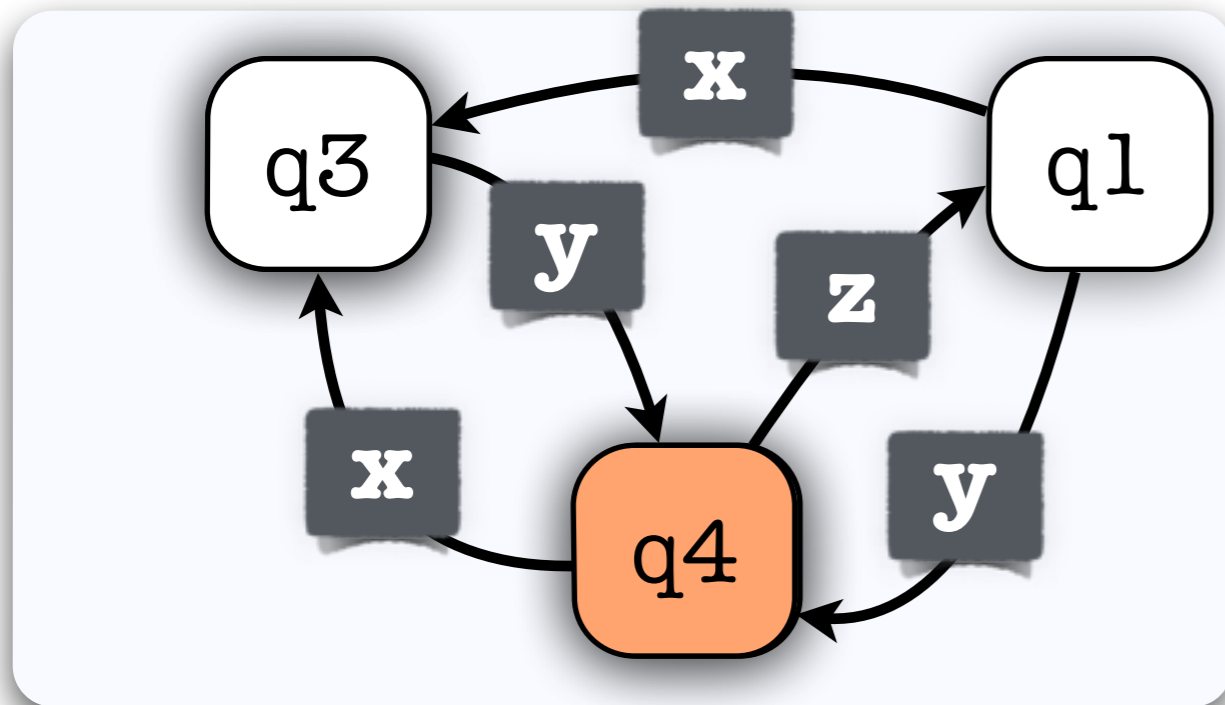
Formal Model

Configuration

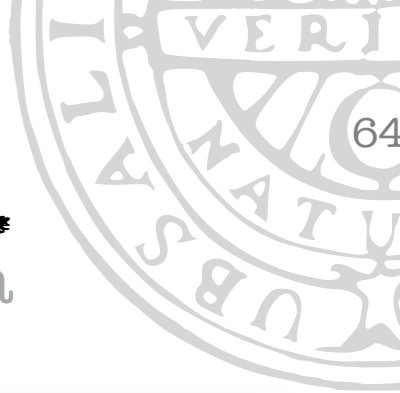
Transition Relation

Register Reset

Process Model



Dynamic Register Automata



Verification of Dynamic Register Automata

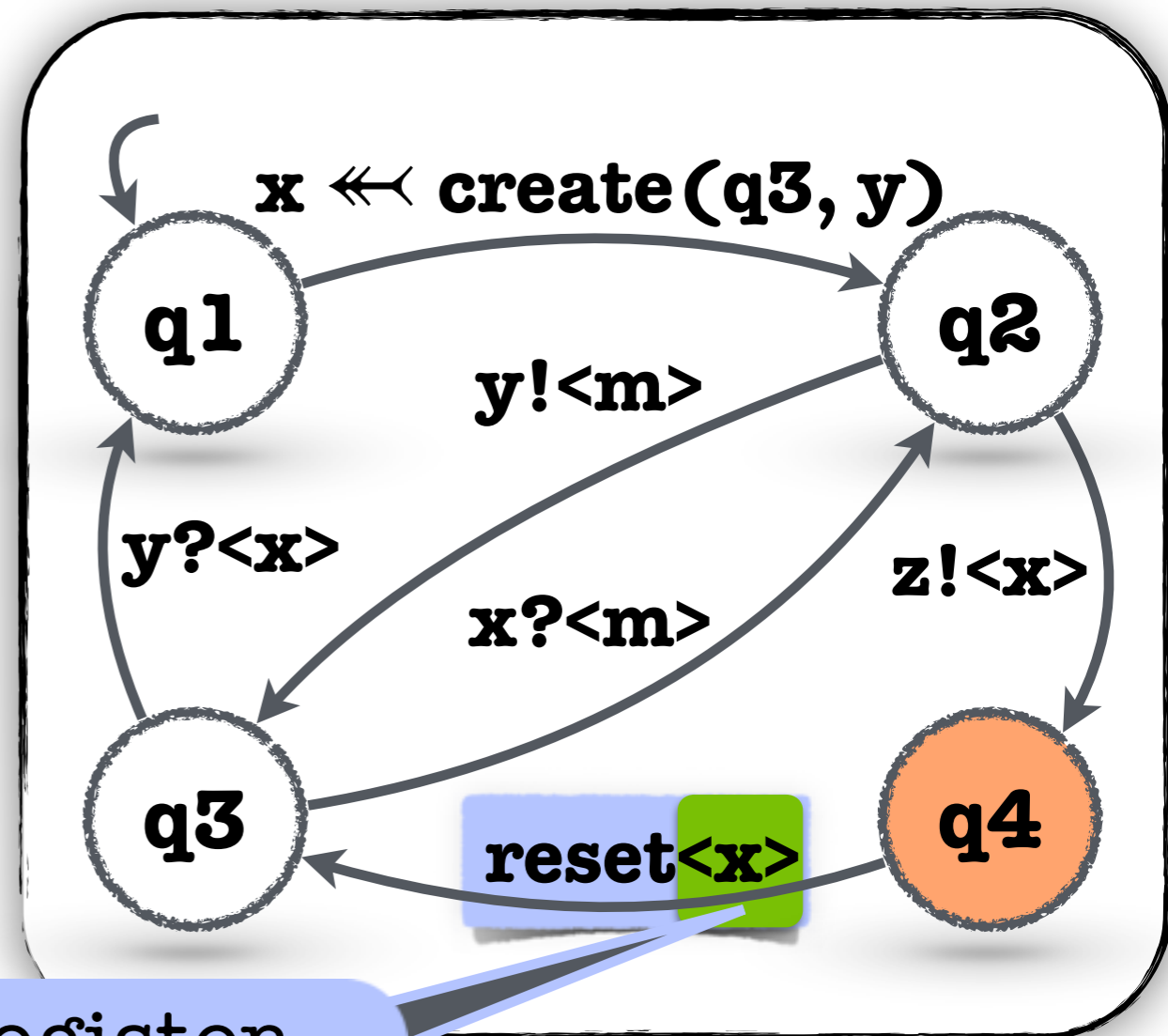
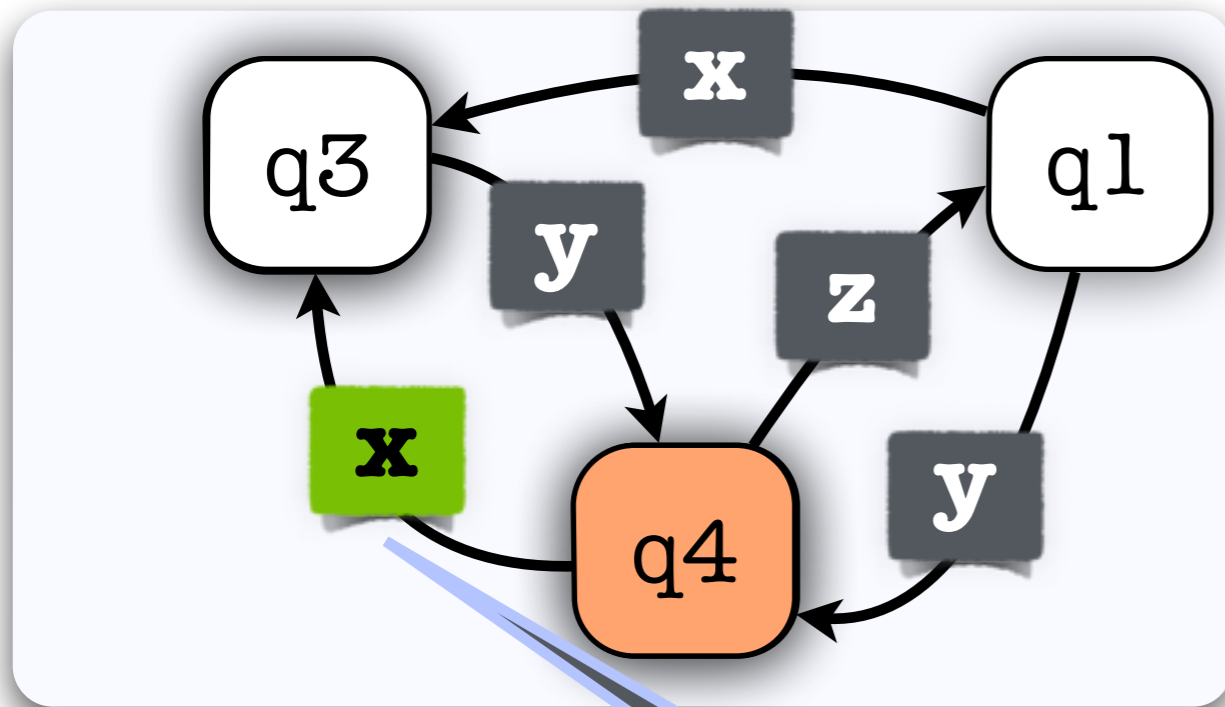
Formal Model

Configuration

Transition Relation

Register Reset

Process Model



Which register

Dynamic Register Automata



Verification of Dynamic Register Automata

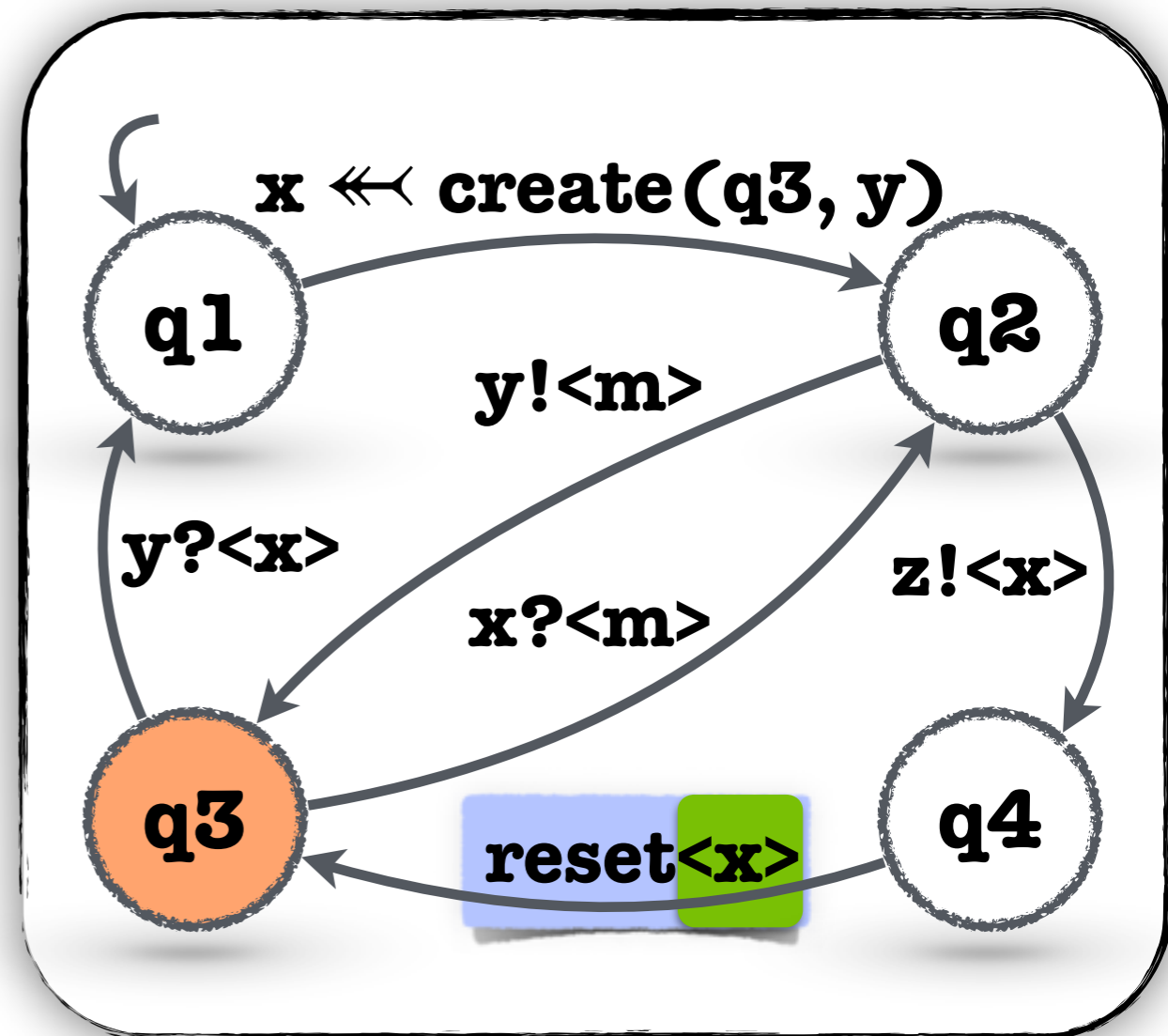
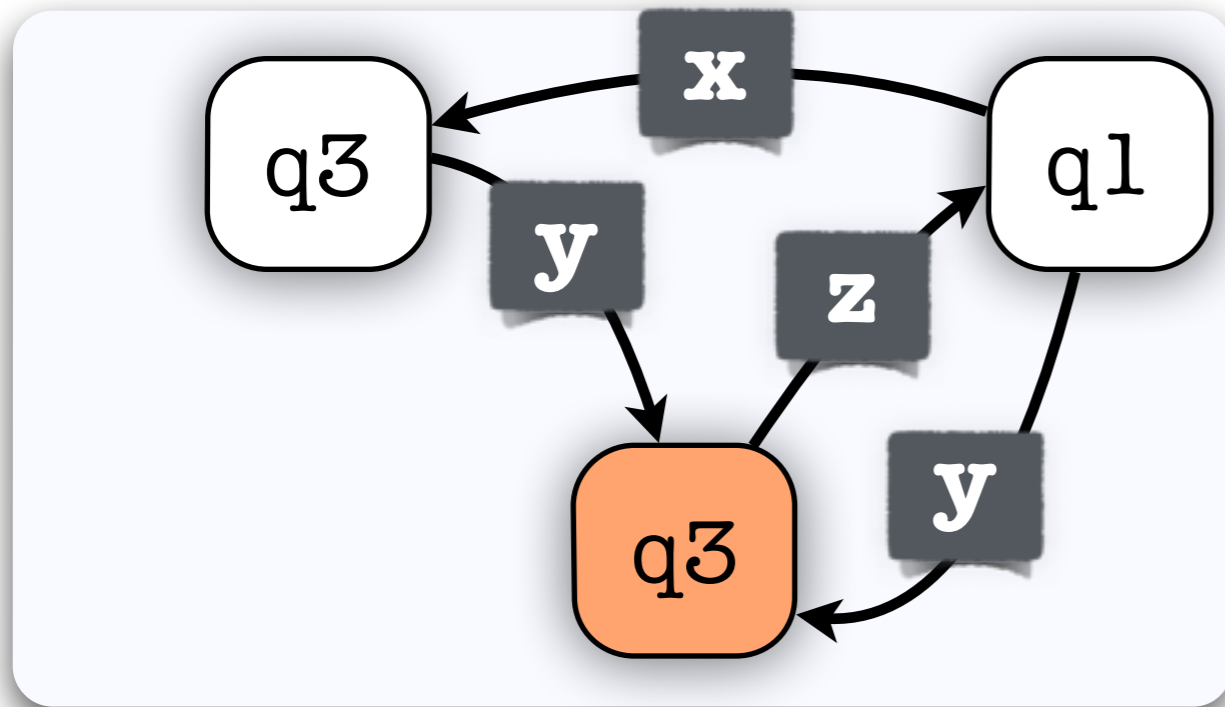
Formal Model

Configuration

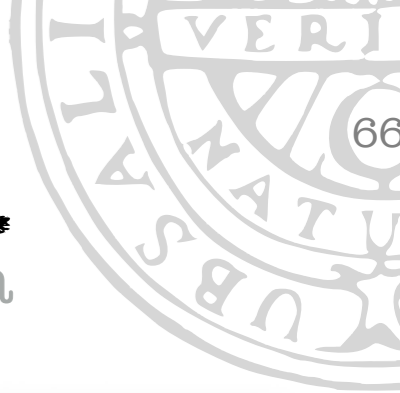
Transition Relation

Register Reset

Process Model



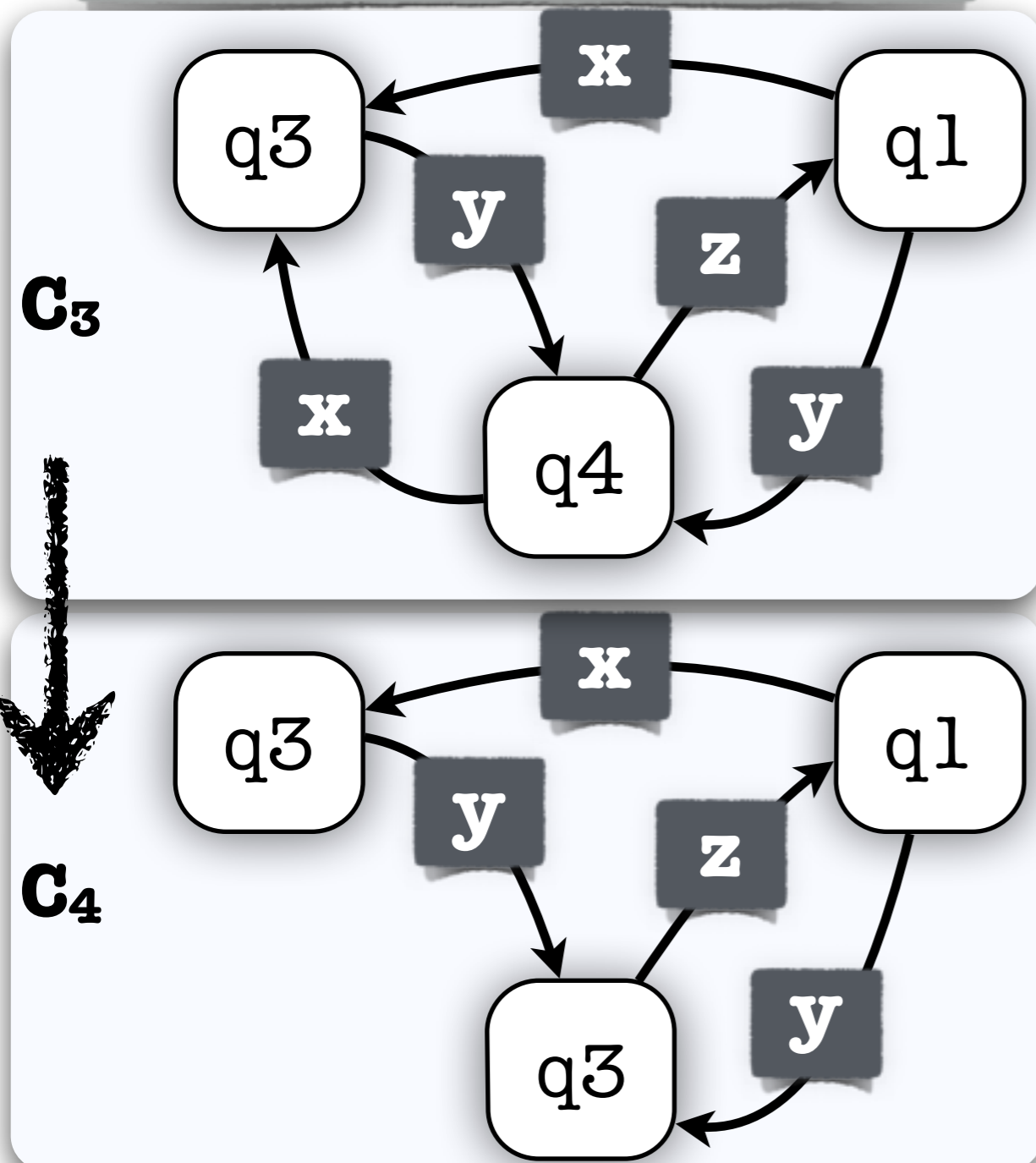
Dynamic Register Automata



Formal Model

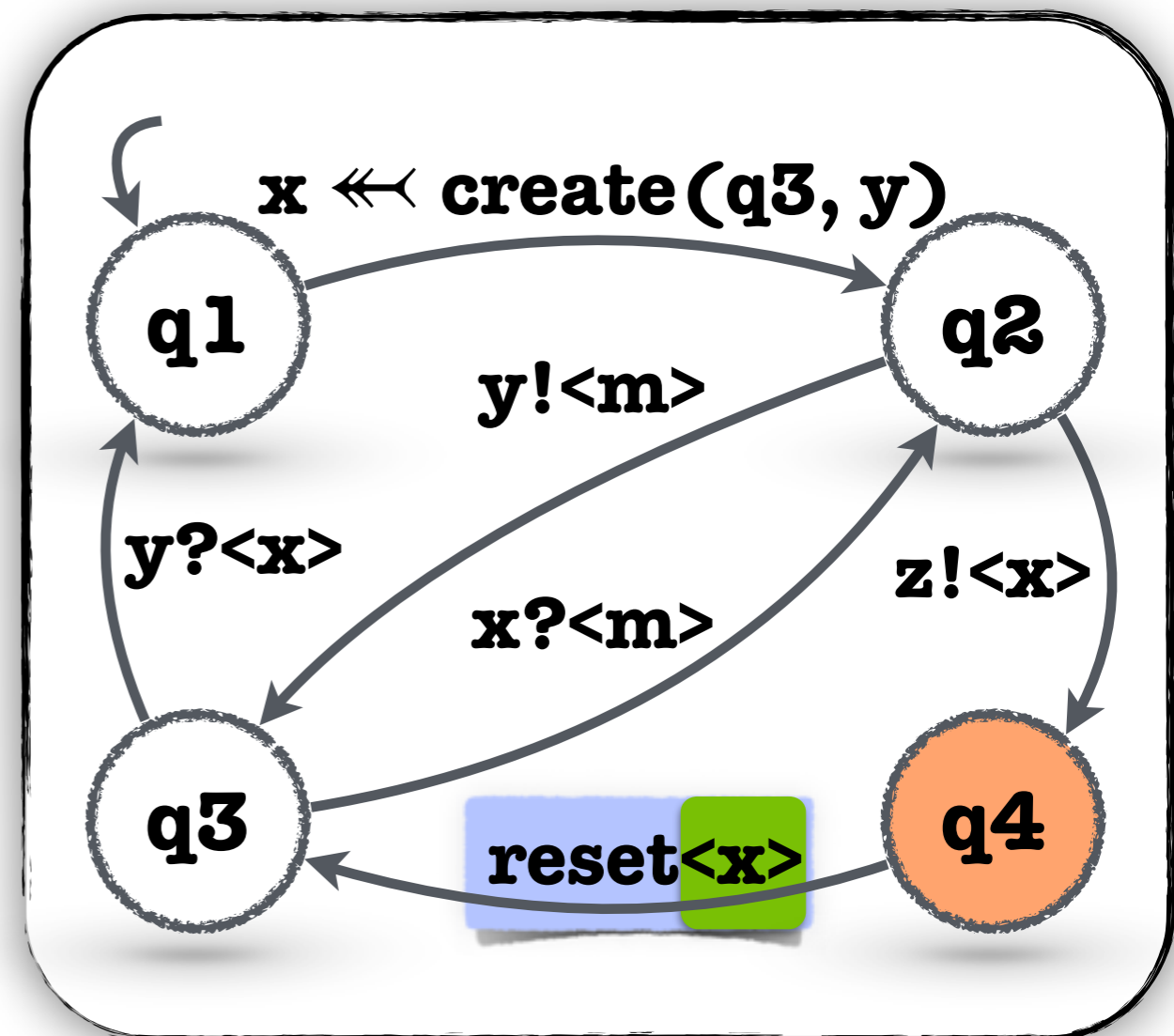
Verification of Dynamic Register Automata

Configuration Transition Relation

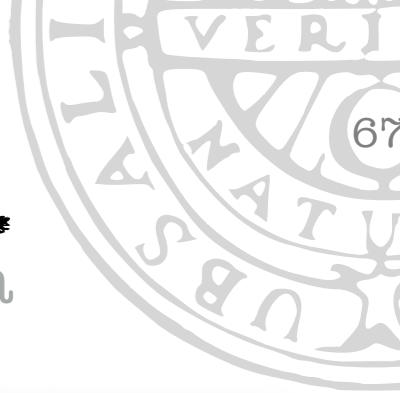


Process Model

Register Reset



Dynamic Register Automata



Verification of Dynamic Register Automata

Formal Model

Configuration

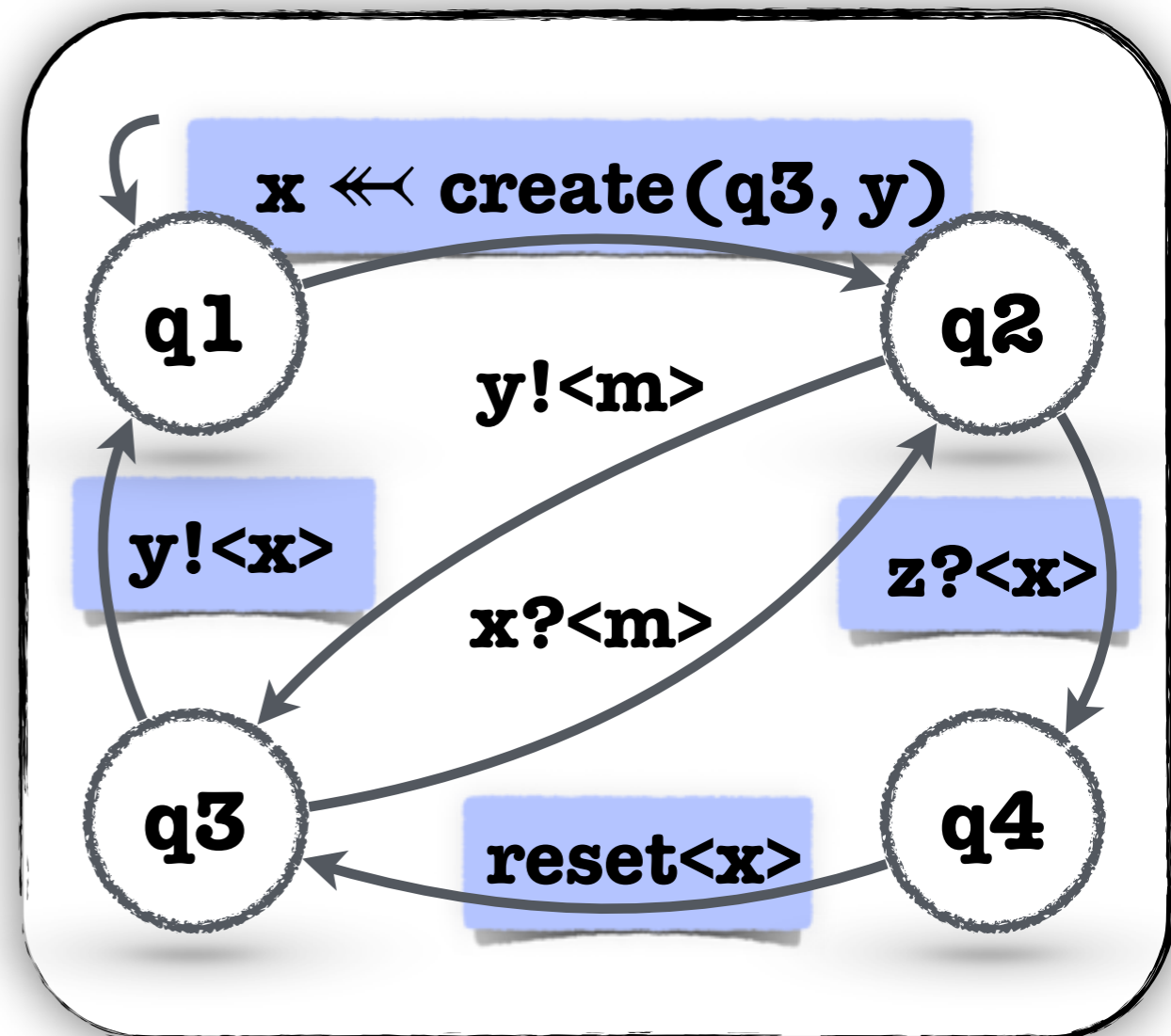
Transition Relation

Process Creation

Send & Receive ID

Register Reset

Process Model



Dynamic Register Automata

Verification of Dynamic Register Automata



Applications

Formal Model

Process Model

Configuration

Transition Relation

Dynamic Register Automata

Verification of Dynamic Register Automata



Applications

Formal Model

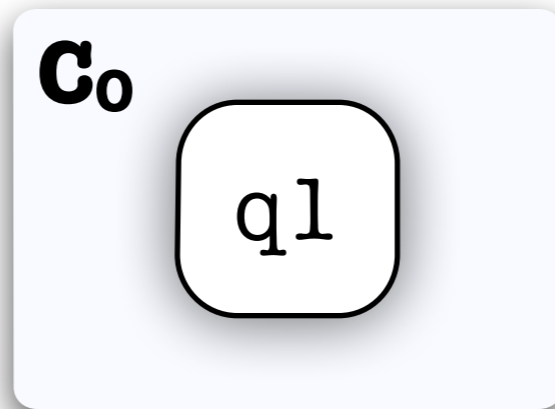
State Reachability

Dynamic Register Automata



State Reachability

Verification of Dynamic Register Automata



Initial Configuration

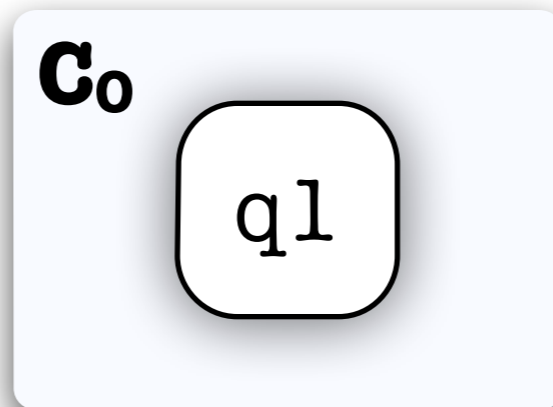
Dynamic Register Automata



State Reachability

Verification of Dynamic Register Automata

Initial Configuration



Run: C_0

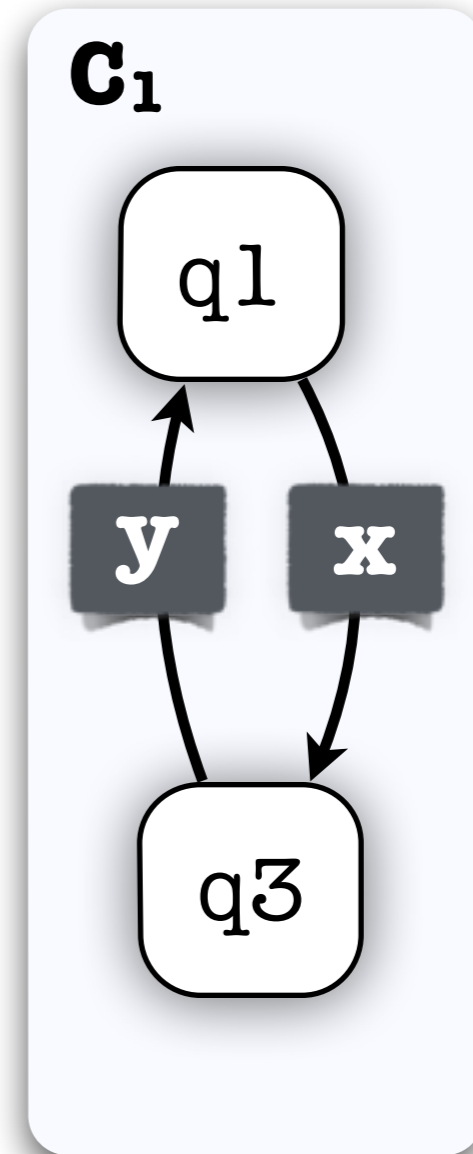
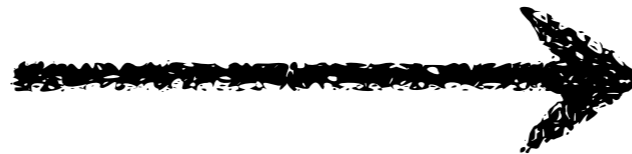
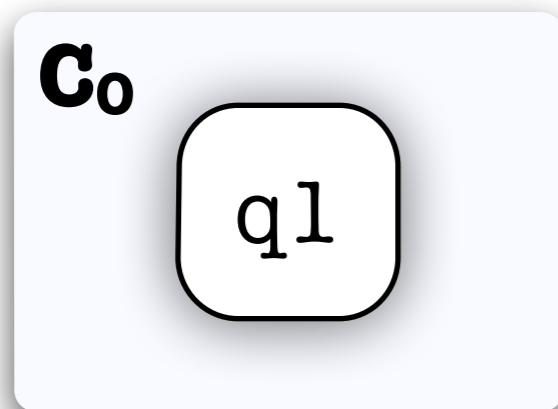
Dynamic Register Automata



State Reachability

Initial Configuration

Verification of Dynamic Register Automata



Run: C₀, C₁

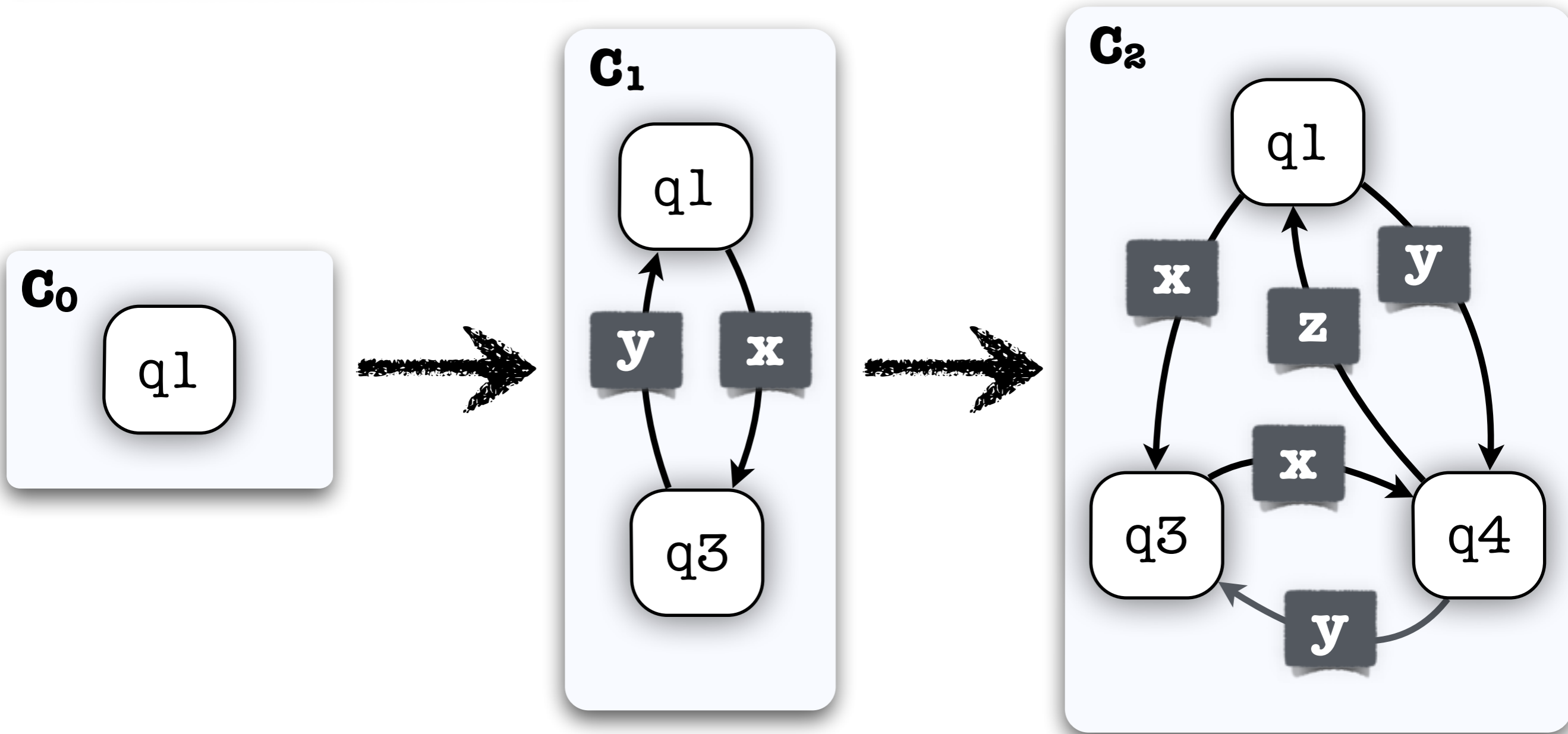
Dynamic Register Automata



State Reachability

Verification of Dynamic Register Automata

Initial Configuration



Run: C_0, C_1, C_2

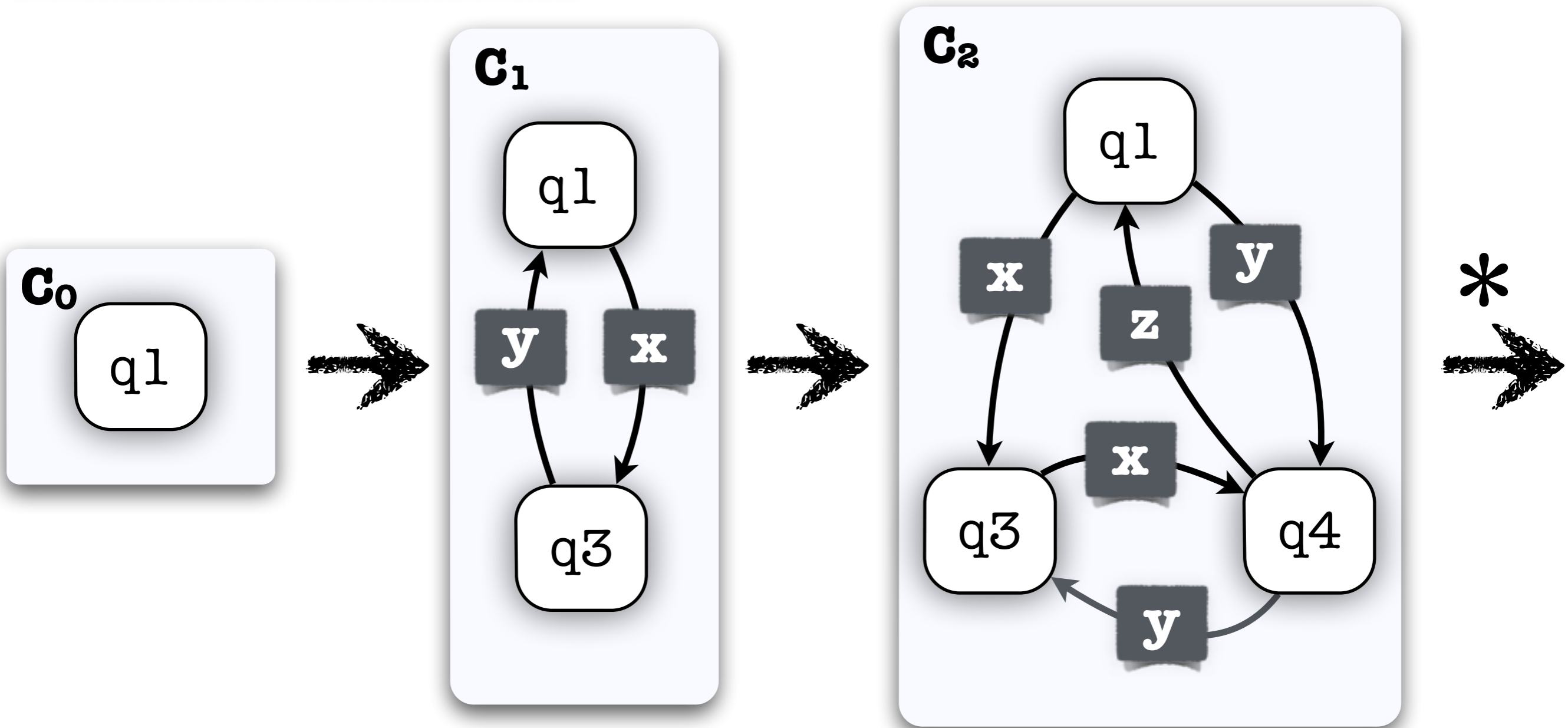
Dynamic Register Automata



State Reachability

Verification of Dynamic Register Automata

Initial Configuration



Run: C_0, C_1, C_2, \dots

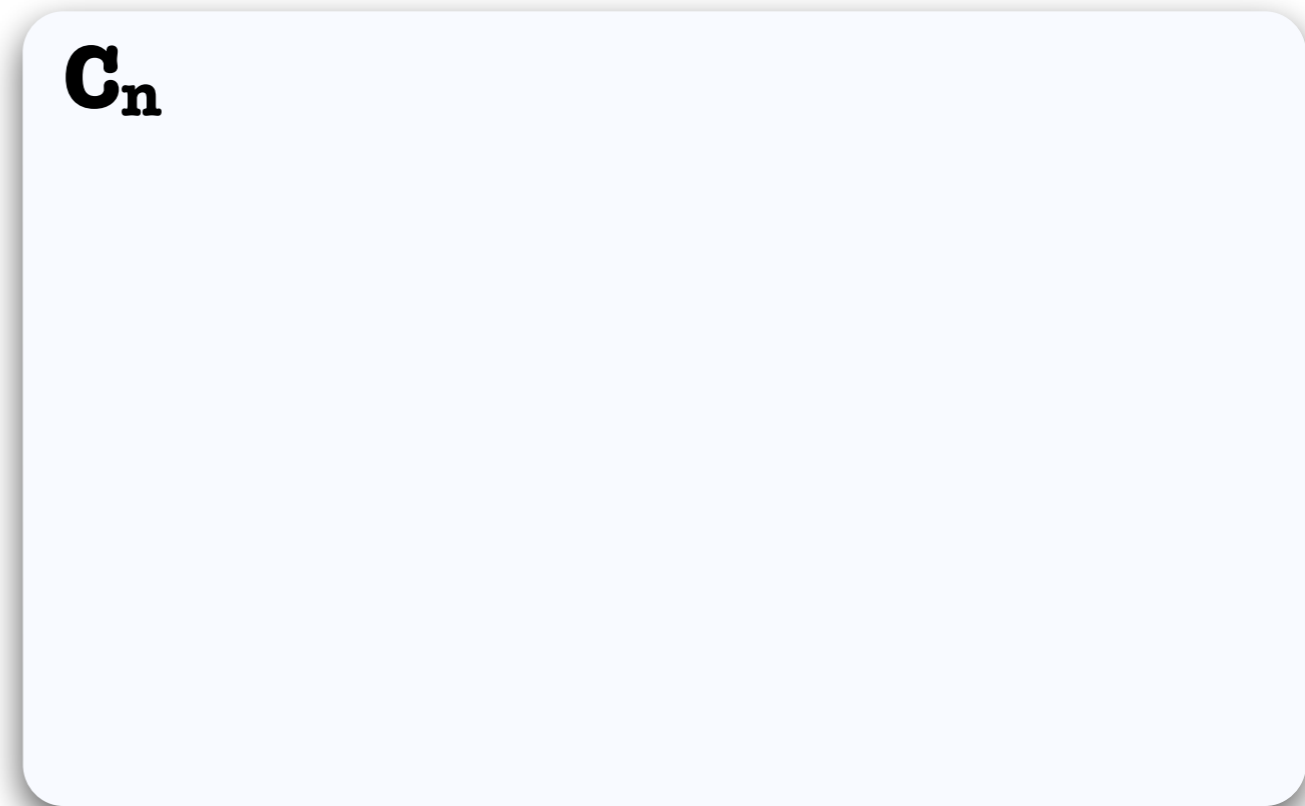
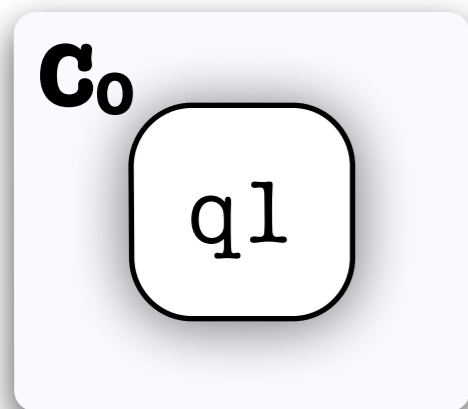
Dynamic Register Automata



State Reachability

Verification of Dynamic Register Automata

Initial Configuration



Run: $C_0, C_1, C_2, \dots, C_n$

Dynamic Register Automata



State Reachability

Verification of Dynamic Register Automata

Initial Configuration

Run: $C_0, C_1, C_2, \dots, C_n$

State Reachability Problem:

Dynamic Register Automata



Verification of Dynamic Register Automata

State Reachability

Initial Configuration

Run: $C_0, C_1, C_2, \dots, C_n$

State Reachability Problem:

Given a control state q_{BAD} , is there a run starting from the initial configuration that reaches a configuration where q_{BAD} occurs.

Dynamic Register Automata



Verification of Dynamic Register Automata

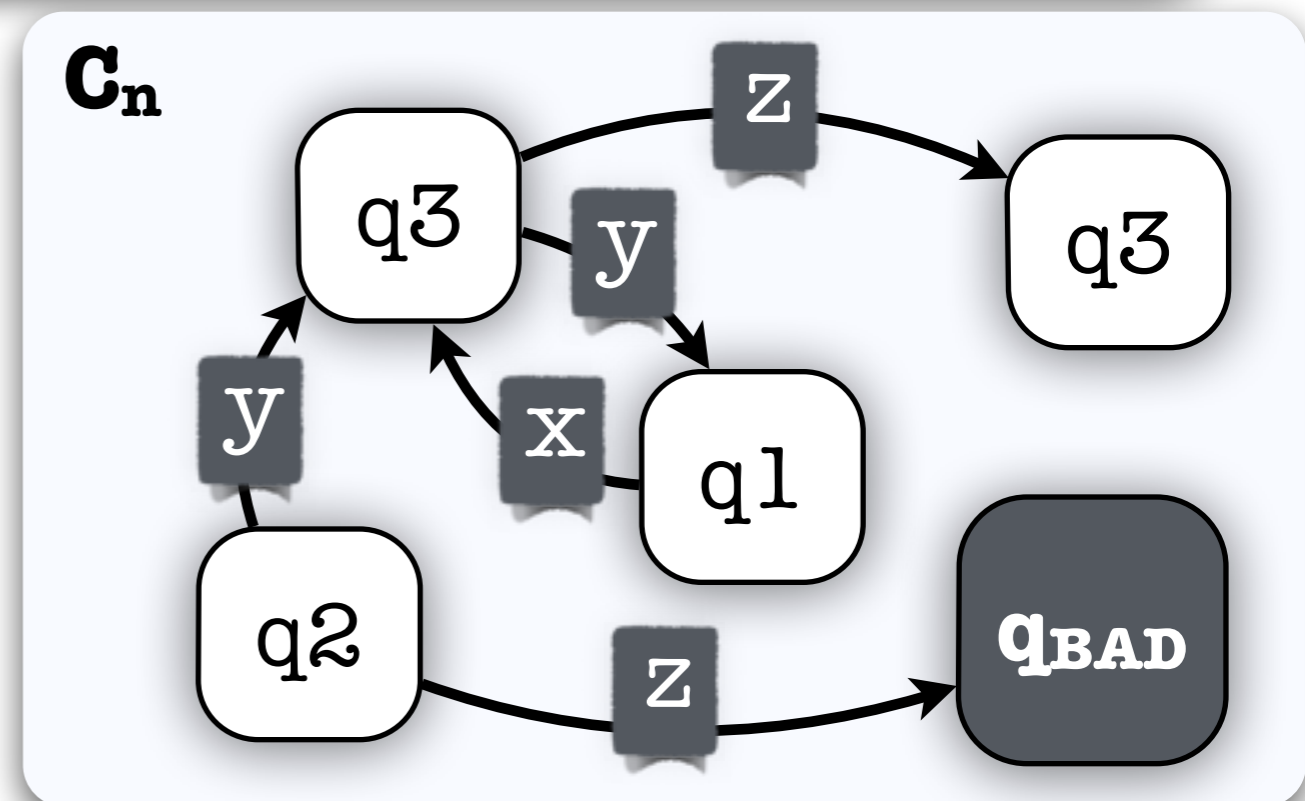
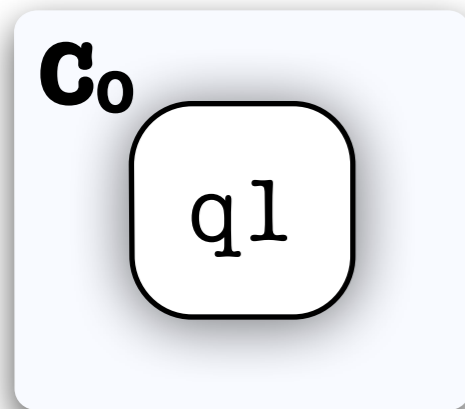
State Reachability

Initial Configuration

Run: $C_0, C_1, C_2, \dots, C_n$

State Reachability Problem:

Given a control state q_{BAD} , is there a run starting from the initial configuration that reaches a configuration where q_{BAD} occurs.



Dynamic Register Automata



Verification of Dynamic Register Automata

State Reachability

Initial Configuration

Run: $C_0, C_1, C_2, \dots, C_n$

State Reachability Problem:

Given a control state q_{BAD} , is there a run starting from the initial configuration that reaches a configuration where q_{BAD} occurs.

Undecidable



Dynamic Register Automata

Verification of Dynamic Register Automata



Applications

Formal Model

State Reachability

Undecidable

Contribution

Verification of Dynamic Register Automata

State Reachability

Study of the decidability and complexity for different sub-classes of the problem



Contribution

Verification of Dynamic Register Automata

State Reachability

Study of the decidability and complexity for different sub-classes of the problem

Bounded DRA

Undecidable

Contribution

Verification of Dynamic Register Automata

State Reachability

Study of the decidability and complexity for different sub-classes of the problem

Bounded DRA

Undecidable

Strongly Bounded DRA

Undecidable

Contribution

Verification of Dynamic Register Automata



State Reachability

Study of the decidability and complexity for different sub-classes of the problem

Bounded DRA

Undecidable

Strongly Bounded DRA

Undecidable

Strongly Safe DRA

Decidable

Non-Primitive Recursive

Contribution

Verification of Dynamic Register Automata



State Reachability

Study of the decidability and complexity for different sub-classes of the problem

Bounded DRA

Undecidable

Strongly Bounded DRA

Undecidable

Strongly Safe DRA

Decidable

Non-Primitive Recursive

Bounded DRA

Verification of Dynamic Register Automata



**Bound the Simple Path Length of the
configuration graph**

Bounded DRA

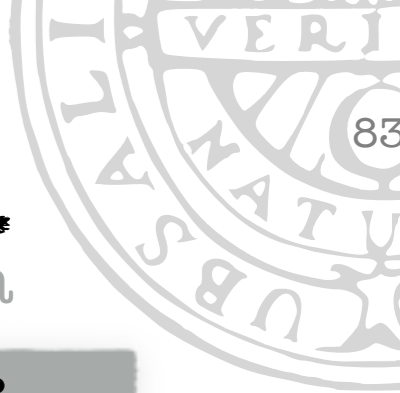
Verification of Dynamic Register Automata

Bound the Simple Path Length of the configuration graph

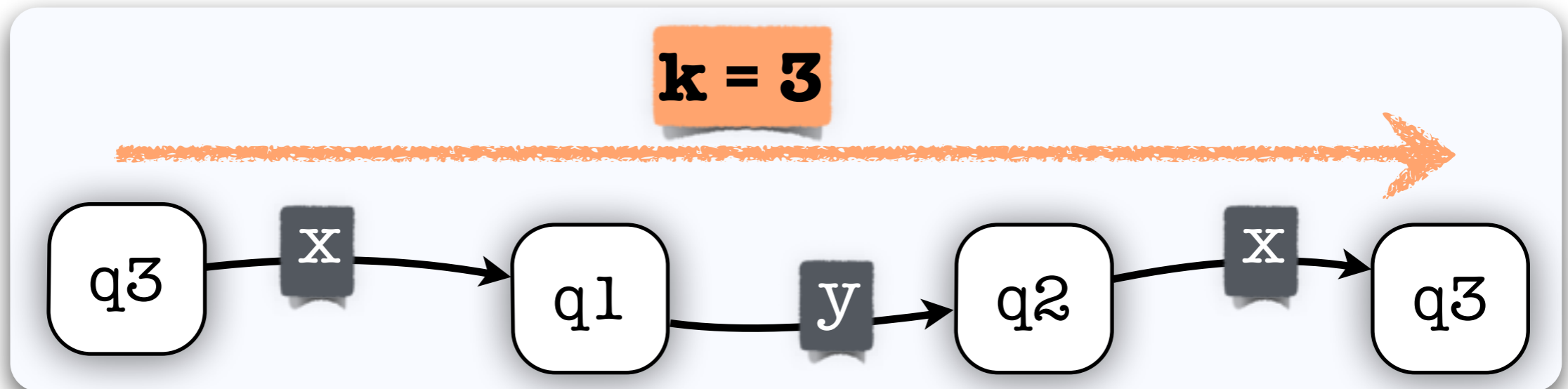


Bounded DRA

Verification of Dynamic Register Automata



Bound the Simple Path Length of the configuration graph

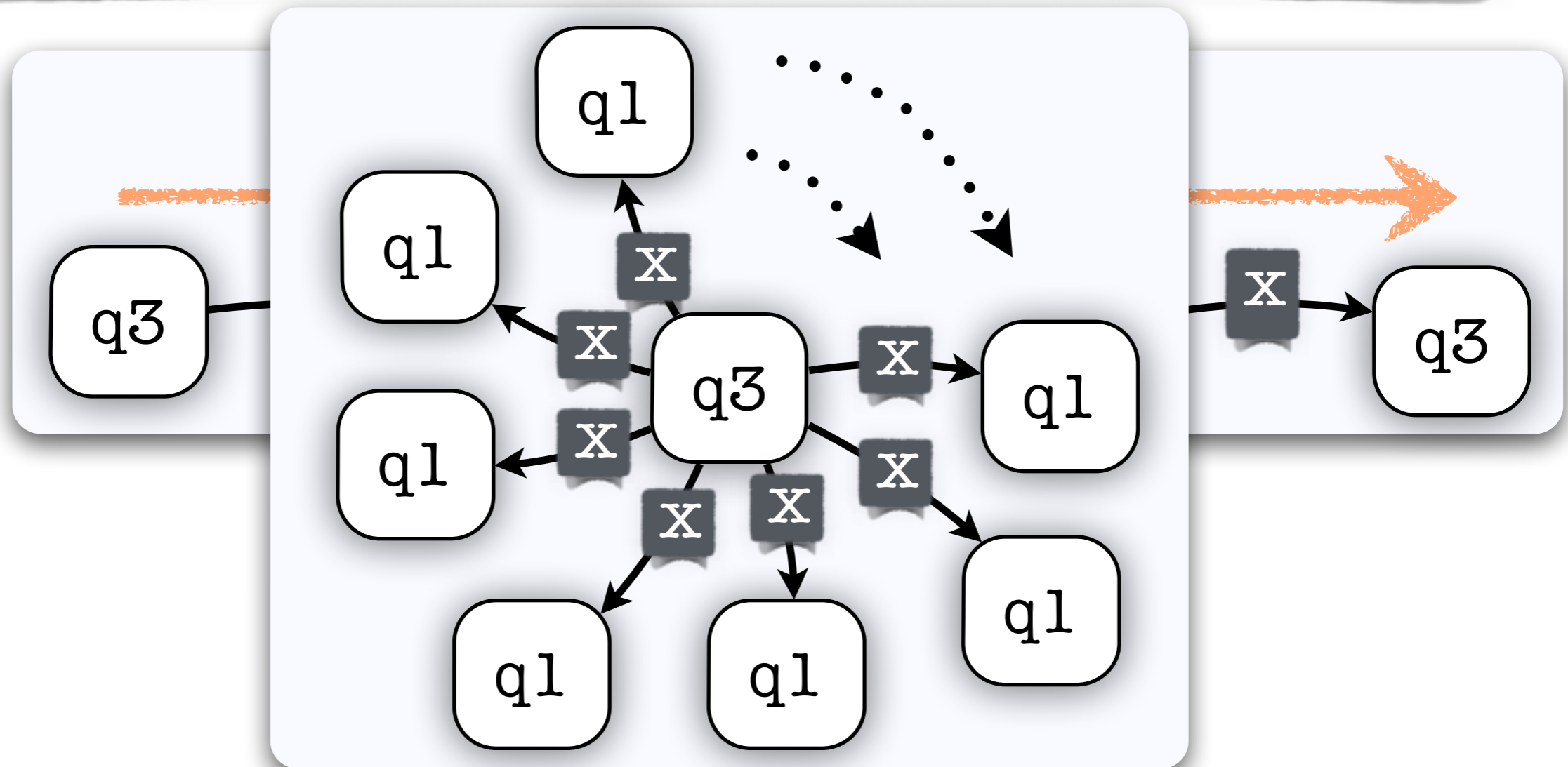


Bounded DRA

Verification of Dynamic Register Automata



Bound the Simple Path Length of the configuration graph

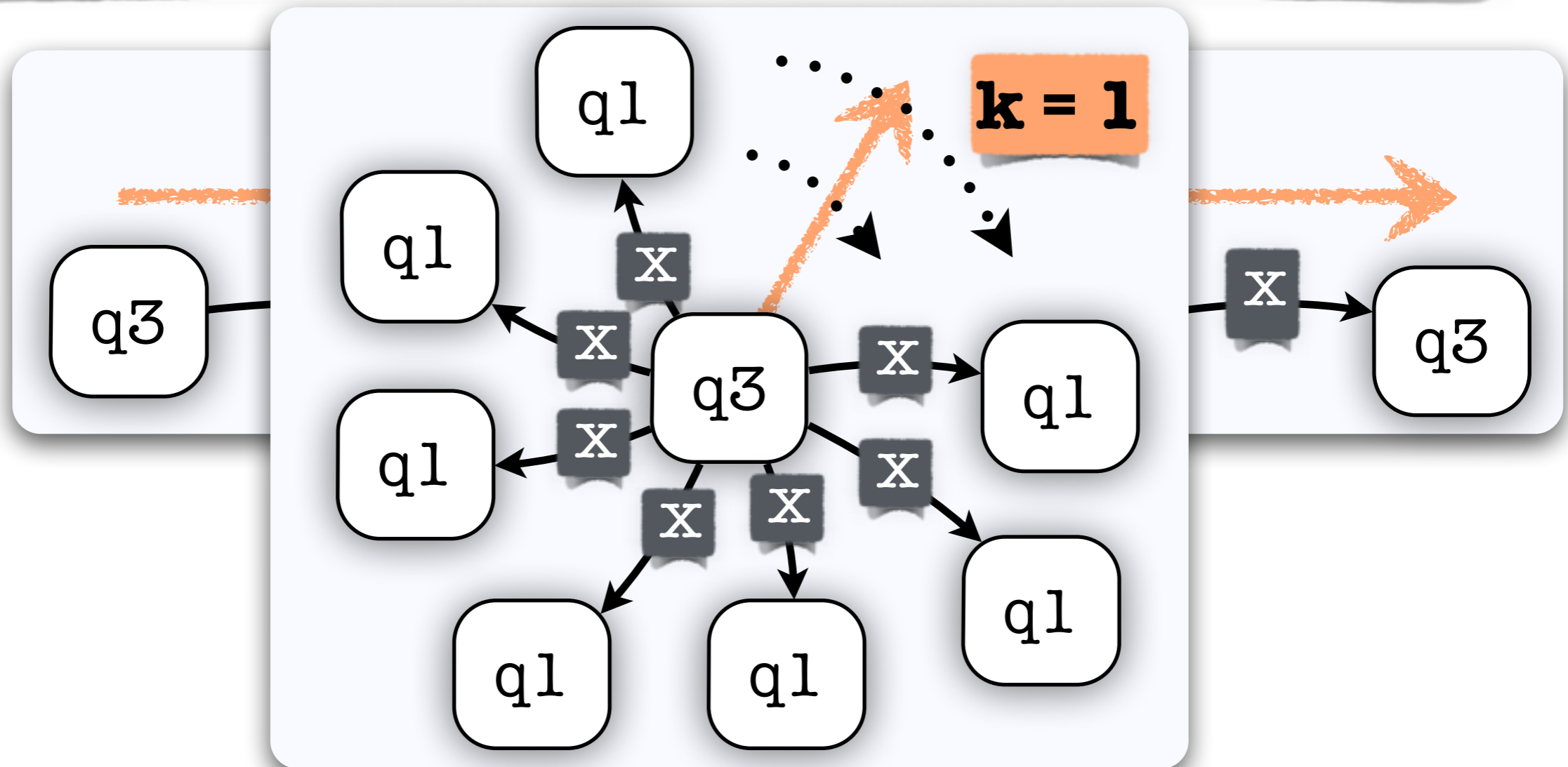


Bounded DRA

Verification of Dynamic Register Automata



Bound the Simple Path Length of the configuration graph

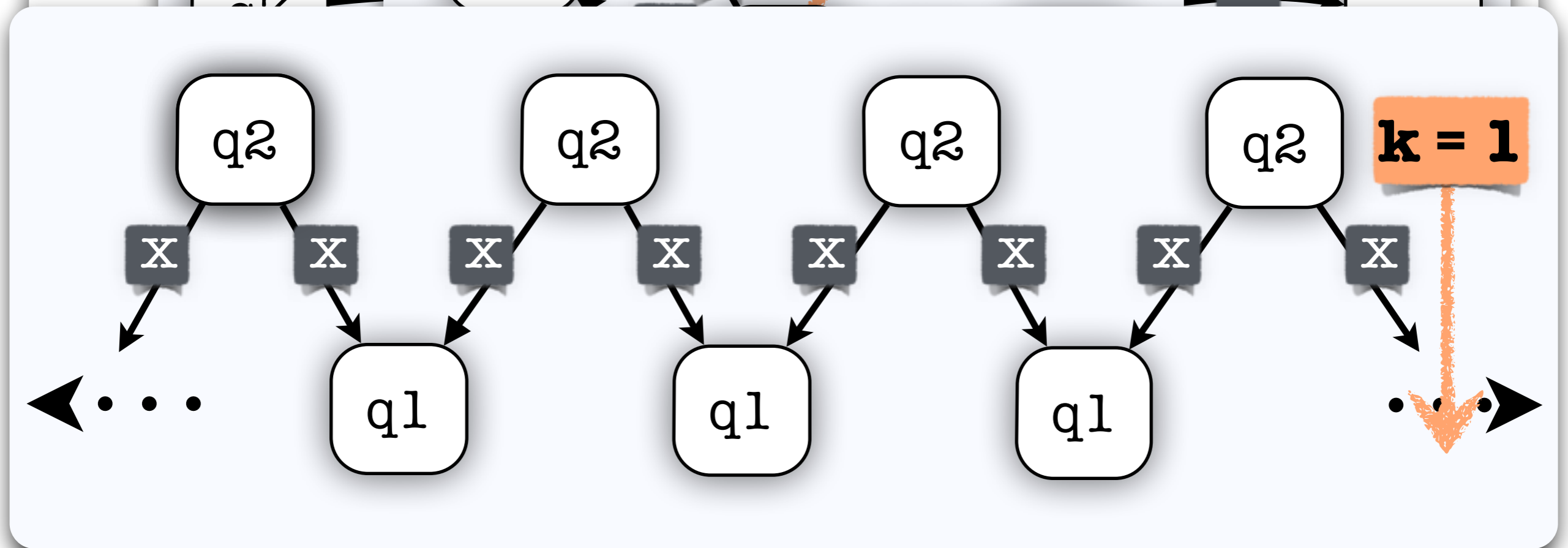
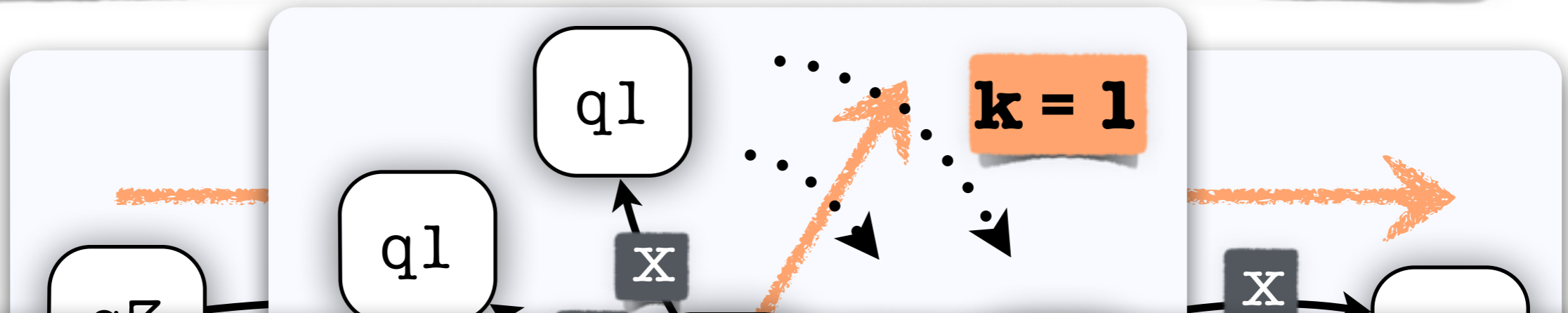


Bounded DRA

Verification of Dynamic Register Automata

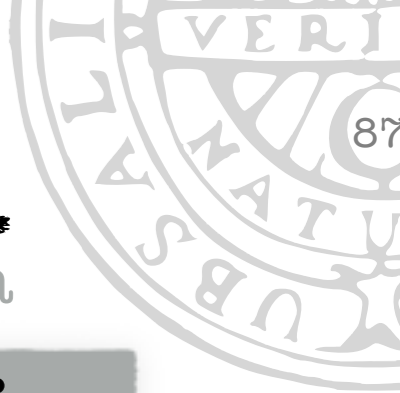


Bound the Simple Path Length of the configuration graph

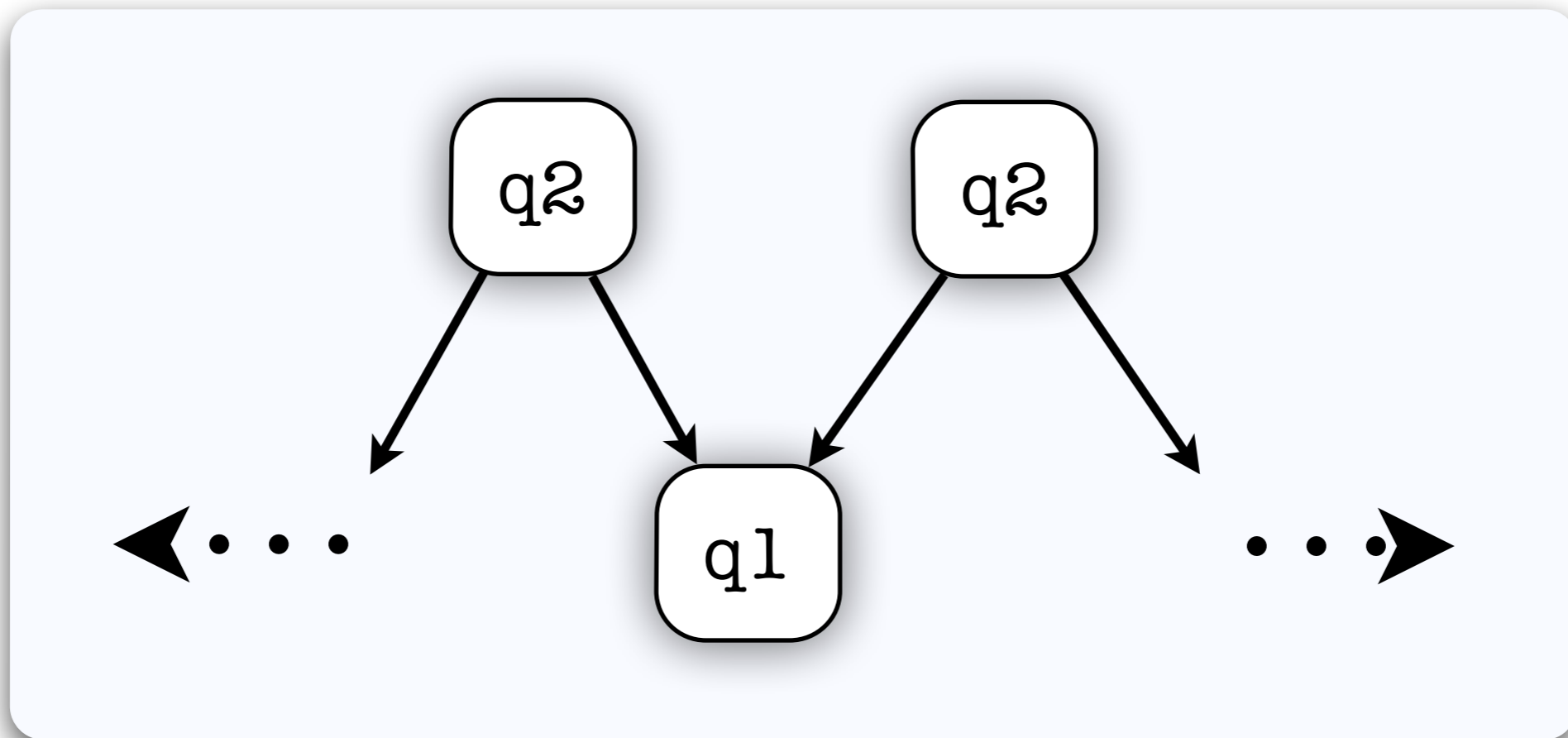


Bounded DRA

Verification of Dynamic Register Automata

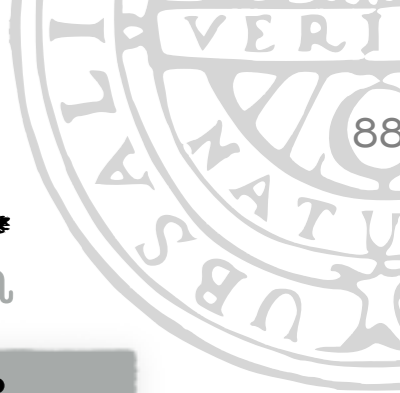


Bound the Simple Path Length of the configuration graph

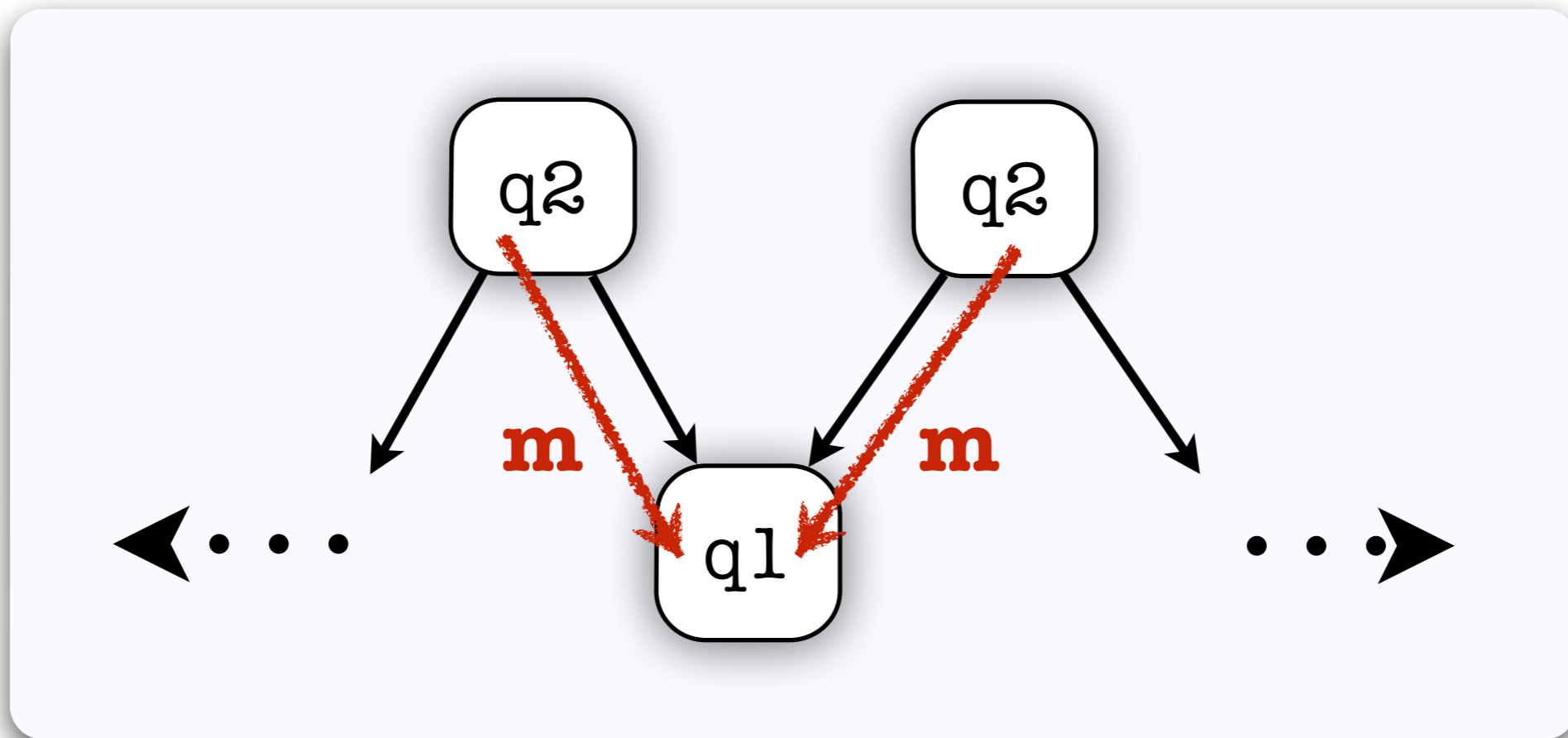


Bounded DRA

Verification of Dynamic Register Automata



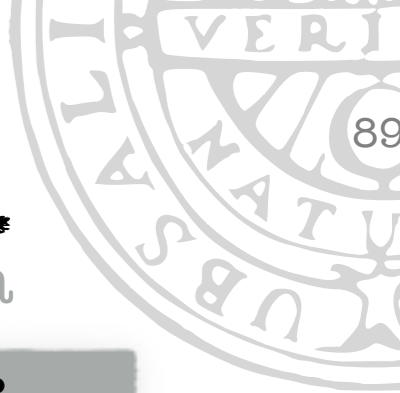
Bound the Simple Path Length of the configuration graph



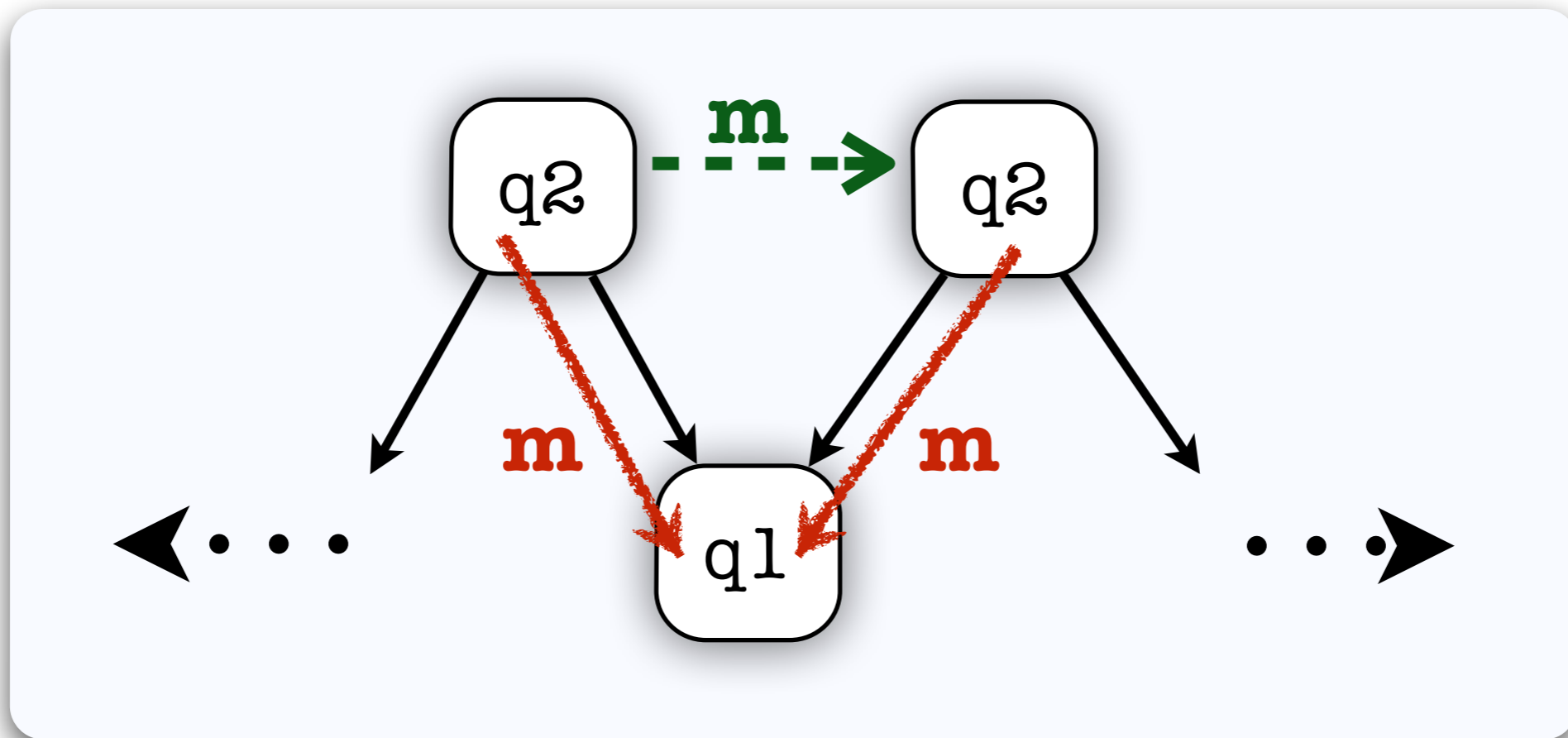
Using Rendez-Vous Communication

Bounded DRA

Verification of Dynamic Register Automata



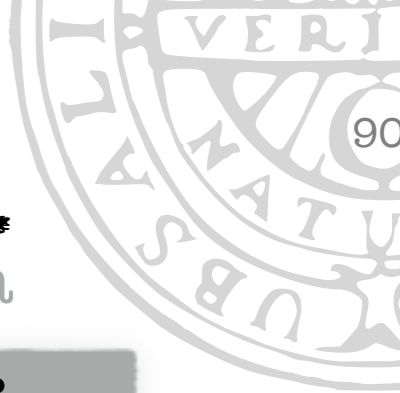
Bound the Simple Path Length of the configuration graph



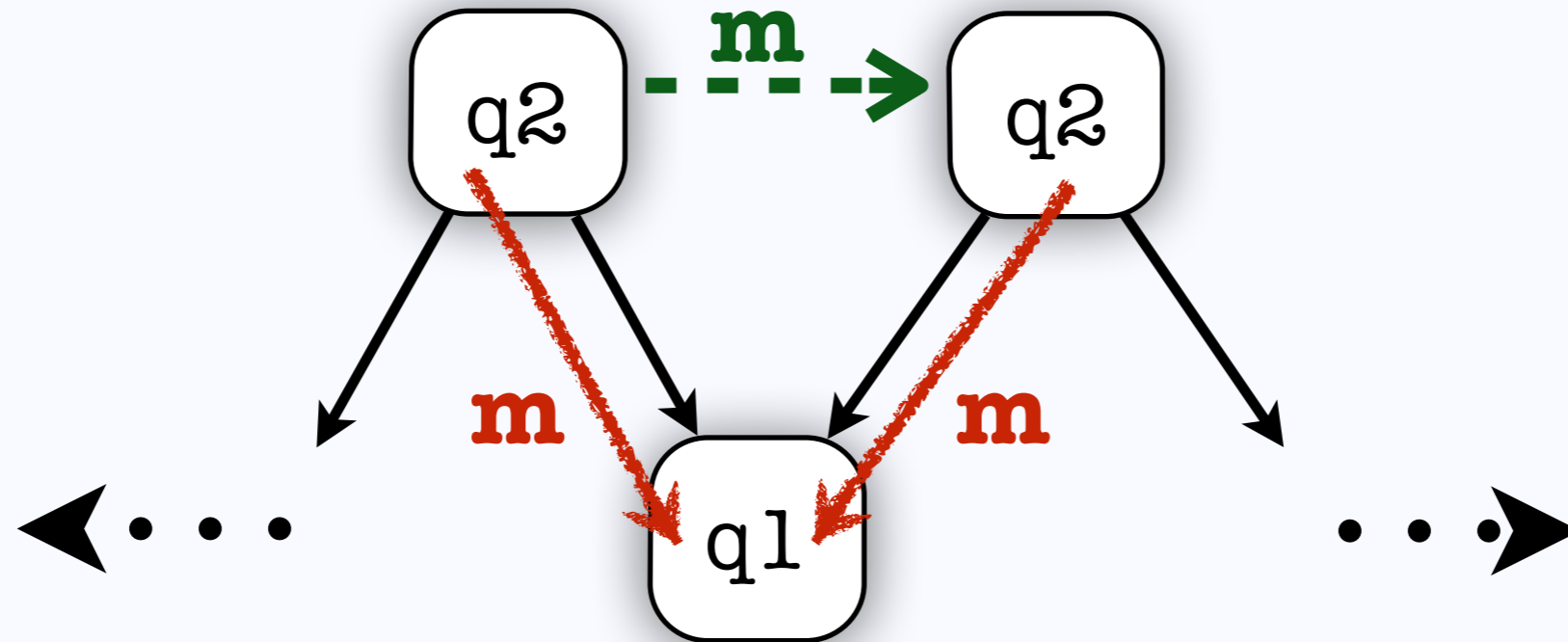
Using Rendez-Vous Communication

Bounded DRA

Verification of Dynamic Register Automata



Bound the Simple Path Length of the configuration graph



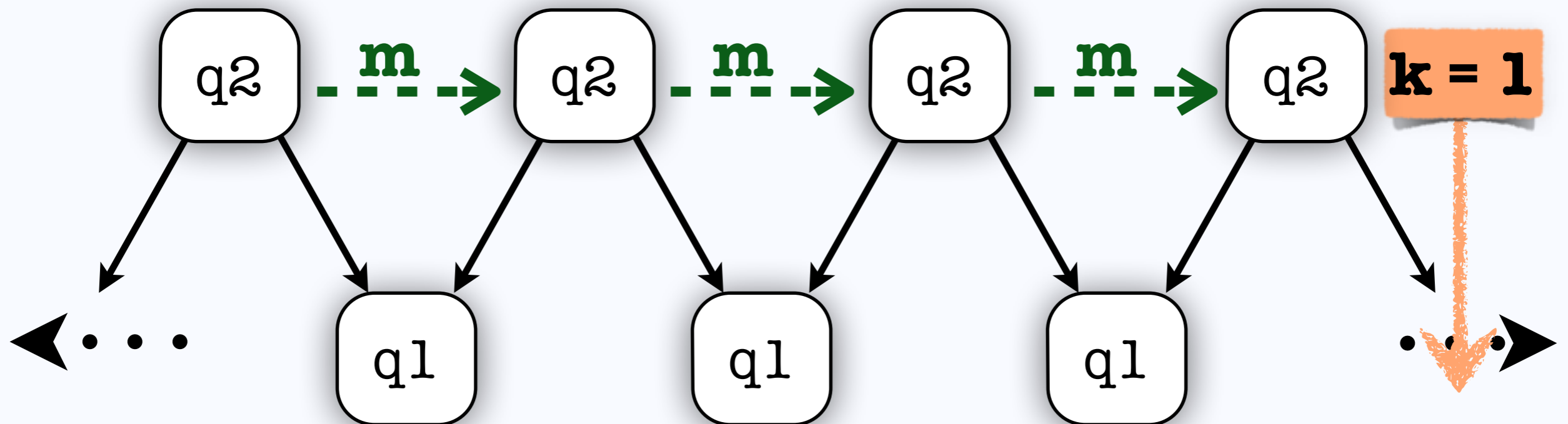
Using Rendez-Vous Communication

Bounded DRA

Verification of Dynamic Register Automata



Bound the Simple Path Length of the configuration graph



Undecidable

Contribution

Verification of Dynamic Register Automata



State Reachability

Bounded DRA

Undecidable

Strongly Bounded DRA

Undecidable

Strongly Safe DRA

Decidable

Non-Primitive Recursive

Contribution

Verification of Dynamic Register Automata



State Reachability

Bounded DRA

Undecidable

Strongly Bounded DRA

Undecidable

Strongly Safe DRA

Decidable

Non-Primitive Recursive

Strongly Bounded DRA

Verification of Dynamic Register Automata

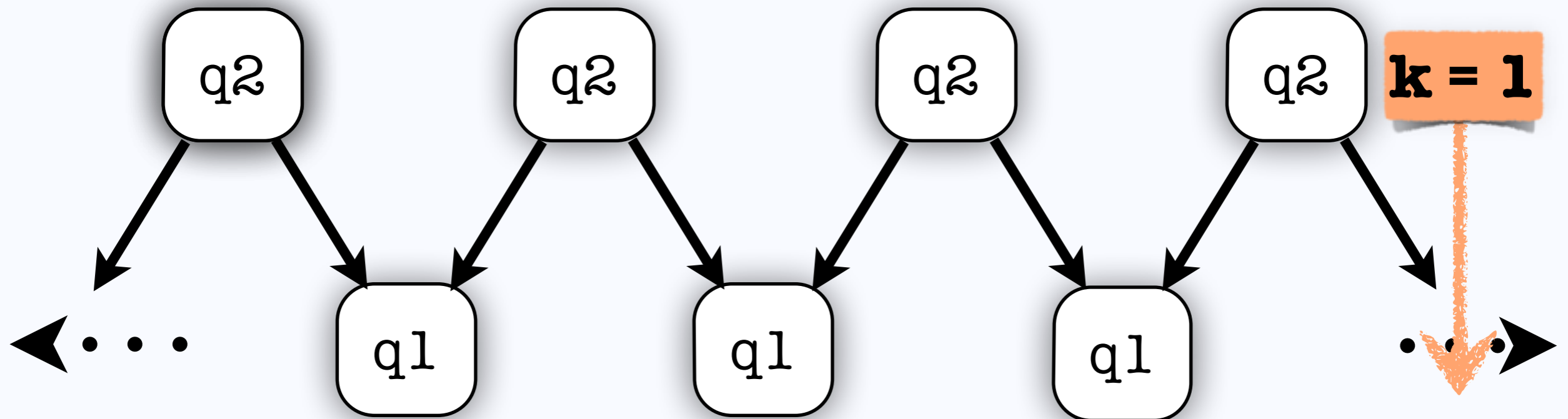


**Bound the Simple Path Length of the
underlying undirected configuration graph**

Strongly Bounded DRA

Verification of Dynamic Register Automata

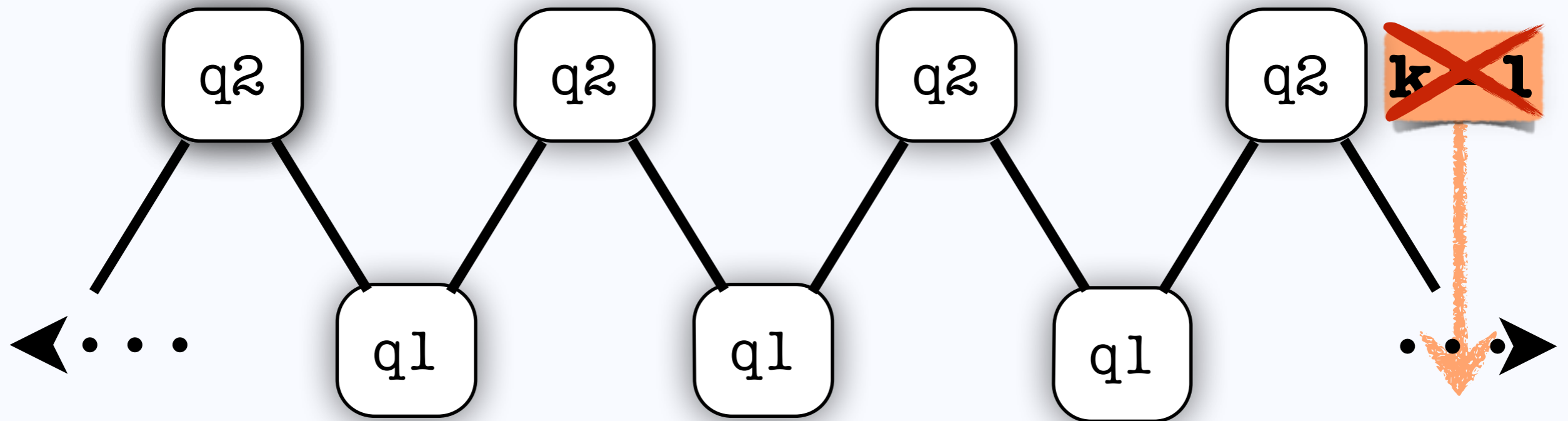
Bound the Simple Path Length of the underlying
undirected configuration graph



Strongly Bounded DRA

Verification of Dynamic Register Automata

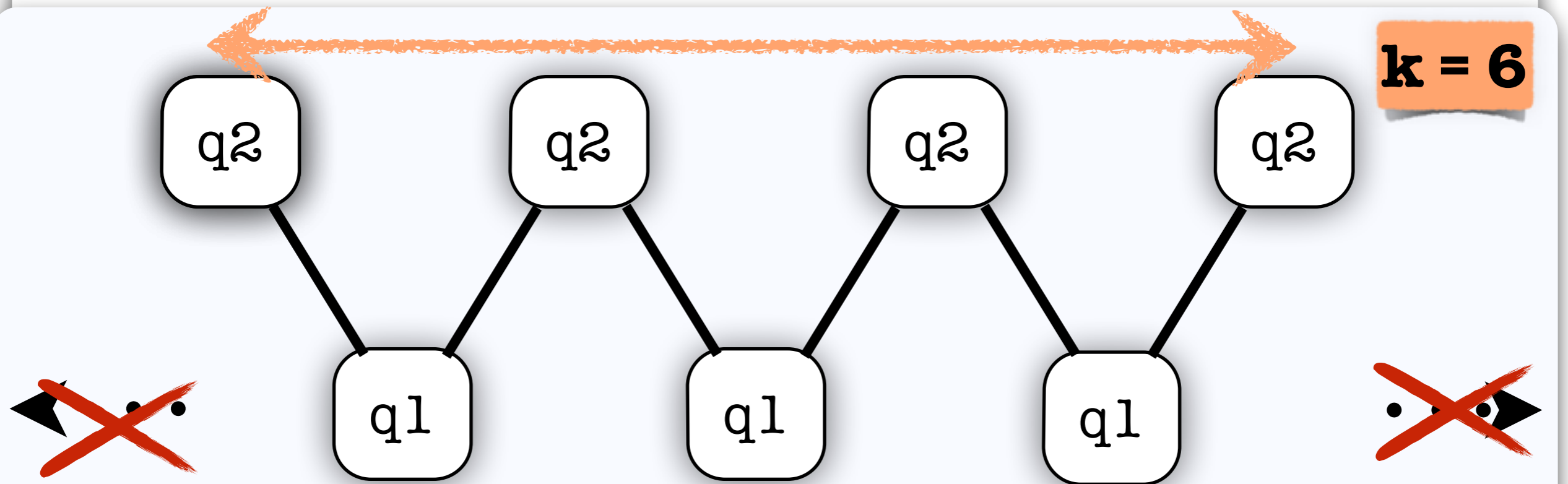
Bound the Simple Path Length of the underlying
undirected configuration graph



Strongly Bounded DRA

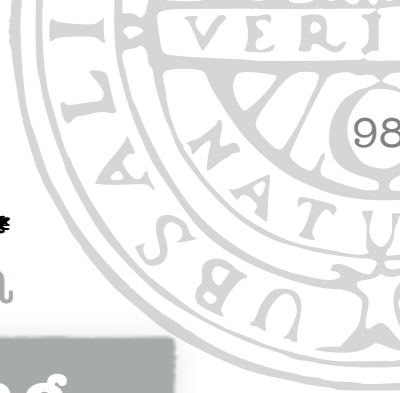
Verification of Dynamic Register Automata

Bound the Simple Path Length of the underlying
undirected configuration graph

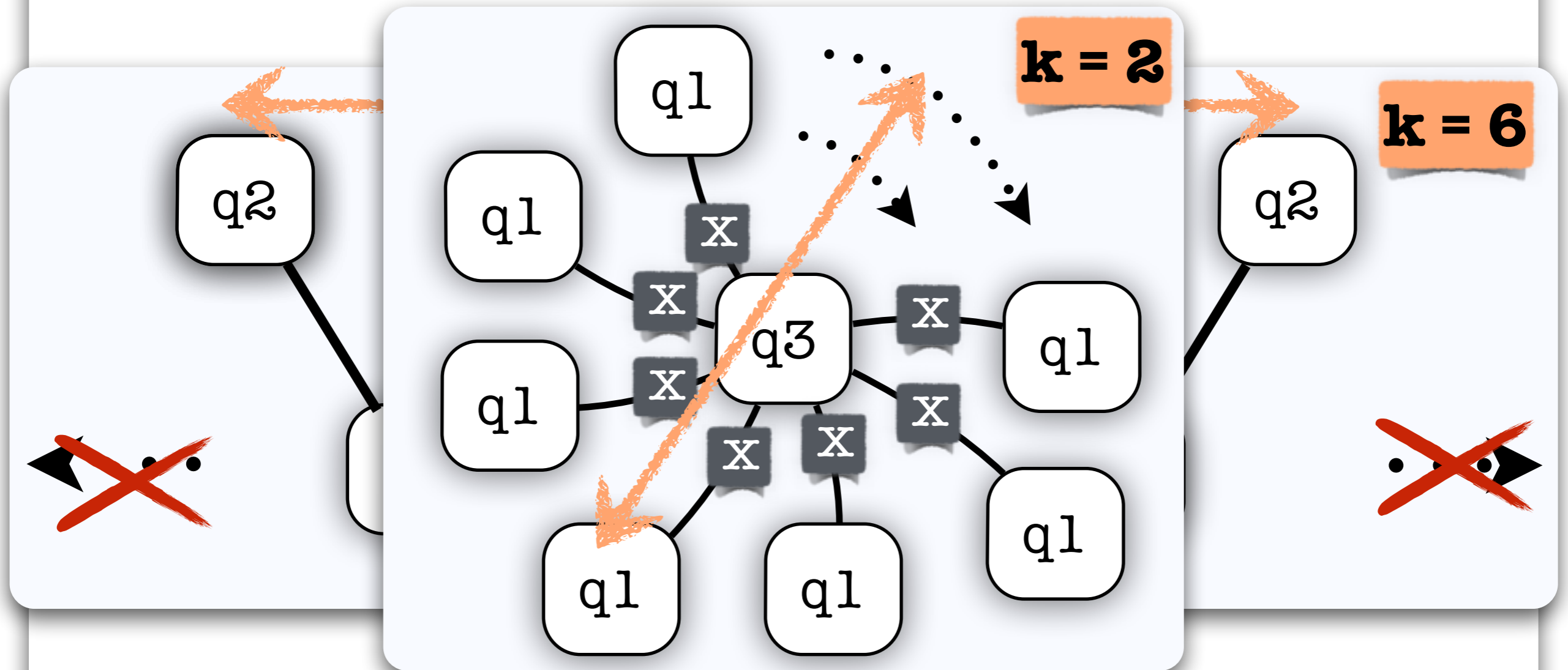


Strongly Bounded DRA

Verification of Dynamic Register Automata



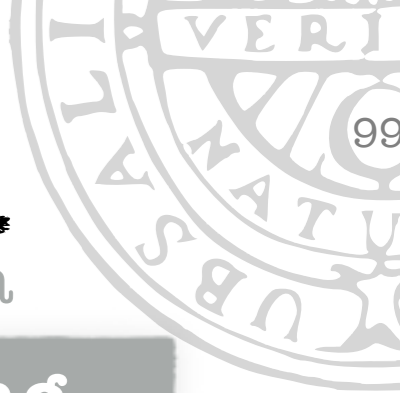
Bound the Simple Path Length of the underlying undirected configuration graph



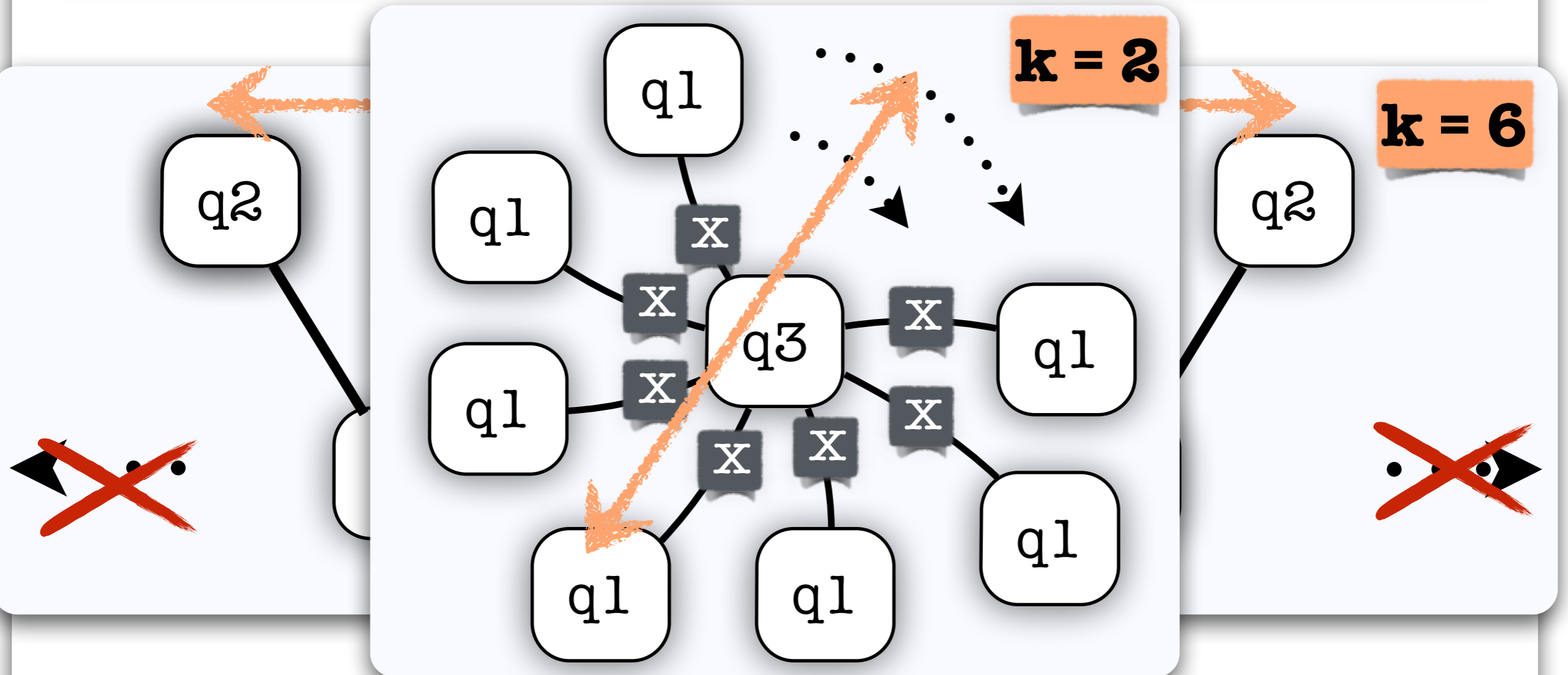
Still: Unbounded Number of Processes

Strongly Bounded DRA

Verification of Dynamic Register Automata



Bound the Simple Path Length of the underlying undirected configuration graph



Undecidable

Strongly Bounded DRA

Verification of Dynamic Register Automata

Bound the Simple Path Length of the underlying
undirected configuration graph **Undecidable**

Two counters Minsky Machine

Strongly Bounded DRA

Verification of Dynamic Register Automata

Bound the Simple Path Length of the underlying
undirected configuration graph **Undecidable**

Two counters Minsky Machine



Strongly-Bounded Reachability

Strongly Bounded DRA

Verification of Dynamic Register Automata

Bound the Simple Path Length of the underlying
undirected configuration graph **Undecidable**

Two counters Minsky Machine

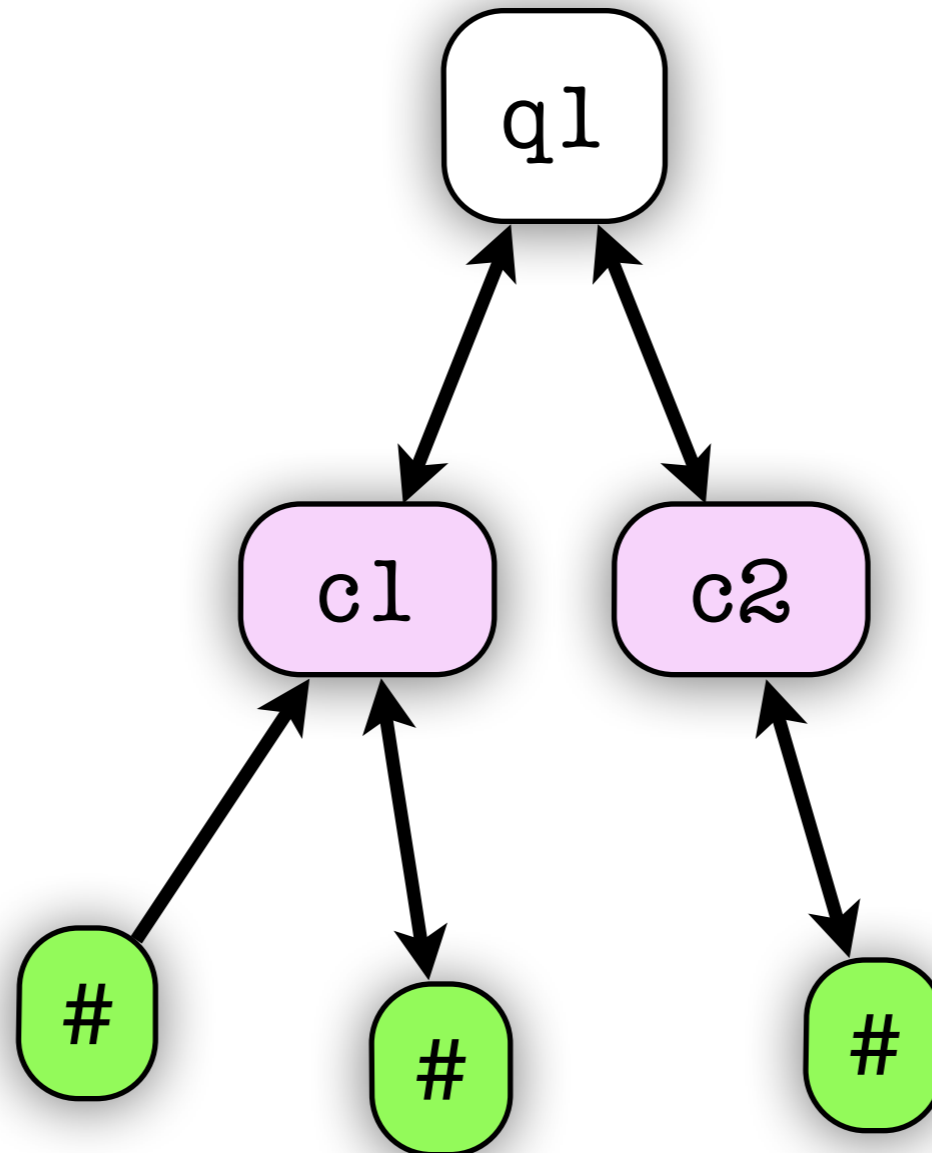


k = 4 Strongly-Bounded Reachability

Strongly Bounded DRA

Verification of Dynamic Register Automata

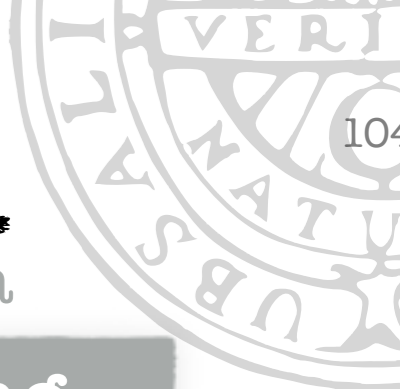
Bound the Simple Path Length of the underlying
undirected configuration graph **Undecidable**



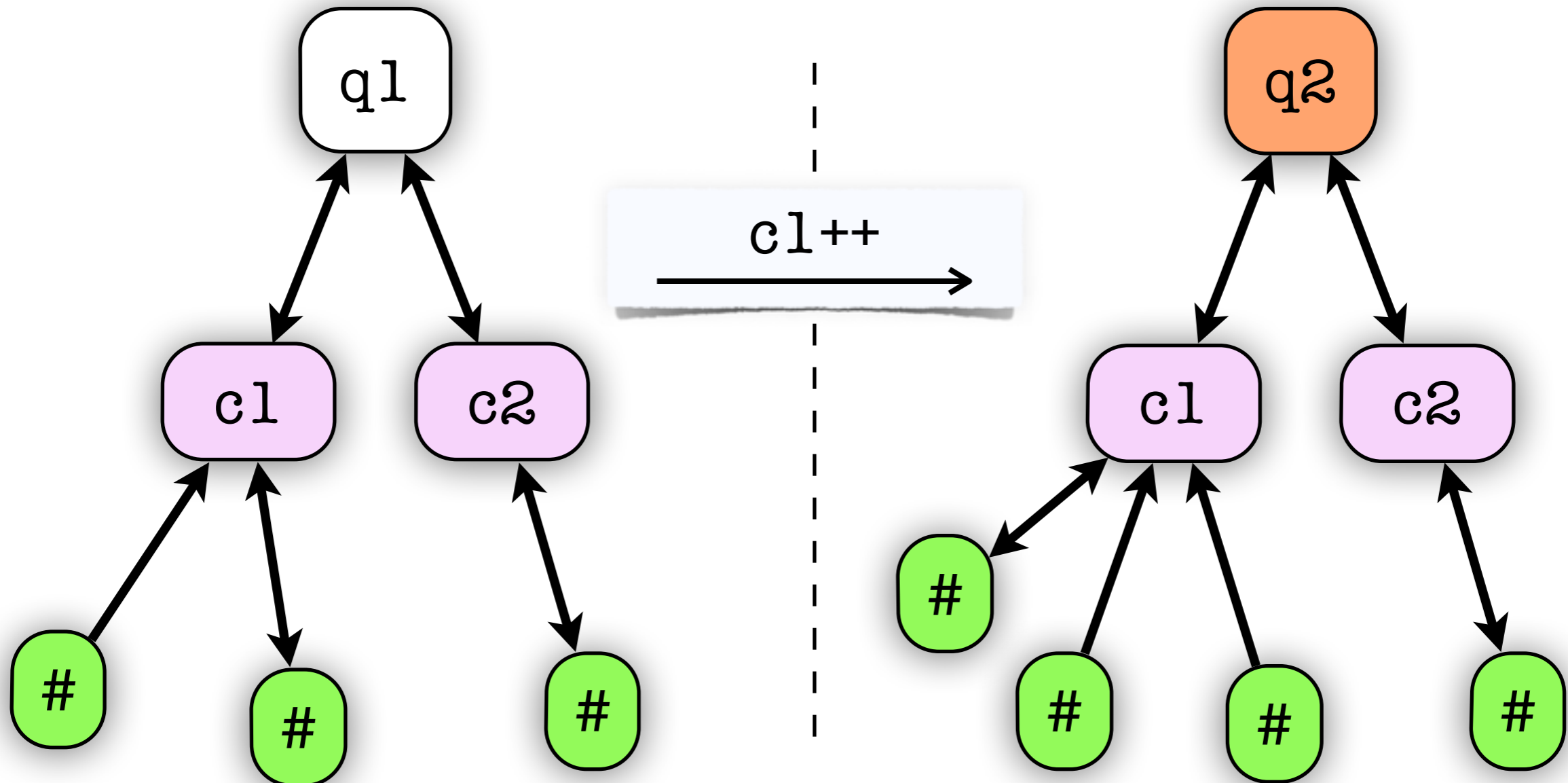
Two counters Minsky Machine

Strongly Bounded DRA

Verification of Dynamic Register Automata



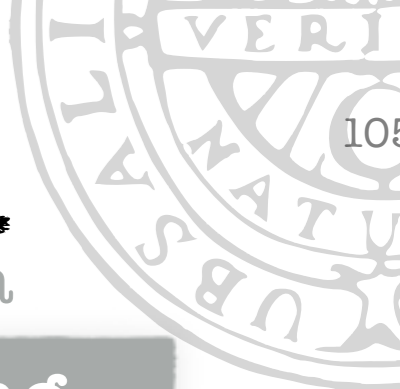
Bound the Simple Path Length of the underlying undirected configuration graph **Undecidable**



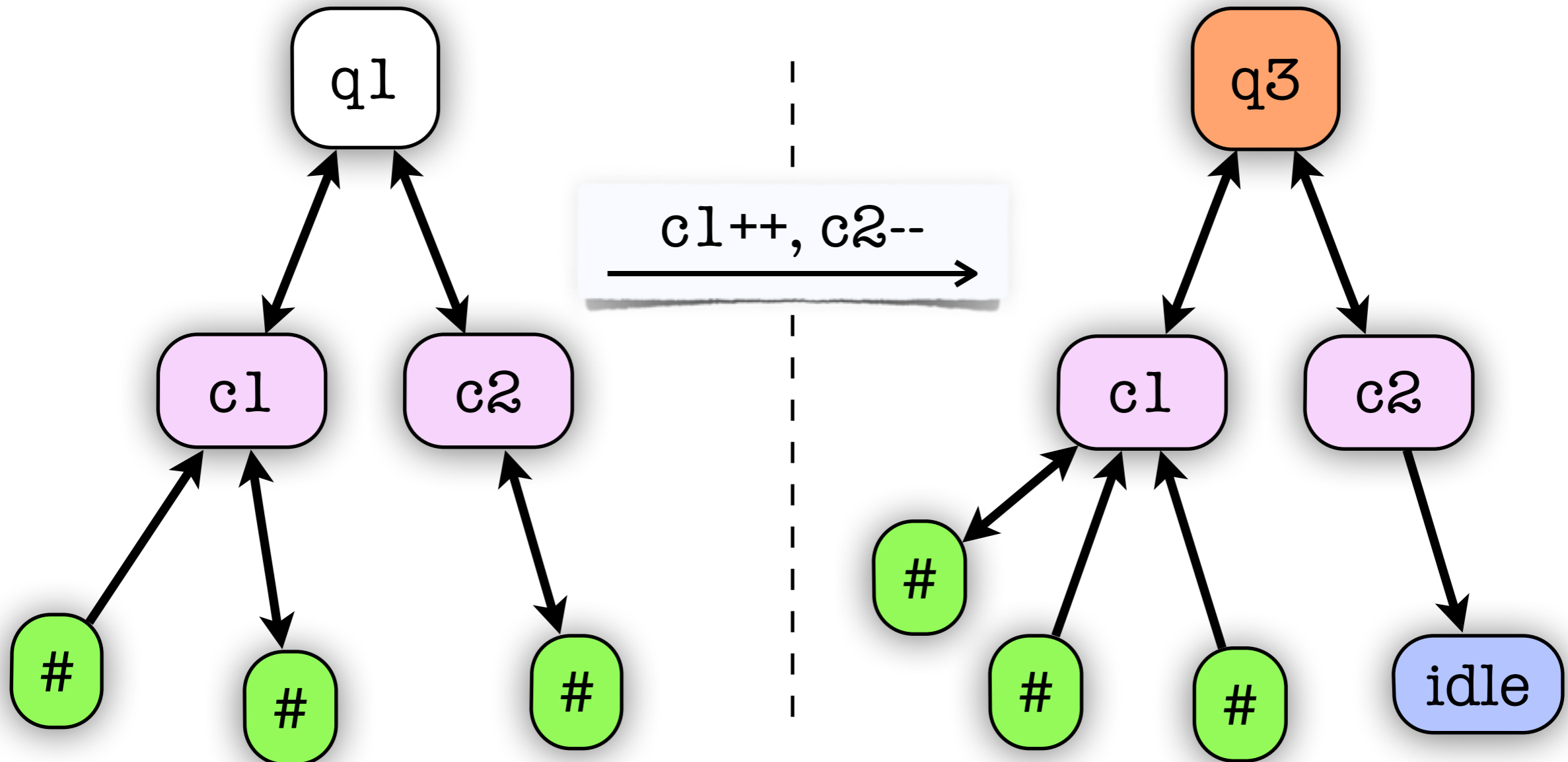
Two counters Minsky Machine

Strongly Bounded DRA

Verification of Dynamic Register Automata



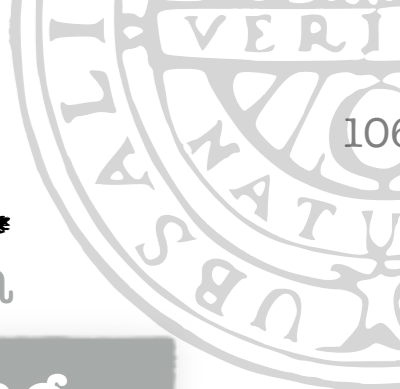
Bound the Simple Path Length of the underlying undirected configuration graph **Undecidable**



Two counters Minsky Machine

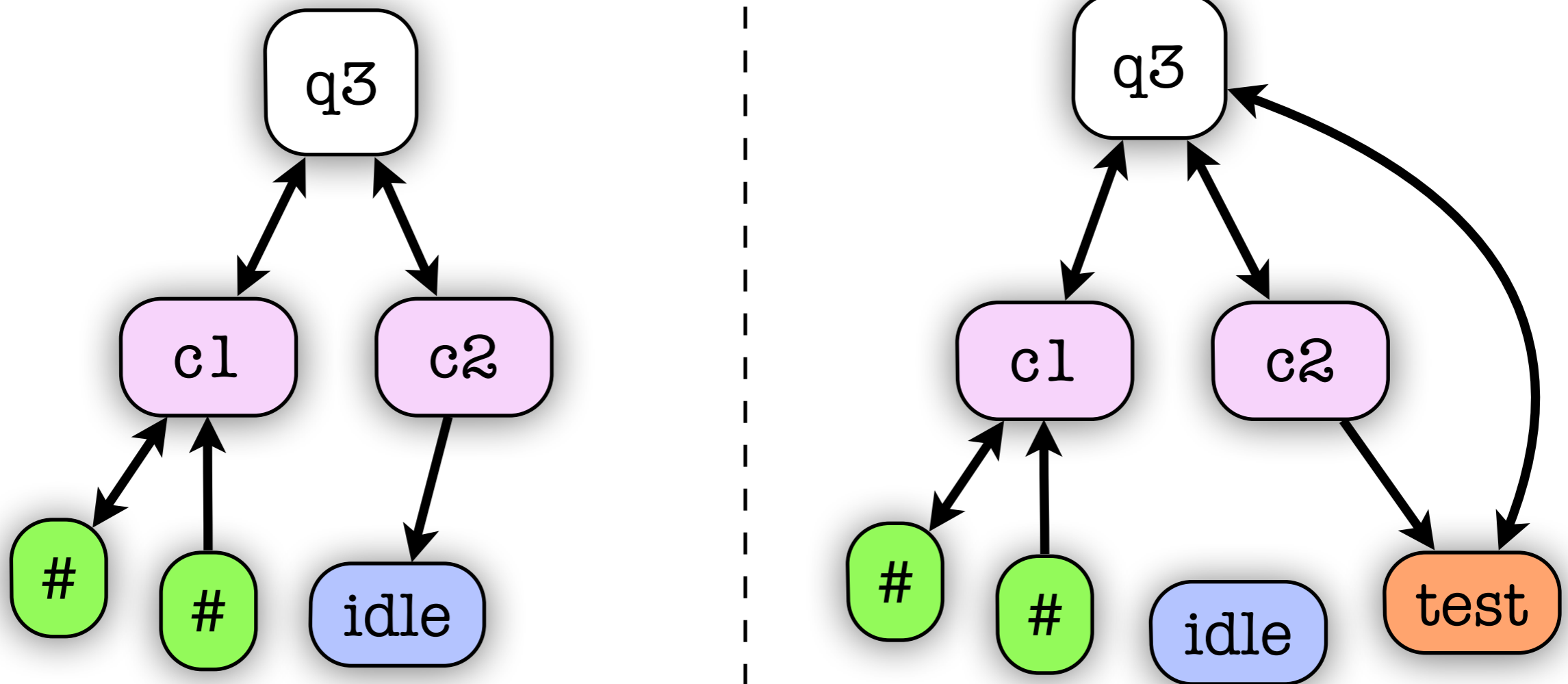
Strongly Bounded DRA

Verification of Dynamic Register Automata



Bound the Simple Path Length of the underlying undirected configuration graph **Undecidable**

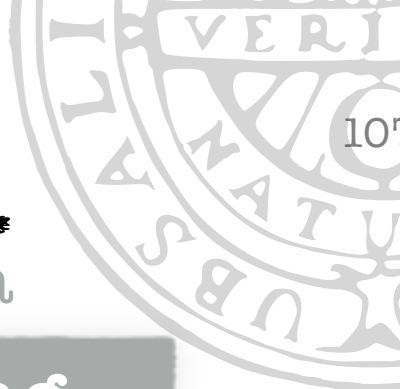
`zerotest(c2)`



Two counters Minsky Machine

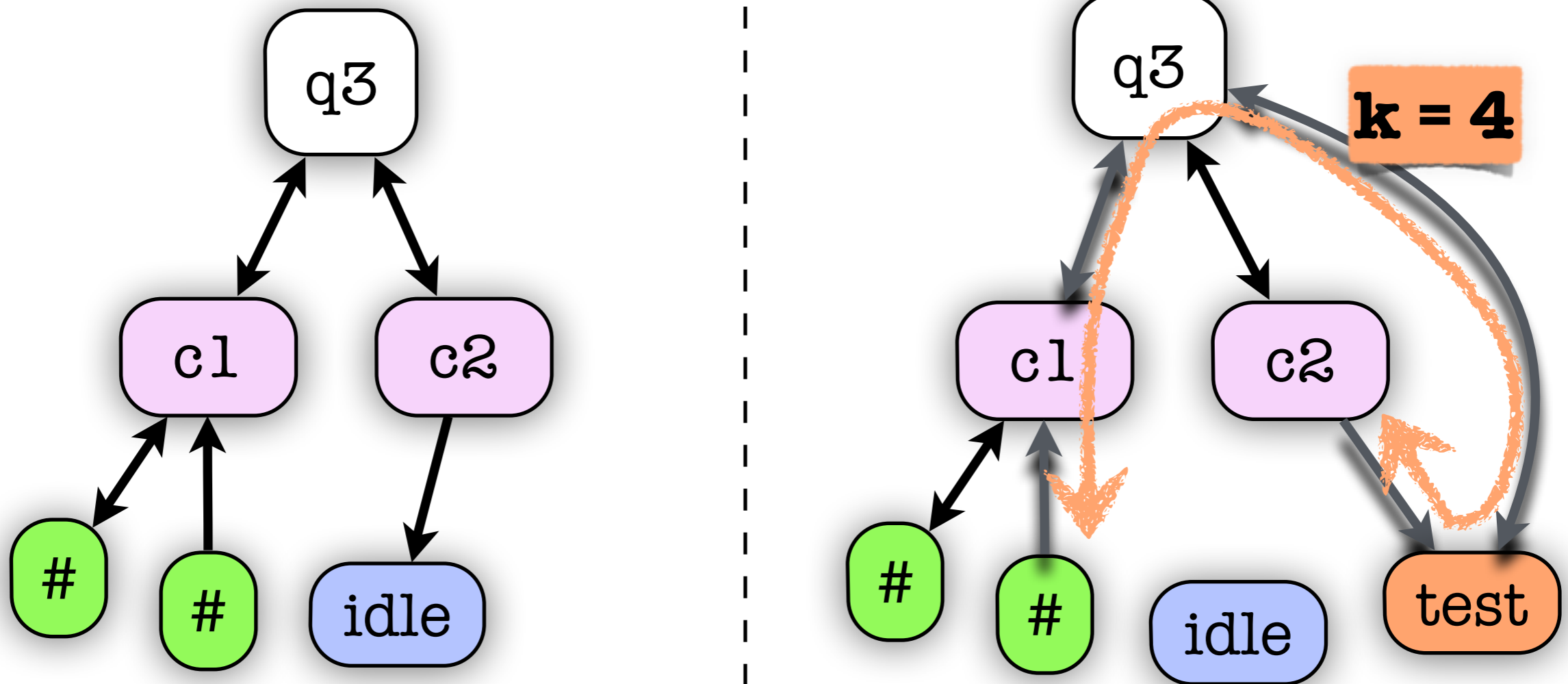
Strongly Bounded DRA

Verification of Dynamic Register Automata



Bound the Simple Path Length of the underlying undirected configuration graph **Undecidable**

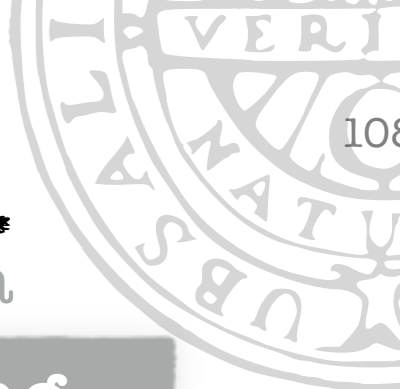
`zerotest(c2)`
→



Two counters Minsky Machine

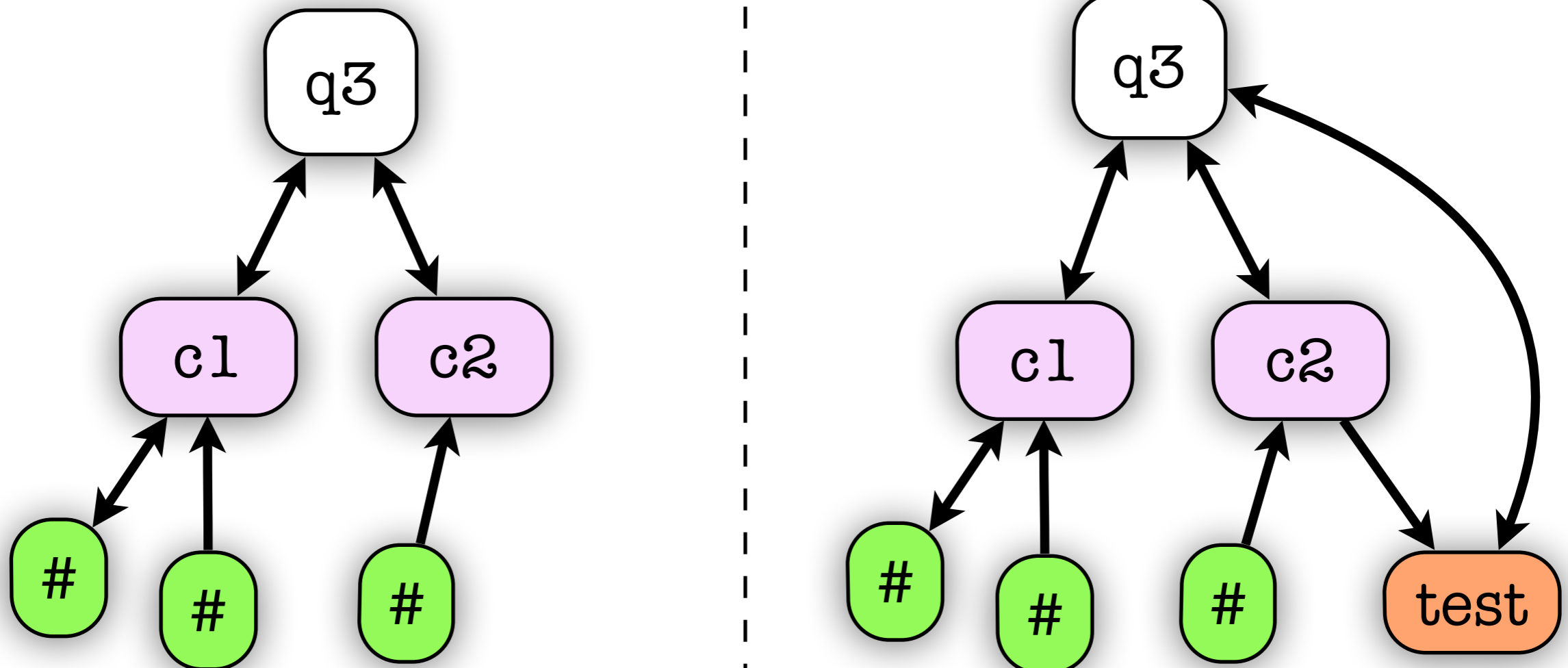
Strongly Bounded DRA

Verification of Dynamic Register Automata



Bound the Simple Path Length of the underlying undirected configuration graph **Undecidable**

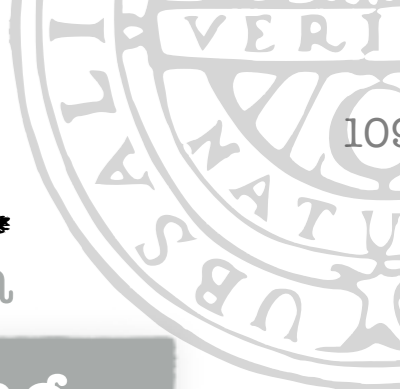
`zerotest(c2)`
→



Two counters Minsky Machine

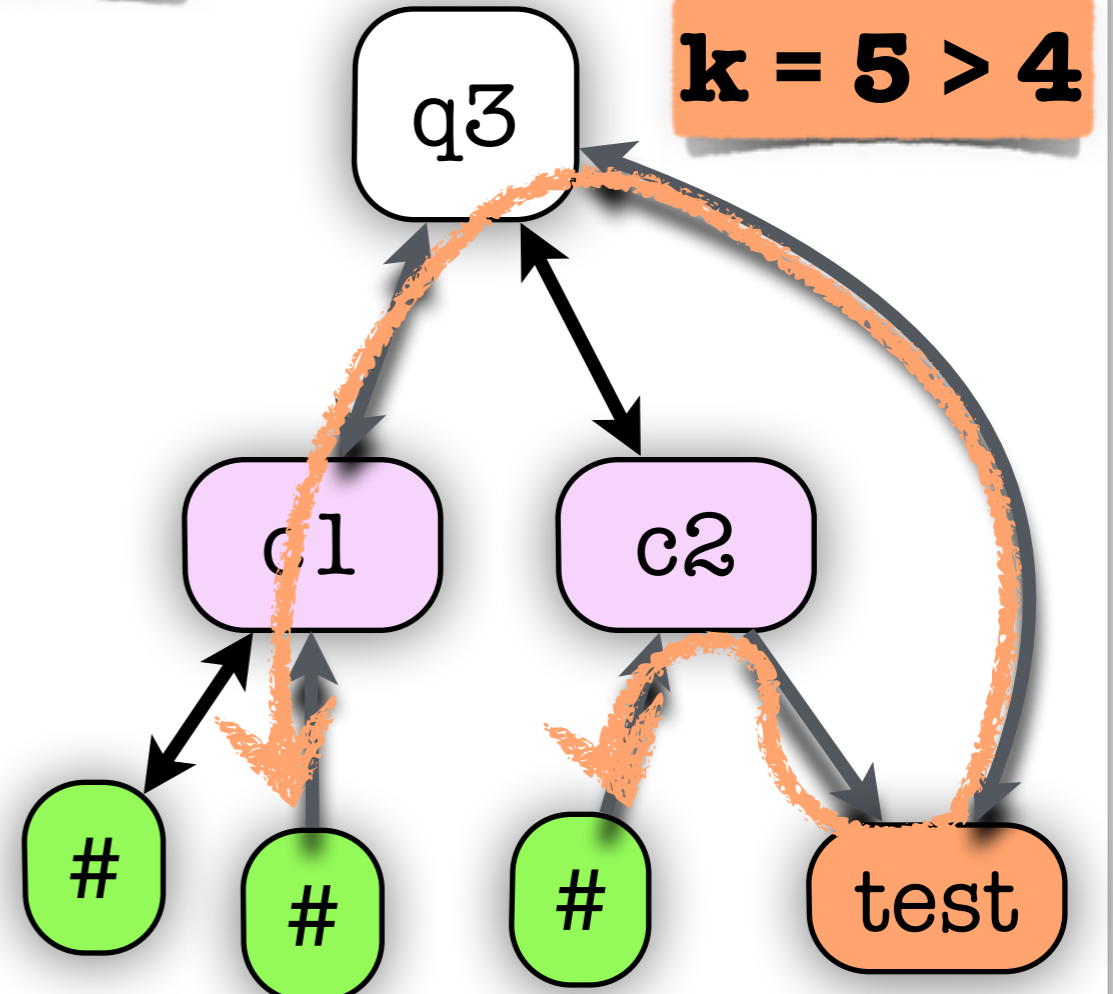
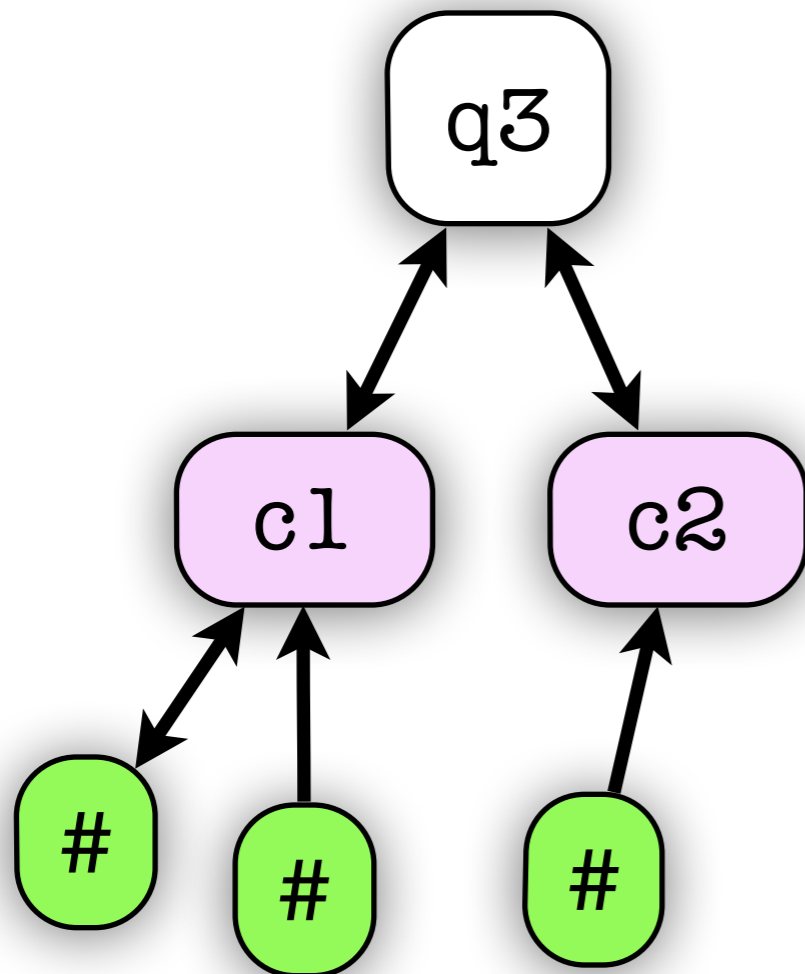
Strongly Bounded DRA

Verification of Dynamic Register Automata



Bound the Simple Path Length of the underlying undirected configuration graph **Undecidable**

`zerotest(c2)`
→



Two counters Minsky Machine

Contribution

Verification of Dynamic Register Automata



State Reachability

Bounded DRA

Undecidable

Strongly Bounded DRA

Undecidable

Strongly Safe DRA

Decidable

Non-Primitive Recursive

Contribution

Verification of Dynamic Register Automata



State Reachability

Bounded DRA

Undecidable

Strongly Bounded DRA

Undecidable

Strongly Safe DRA

Decidable

Non-Primitive Recursive

Contribution

Verification of Dynamic Register Automata



State Reachability

Bounded DRA

Undecidable

Strongly Bounded DRA

Undecidable

Strongly Safe DRA

Decidable

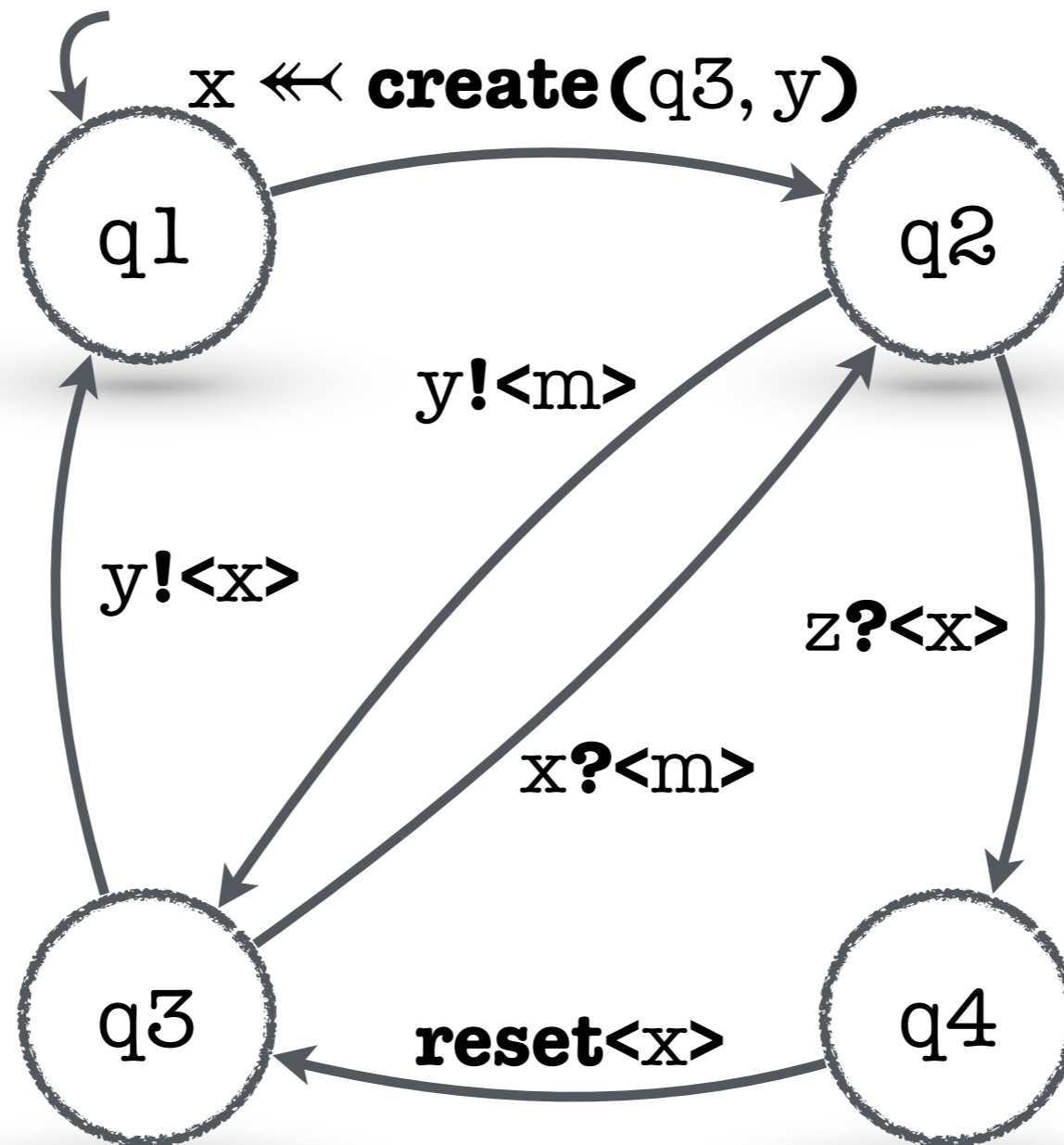
Degenerative DRA

Non-Primitive Recursive

Degenerative DRA

Verification of Dynamic Register Automata

Dynamic Register Automata **D**

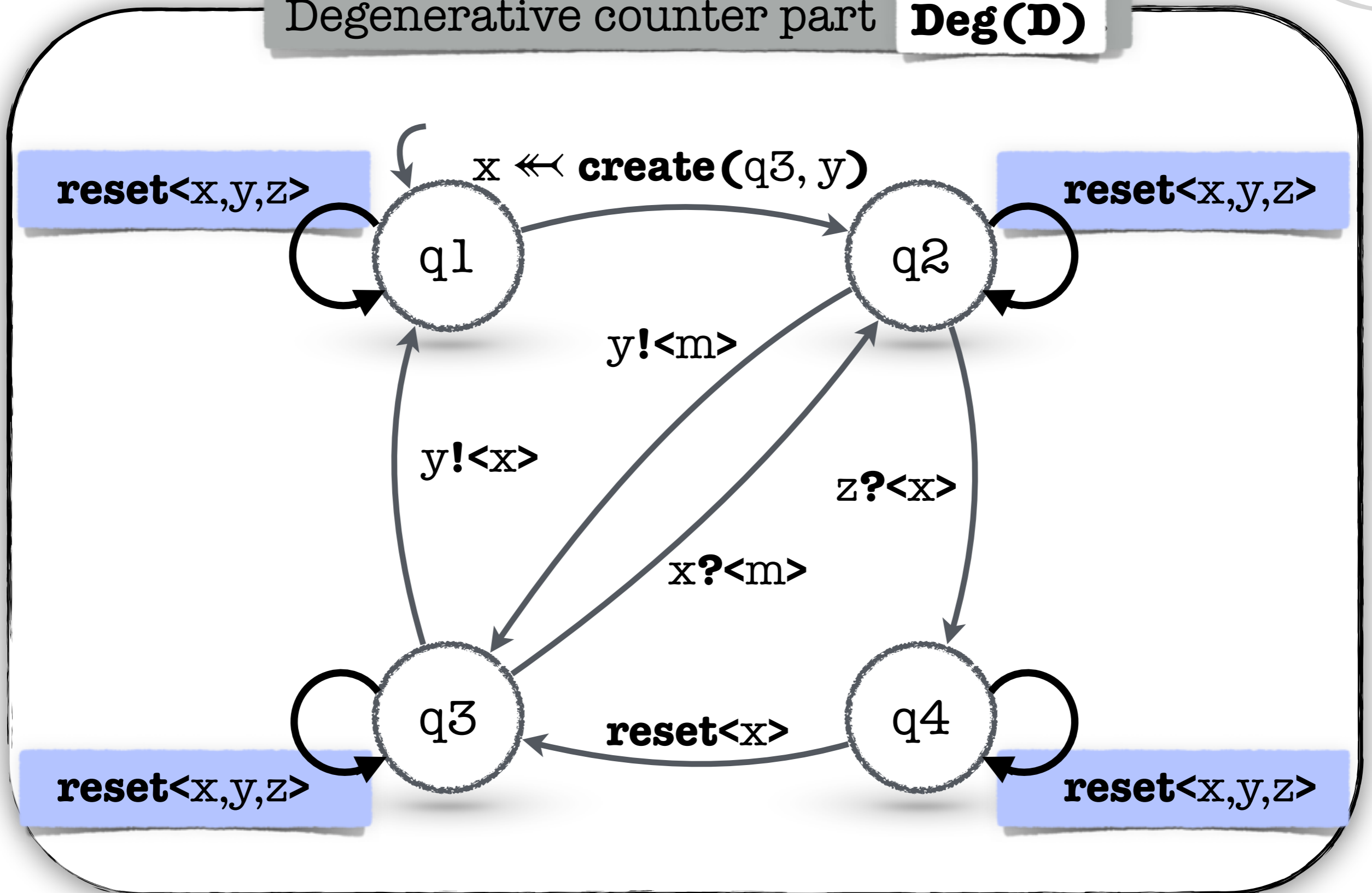


Degenerative DRA

Verification of Dynamic Register Automata



Degenerative counter part **Deg(D)**



Contribution

Verification of Dynamic Register Automata



State Reachability

Bounded DRA

Undecidable

Strongly Bounded DRA

Undecidable

Strongly Safe DRA

Decidable

Degenerative DRA

Non-Primitive Recursive

Strongly Safe DRA

Verification of Dynamic Register Automata



DRA is degenerative



**Bound the Simple Path Length of the
underlying undirected configuration graph**

Strongly Safe DRA

Verification of Dynamic Register Automata



DRA is degenerative



Bound the Simple Path Length of the underlying undirected configuration graph

Well-Structured Transition Systems

[Abdulla et al. 1996], [Finkel et al. 2001]

Symbolic representation of infinite set of configurations

Strongly Safe DRA

Verification of Dynamic Register Automata



Well-Structured Transition Systems

- ▶ Define a **Well-Quasi Order** on configurations
- ▶ Prove **Monotonicity** of Transition Relation
- ▶ Provide an algorithm to compute the **Pre** of an upward closed set

Strongly Safe DRA

Verification of Dynamic Register Automata



Well-Structured Transition Systems

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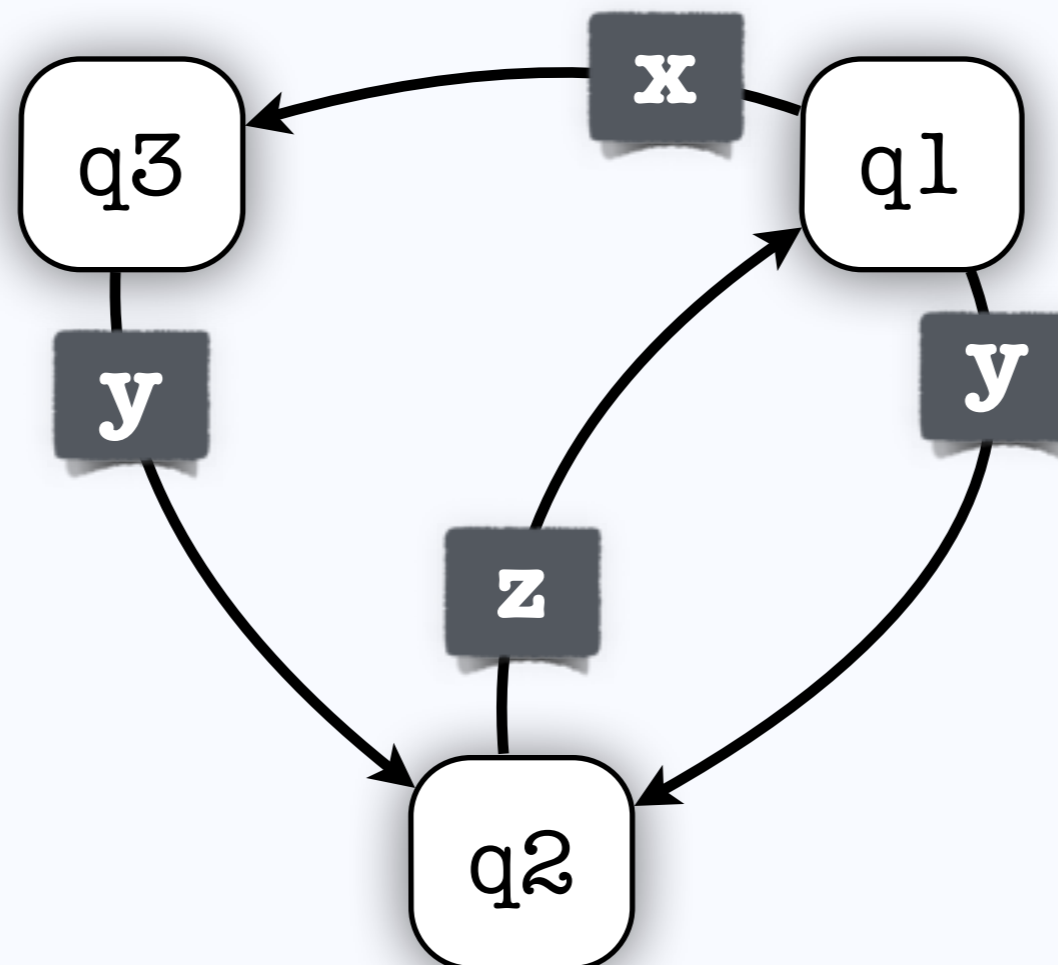
Verification of Dynamic Register Automata



Well-Structured Transition Systems

► Define a **Well-Quasi Order** on configurations

Ordering: subgraph relation



Strongly Safe DRA

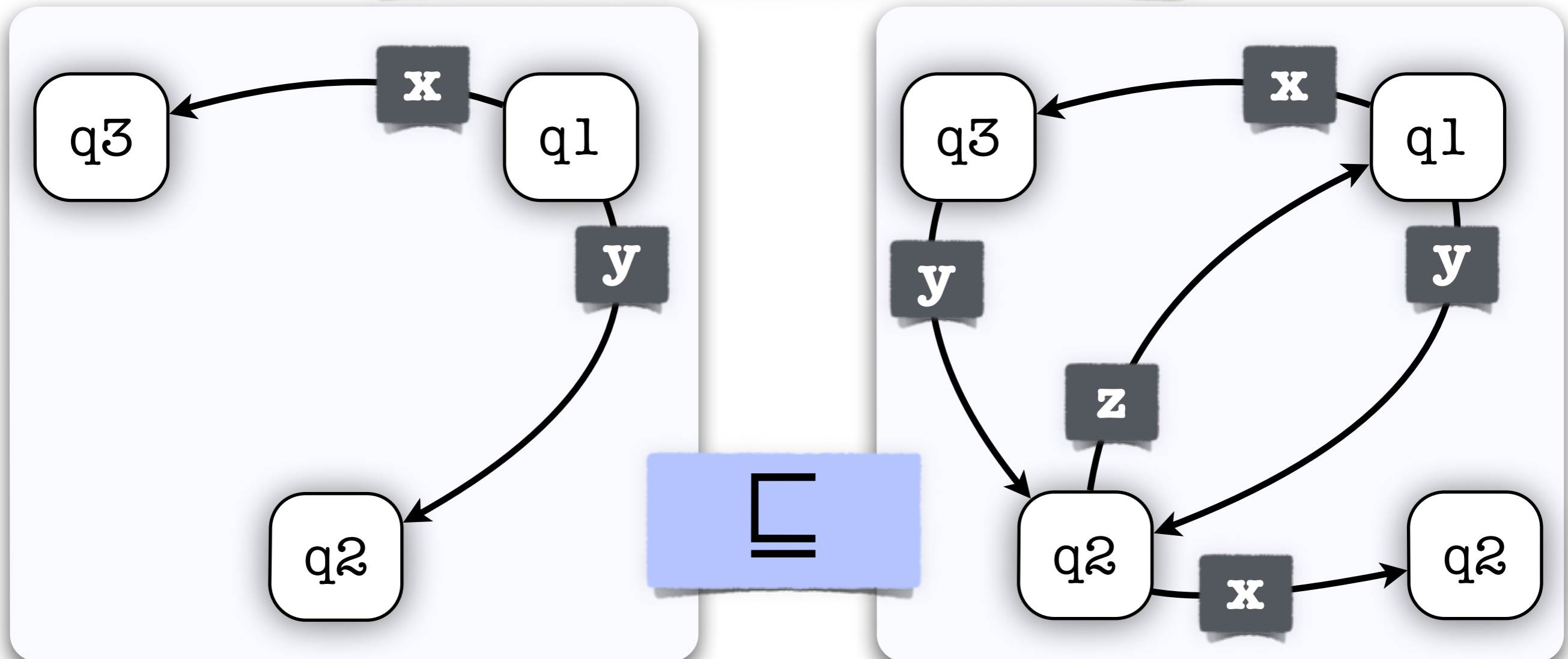
Verification of Dynamic Register Automata



Well-Structured Transition Systems

► Define a **Well-Quasi Order** on configurations

Ordering: subgraph relation



Strongly Safe DRA

Verification of Dynamic Register Automata

Well-Structured Transition Systems

► Define a **Well-Quasi Order** on configurations

Ordering: subgraph relation

[Ding, 1992] Subgraphs and Well-Quasi Ordering

(Induced) subgraph relation is a WQO on Strongly-Bounded graphs

Strongly Safe DRA

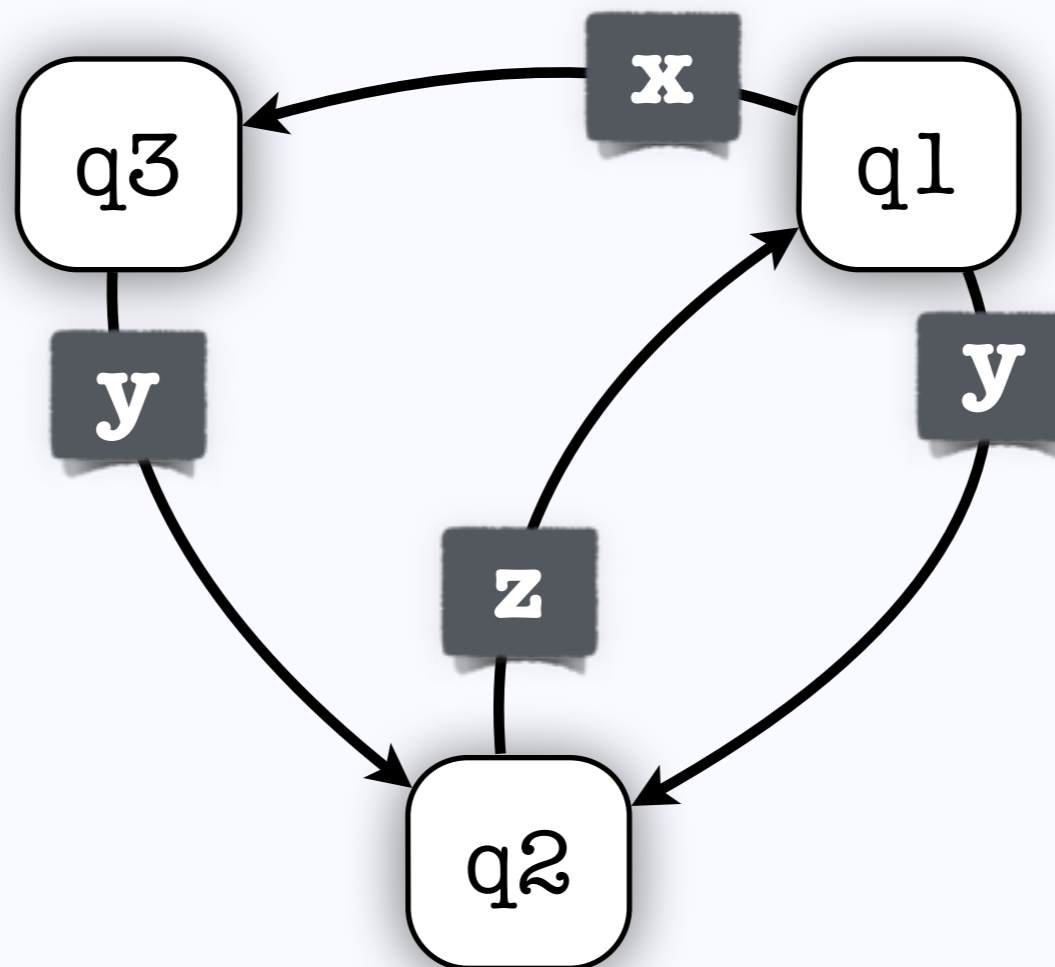
Verification of Dynamic Register Automata



Well-Structured Transition Systems

► Define a **Well-Quasi Order** on configurations

Ordering: subgraph relation



Strongly Safe DRA

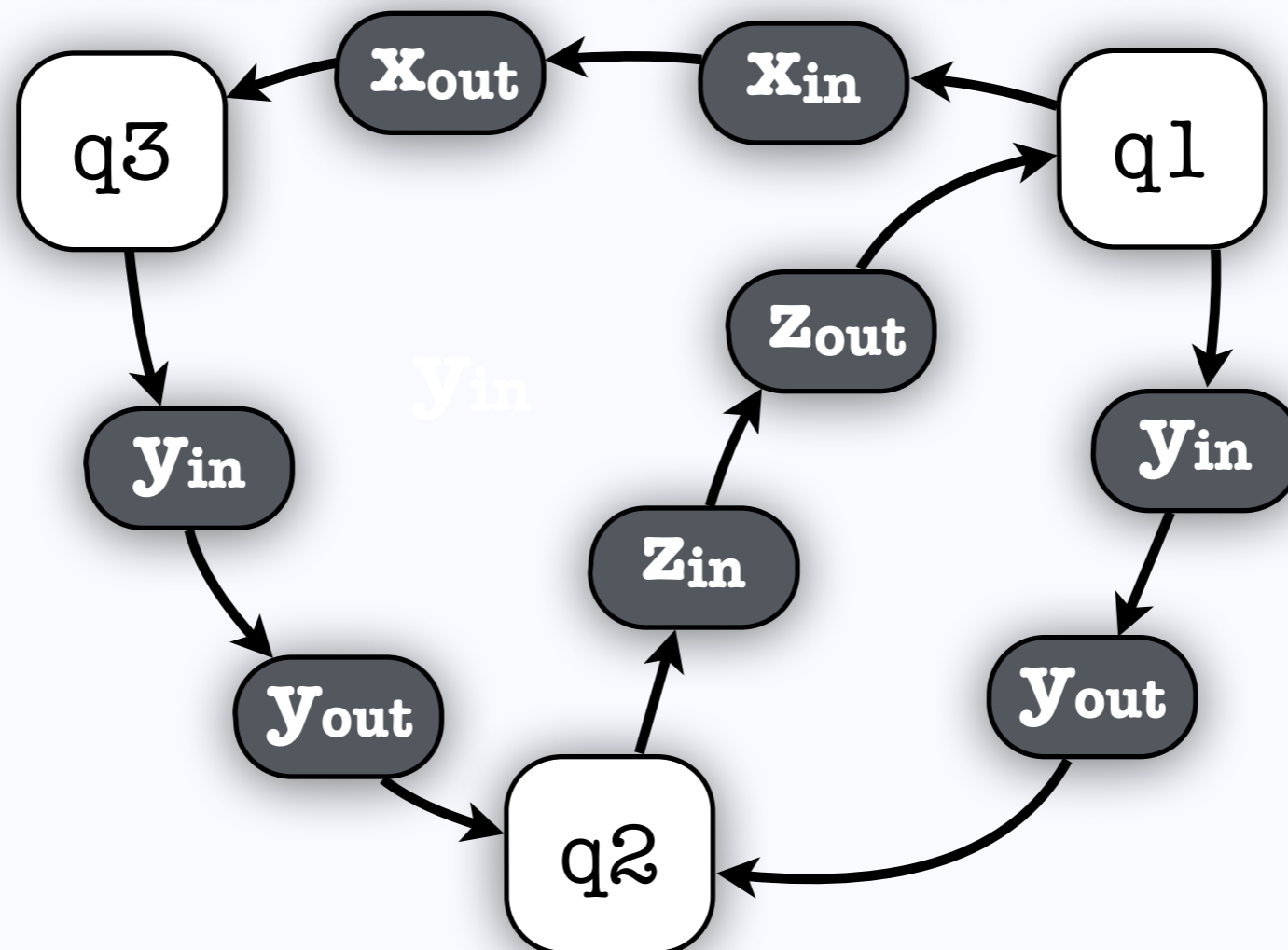
Verification of Dynamic Register Automata



Well-Structured Transition Systems

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Ordering: subgraph relation



Strongly Safe DRA

Verification of Dynamic Register Automata



Well-Structured Transition Systems

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Strongly Safe DRA

Verification of Dynamic Register Automata



Well-Structured Transition Systems

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Strongly Safe DRA

Verification of Dynamic Register Automata



Well-Structured Transition Systems

► Prove **Monotonicity** of Transition Relation

C_2

C_1

C_3

Strongly Safe DRA

Verification of Dynamic Register Automata



Well-Structured Transition Systems

► Prove **Monotonicity** of Transition Relation

C_2

\sqcup

C_1

C_3

Strongly Safe DRA

Verification of Dynamic Register Automata



Well-Structured Transition Systems

► Prove **Monotonicity** of Transition Relation

C_2

\sqsubseteq

C_1



C_3

Strongly Safe DRA

Verification of Dynamic Register Automata



Well-Structured Transition Systems

► Prove **Monotonicity** of Transition Relation

C_2

C_4

\sqcup

C_1



C_3

Strongly Safe DRA

Verification of Dynamic Register Automata



Well-Structured Transition Systems

► Prove **Monotonicity** of Transition Relation

$C_2 \longrightarrow C_4$

\sqcup

$C_1 \longrightarrow C_3$

Strongly Safe DRA

Verification of Dynamic Register Automata



Well-Structured Transition Systems

► Prove **Monotonicity** of Transition Relation

$C_2 \longrightarrow C_4$

\sqcup

$C_1 \longrightarrow C_3$

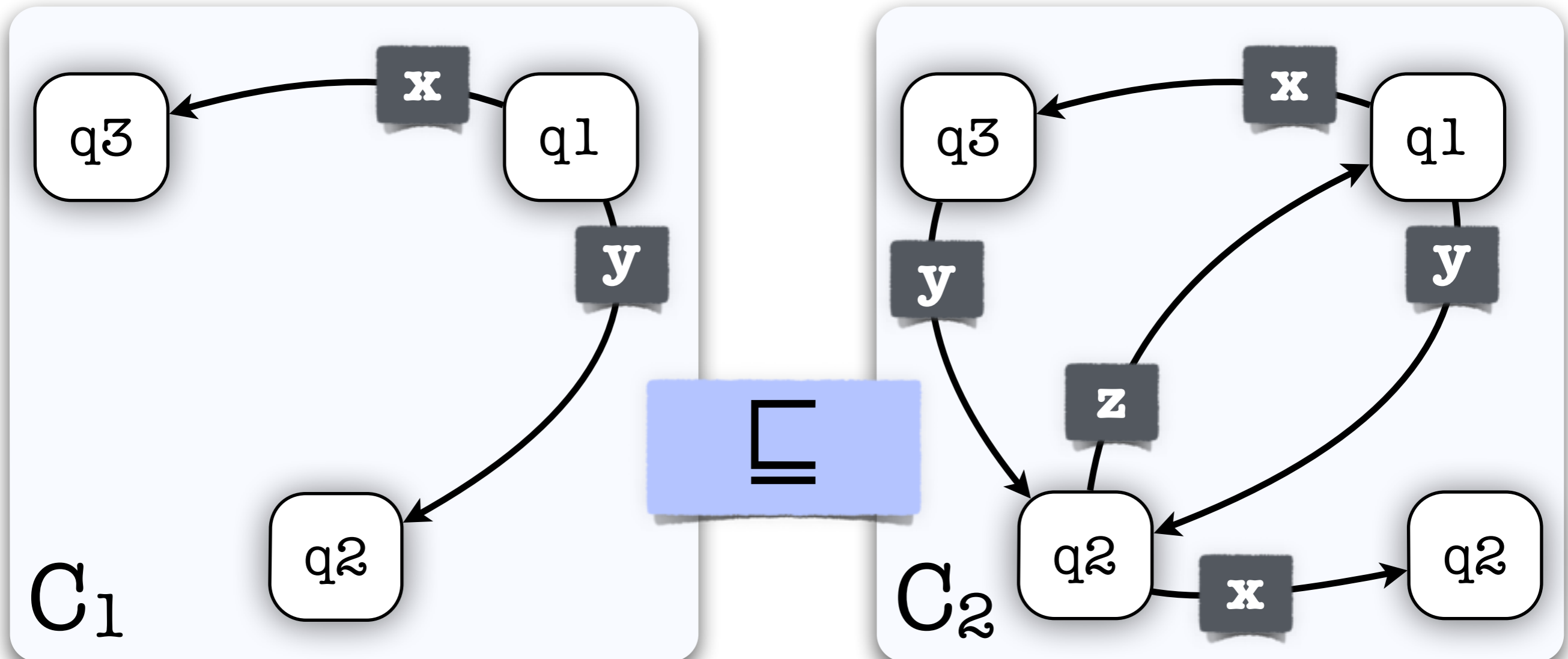
Strongly Safe DRA

Verification of Dynamic Register Automata



Well-Structured Transition Systems

► Prove **Monotonicity** of Transition Relation



Strongly Safe DRA

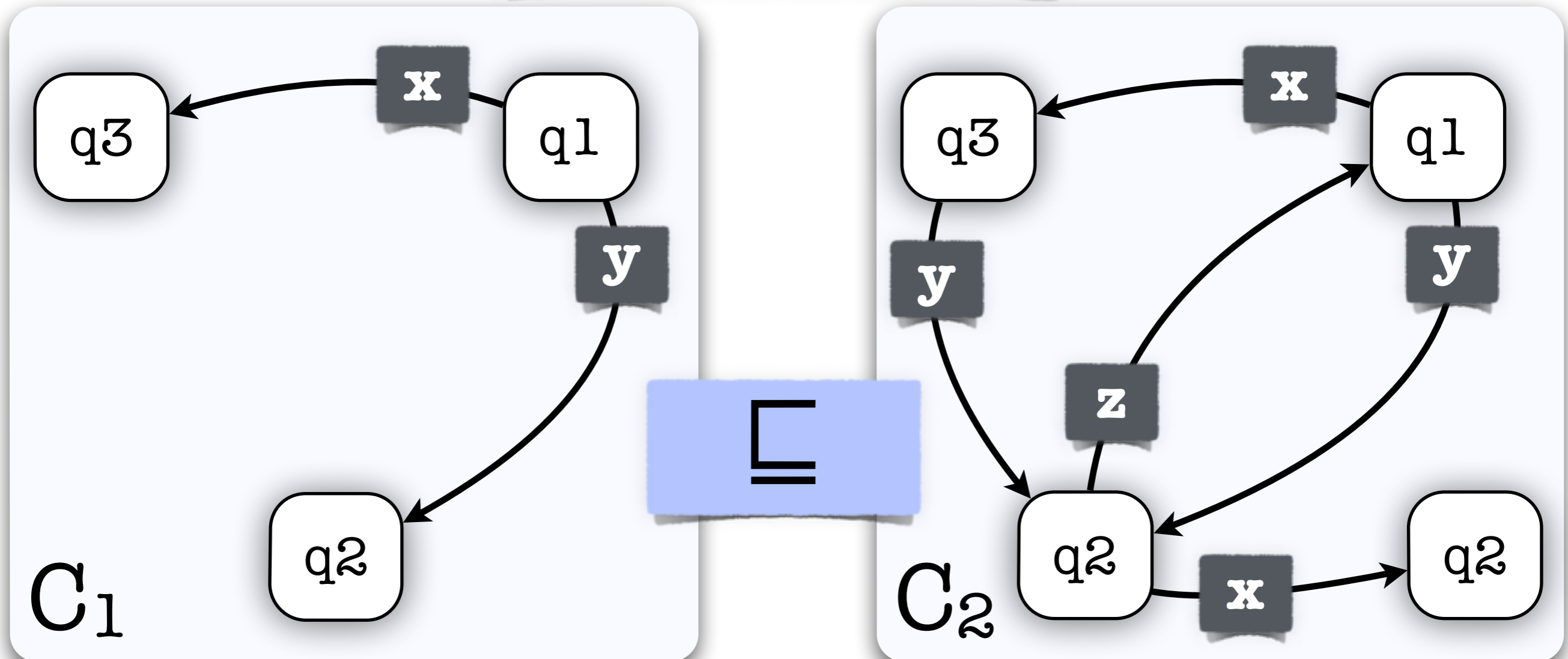
Verification of Dynamic Register Automata



Well-Structured Transition Systems

► Prove **Monotonicity** of Transition Relation

Degenerative



Strongly Safe DRA

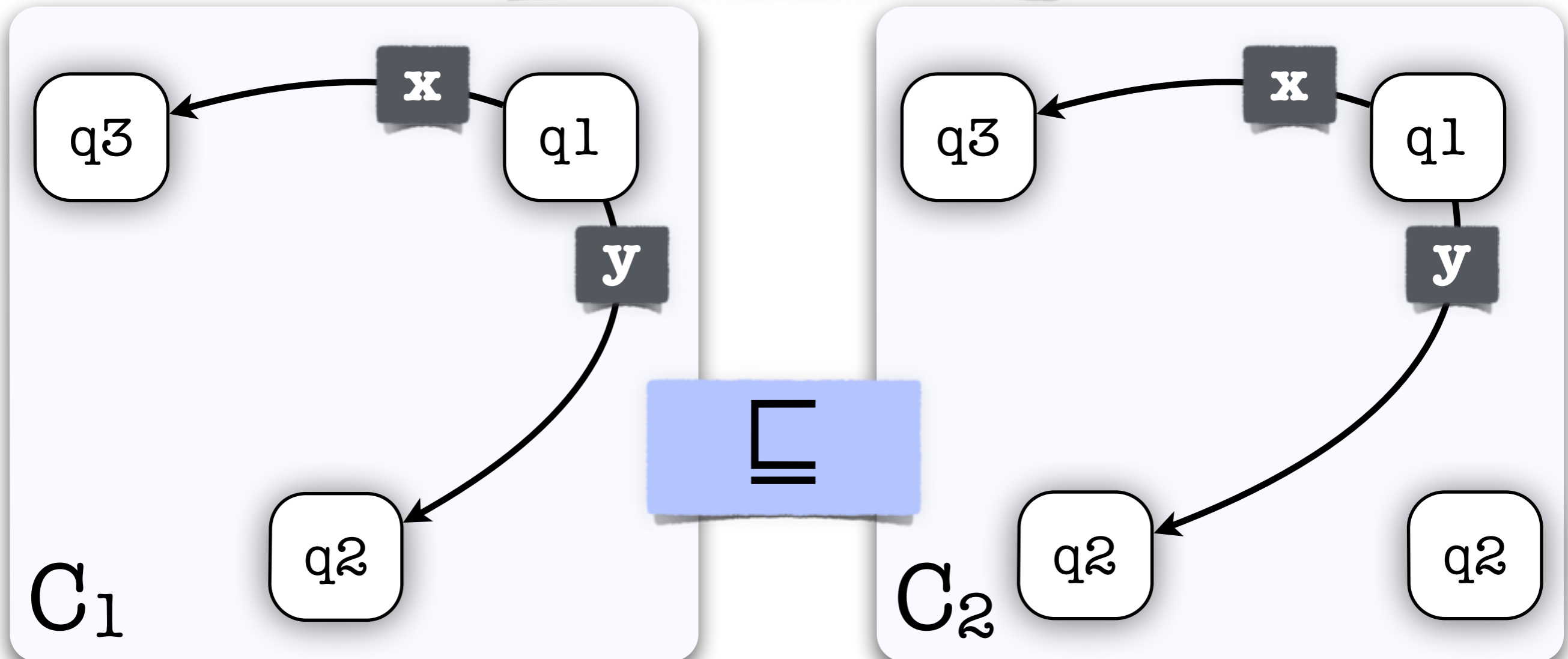
Verification of Dynamic Register Automata



Well-Structured Transition Systems

► Prove **Monotonicity** of Transition Relation

Degenerative



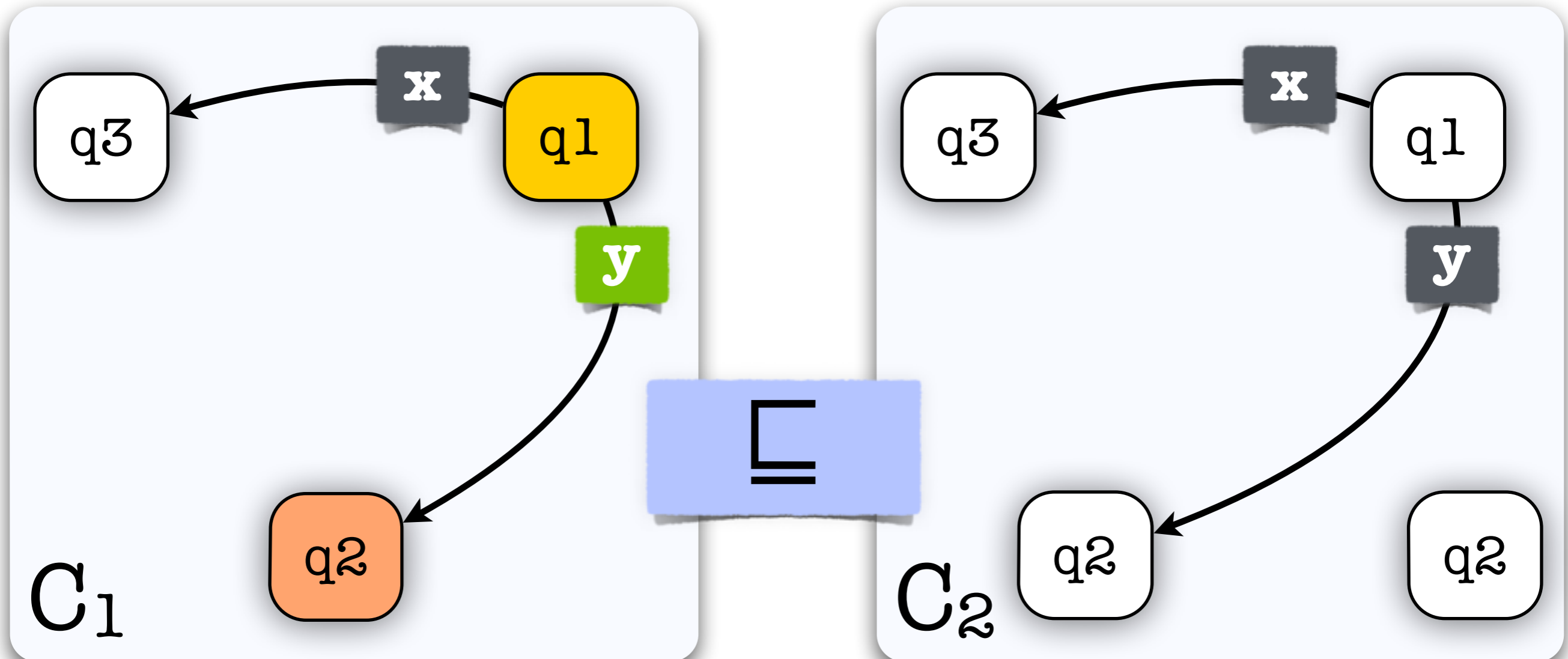
Strongly Safe DRA

Verification of Dynamic Register Automata



Well-Structured Transition Systems

► Prove **Monotonicity** of Transition Relation



Strongly Safe DRA

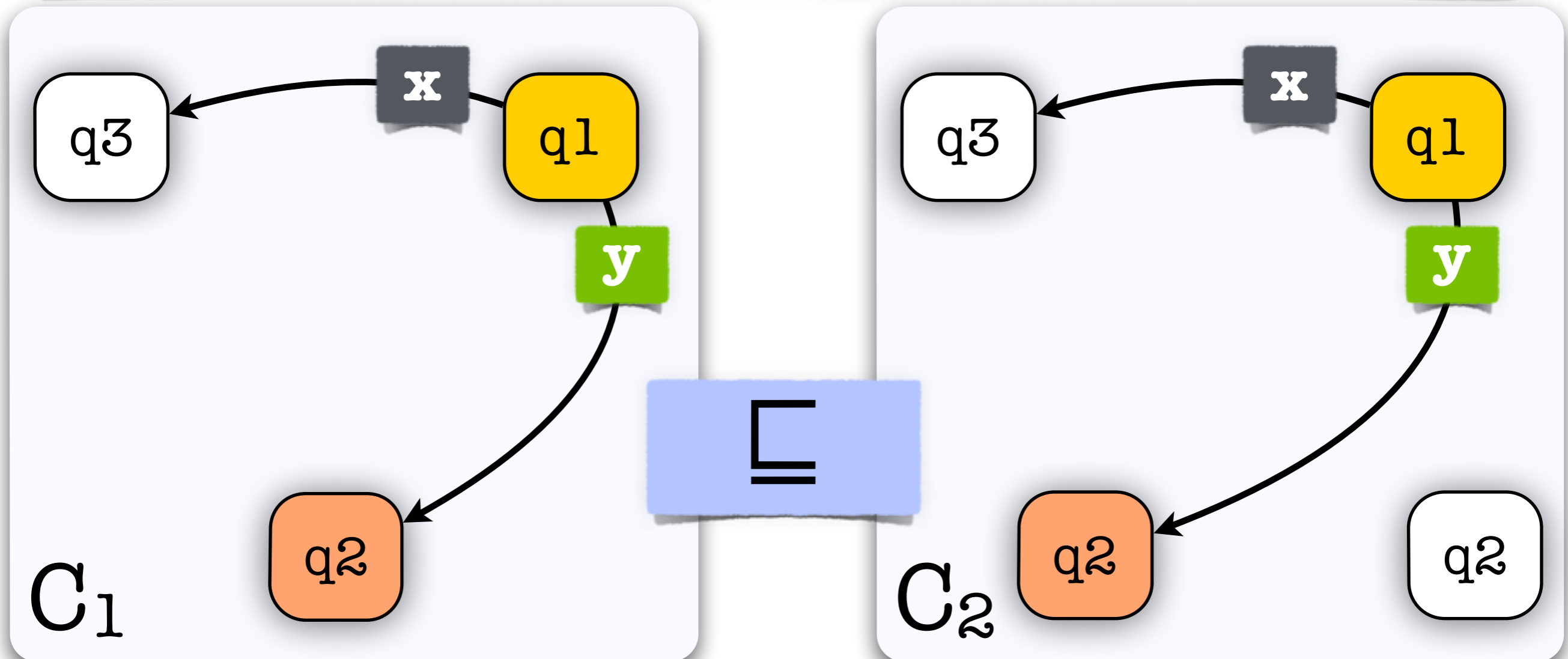
Verification of Dynamic Register Automata



Well-Structured Transition Systems

► Prove **Monotonicity** of Transition Relation

Subgraph relation: Register Mapping & States preserved



Strongly Safe DRA

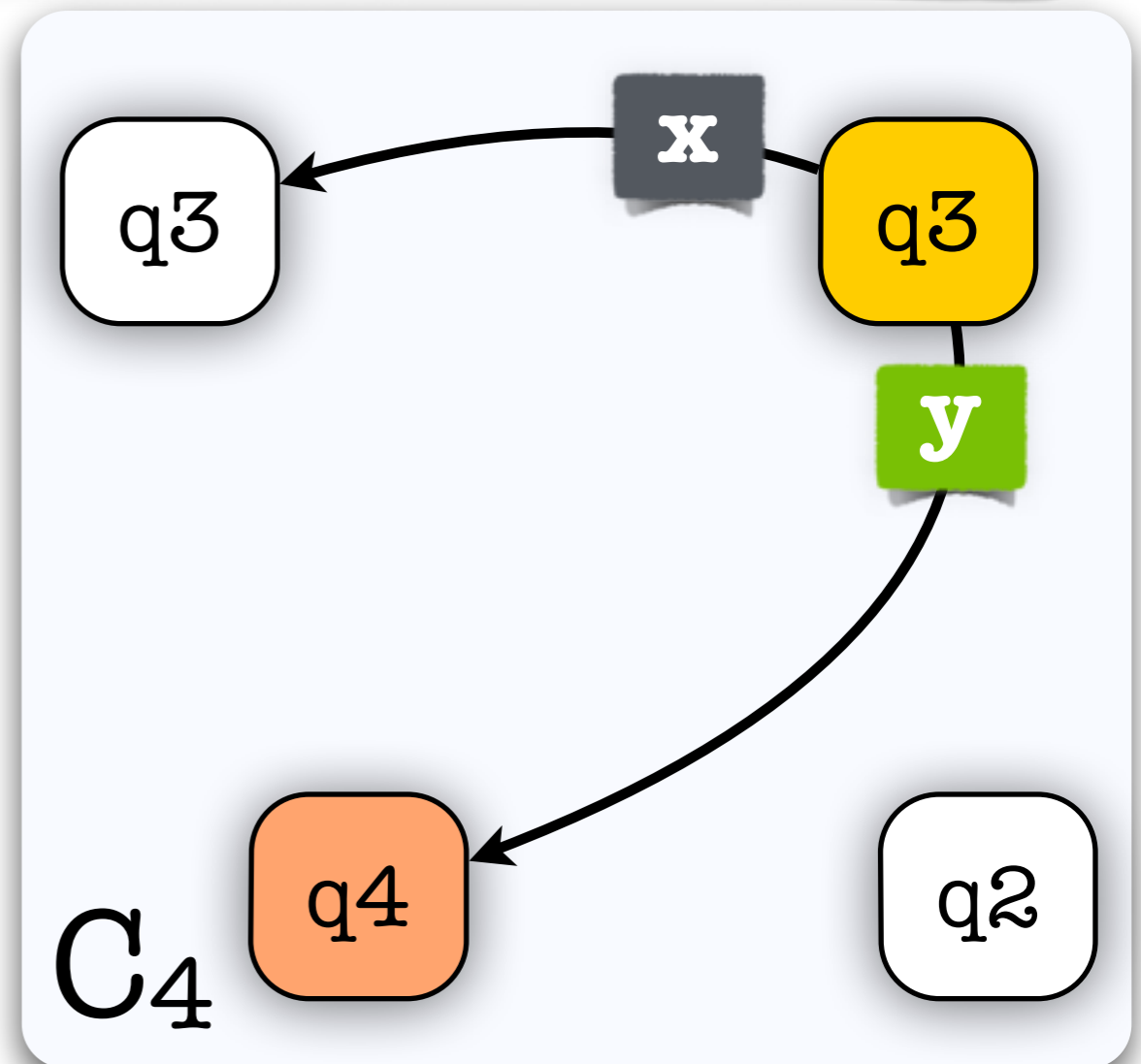
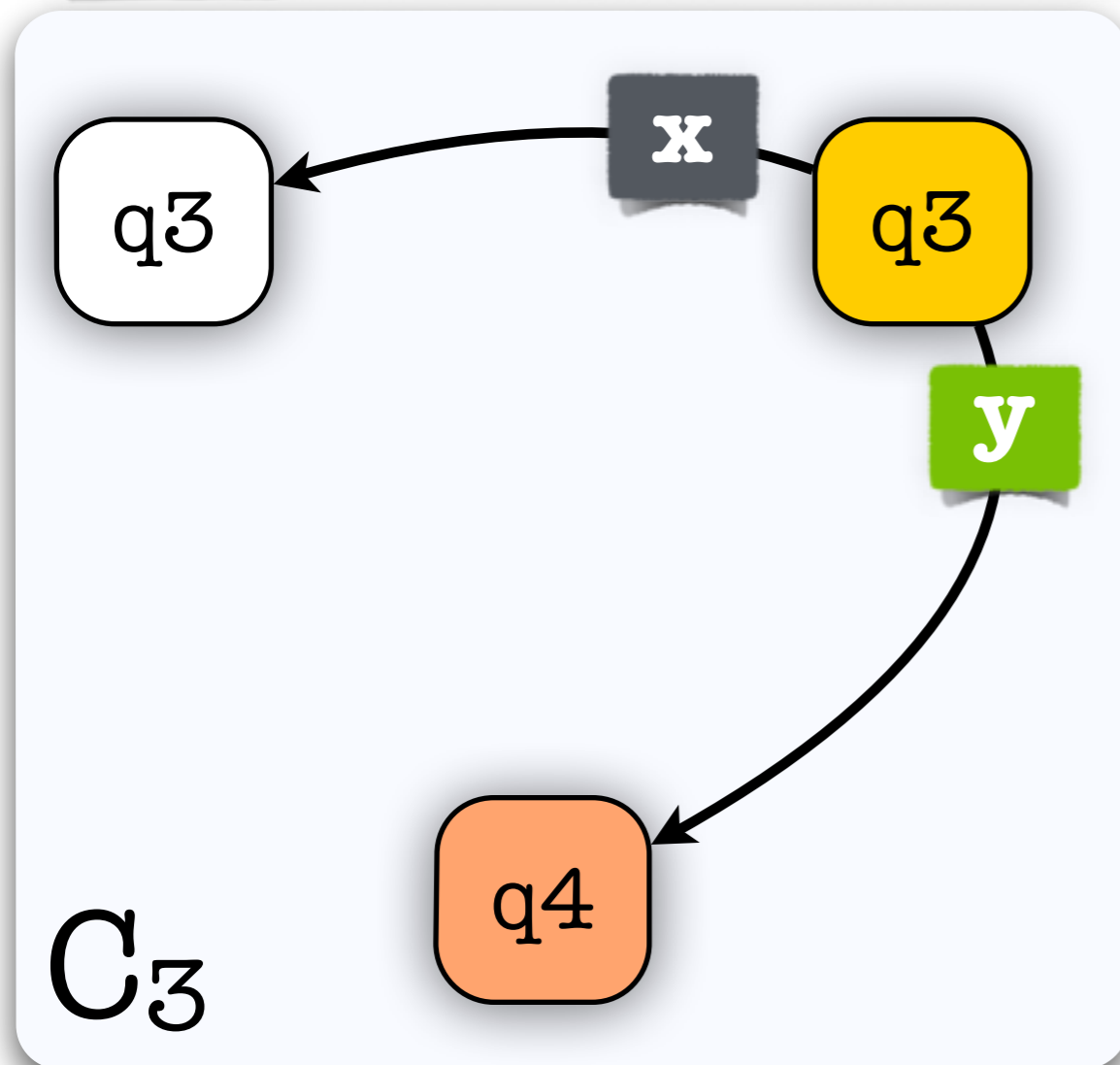
Verification of Dynamic Register Automata



Well-Structured Transition Systems

► Prove **Monotonicity** of Transition Relation

Subgraph relation: Register Mapping & States preserved



Strongly Safe DRA

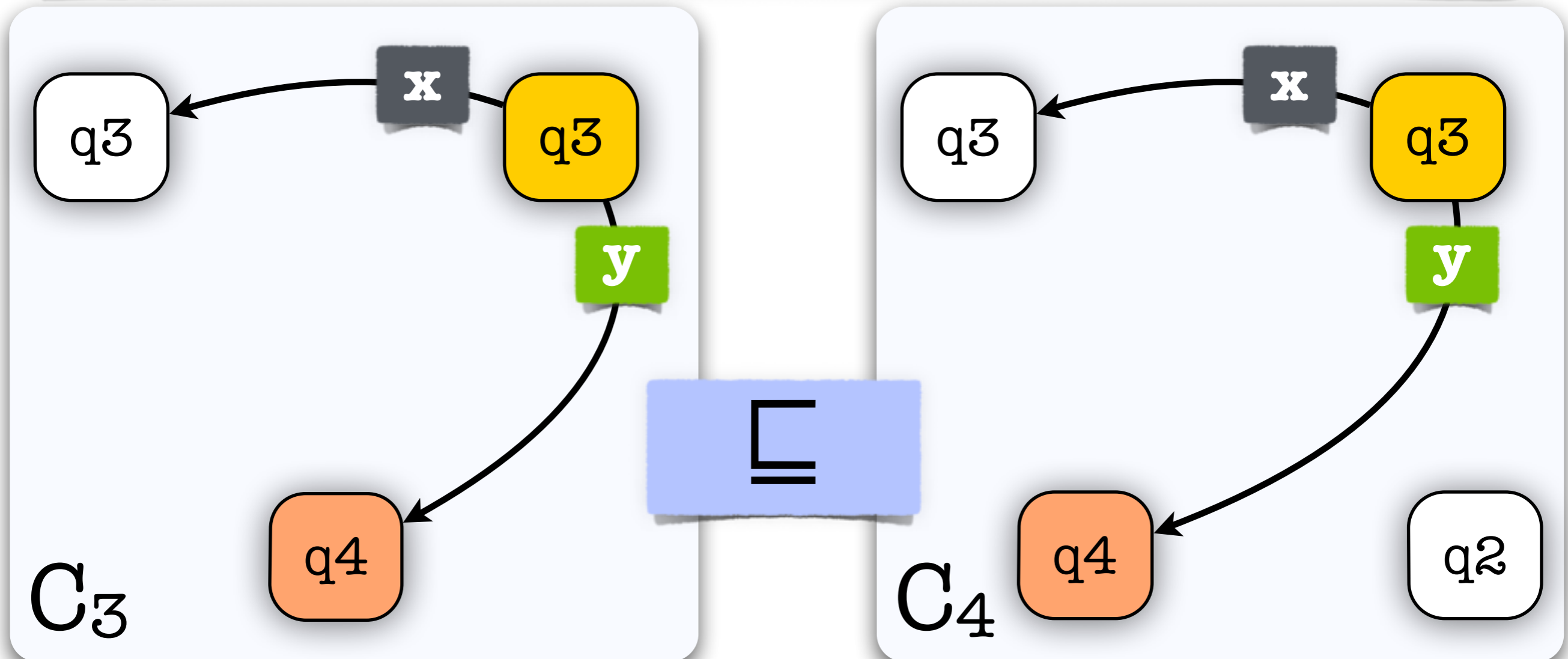
Verification of Dynamic Register Automata



Well-Structured Transition Systems

► Prove **Monotonicity** of Transition Relation

Subgraph relation: Register Mapping & States preserved



Strongly Safe DRA

Verification of Dynamic Register Automata



Well-Structured Transition Systems

- ▶ Define a **Well-Quasi Order** on configurations
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- ▶ Provide an algorithm to compute the **Pre** of an upward closed set

Strongly Safe DRA

Verification of Dynamic Register Automata



Well-Structured Transition Systems

- ▶ Define a **Well-Quasi Order** on configurations
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- ▶ Provide an algorithm to compute the **Pre** of an upward closed set

Contribution

Verification of Dynamic Register Automata



State Reachability

Bounded DRA

Undecidable

Strongly Bounded DRA

Undecidable

Strongly Safe DRA

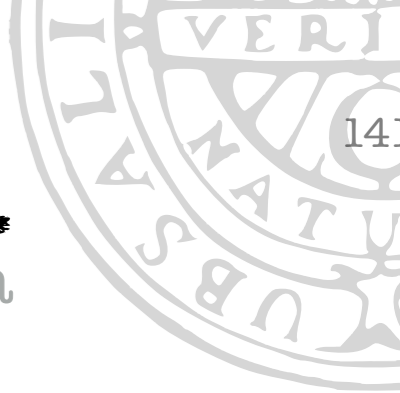
Decidable

Degenerative DRA

Non-Primitive Recursive

Conclusion

Verification of Dynamic Register Automata



Dynamic Register Automata

Dynamic Creation of Processes

Point-to-Point Comm.

Register Mapping

Rendez-Vous Comm.

State Reachability

Bounded DRA

Undecidable

Strongly Bounded DRA

Undecidable

Strongly Safe DRA

Decidable

Non-Primitive Recursive

