Bonus Assignment 1 — Caches and the Memory System

Instructions

- The assignment should be solved *individually*.
- The solutions should be properly *motivated*, a few short sentences is usually enough.
- Answer the questions in *your* own words. Copying answers from other sources, such as the text book, is not acceptable. You may quote other sources, in that case, make sure to include the source and say how you interpret the quoted text.
- Solutions should be given in *English* or *Swedish*, English is preferred.
- Solutions should be posted in *Andreas Sandberg's* mailbox (4th floor in house 1, mailbox number 147) before the deadline.
- Fill out (preferably on your computer) and include this cover page when you hand in your solution.
- Unless you have an excellent handwriting, please use a text editor, TEX or a word processor to write your answers.

Deadline

To get a bonus on the exam, correct solutions must be handed in before the deadline specified on the course homepage. Solutions handed in after the deadline will be marked on a best effort basis and will not result in any bonus on the exam.

Student

Name

Civic registration number (personnummer)

Email address

Date

1 Cache Design

You have already written your civic registration number (personnummer) on the cover page in the format *YyMmDd-XXXX*. Use the following formulas to calculate the parameters of your caches:

$$S = 32 * 2^d \text{ kB} \quad (1)$$

$$L = 32 * 2^D \text{ B} \quad (2)$$

$$A = 2 * 2^m \bmod 4 \quad (3)$$

$$W = 16 * 2^y \bmod 4 \text{ b} \quad (4)$$

1.1 Direct-mapped Cache

Assume that you have a direct mapped cache of size S (Equation 1) with the line size L (Equation 2). The cache is physically indexed and tagged. The physical address is 50 bits, numbered from 0 to 49 (with 0 being the least significant bit). The machine has a word size of W bits (Equation 4) and the memory is byte-addressable.

1. Write your personal values of the parameters S, L, A and W (along with the parameters y, d, D and m).
2. Make a schematic drawing of the cache.
3. Describe which bits are used to index the cache, i.e. used to select the row in the cache.
4. Which bits are compared with the address tag?
5. Which bits are used to select a word from the selected cache line?

1.2 Associative Cache

Now, assume that you have an A-way (Equation 3) set associative cache of size S (Equation 1) and cache line size L (Equation 2).

1. Make a schematic drawing of the cache.
2. Describe which bits are used to index the cache, i.e. used to select the row in the cache.
3. Which bits are compared with the address tag?
4. Which bits are used to select the word to read from the selected cache line?

2 More on Caches

1. Describe how the *LRU* and *RANDOM* replacement policies work.
2. Why would a computer architect choose to implement...
   (a) ...*LRU* instead of *RANDOM*?
   (b) ...*RANDOM* instead of *LRU*?

3. Explain when the following miss types occur and how they can be avoided:
   (a) *Compulsory* misses
   (b) *Capacity* misses
   (c) *Conflict* misses

3 Virtual Memory

1. Describe two problems with a computer that doesn't implement virtual memory.
2. Give at least one reason why a computer system with virtual memory should have a TLB.
3. What is the TLB reach if the page size is 4 kB and the TLB contains 128 entries?
4. What is the benefit of using a *virtually indexed* and *virtually tagged* cache? Are there any problems?
5. What is the benefit of using a *virtual indexed* and *physically tagged* cache? Are there any problems?